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Performance Evaluation of Gate-Driven and Body-Driven MOS-Based Transimpedance Amplifiers

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ABSTRACT

In this paper, a comparative investigations of four transimpedance amplifier (TIA) topologies is performed. Each of the four topologies is precisely designed to fit a diverse range of applications. The discussed topologies of the TIA are the regulated cascode (RGC), the common source (CS) with resistive feedback, the CMOS inverter with resistive feedback, and the composite cascode with resistive feedback. Each topology was studied in both gate-driven (GD) and body-driven (BD) configurations with a thorough evaluation of its performance characteristics provided. Among these topologies, the composite cascode topology is proposed for use for the first time with TIAs in both the gate-driven and the body-driven configurations. The type of applications that are suitable for specific performance metrics are mentioned. The simulation is performed utilizing 130-nm CMOS technology predictive technology model (PTM) with a power-supply voltage, V_{DD}, of 1.2 V for GD configurations and 0.9 V for BD configurations. Finally, the impact of technology scaling on the performance of the GD and BD configurations are investigated.

Keywords: Body-driven, CMOS inverter, Common source, Composite cascode, Gate-driven, Regulated cascode, Transimpedance amplifier.

1. INTRODUCTION

A transimpedance amplifier (TIA) is a crucial electronic component widely used in various applications such as optical communications, photodetection, and sensors. The TIA converts the input current signal into a corresponding output voltage signal. The well-designed TIA must have a low input impedance, Z_{in}, in order to draw most of the source current as well as a low output impedance, Z_{out}, in order to provide a relatively large output voltage signal, thus providing a large overall transimpedance gain. The well-designed TIA must also have a high bandwidth, small area, low power consumption, good linearity, and low input-referred noise current.

Two prominent domains where the TIAs play a pivotal role are optical communications and biomedical sensing. In optical communications, the TIA converts the weak output current of the photodiode into a large output voltage. This process is critical for long-haul data transmission where optical signals attenuate over large distances. In optical communications, ultra-high bandwidth, low distortion, and high dynamic range are essential features for optical signals [1]. On the other hand, biomedical sensing relies on sensitive detectors to convert the biological signals that are extracted from the human body into suitable electrical signals. In this type of applications, the power consumption and the input-referred noise current are the most important performance metrics since the biological signals are

extremely weak; typically in the range of 1 μA to 100 mV [1], [2].

In this paper, two main configurations for the MOS transistor are adopted for designing TIAs with their performance compared in various topologies; they are the gate-driven (GD) and the body-driven (BD) configurations [1]. In the BD devices, the body terminal is used as the input terminal so that the body-source voltage, v_{BS}, acts as the input-signal voltage. This is in contrast to the conventional GD devices in which the gate terminal is used as the input terminal so that the gate-to-source voltage, v_{GS}, acts as the input-signal voltage. The GD devices are suitable for high-speed applications while the BD devices are suitable for low-power applications. The GD devices have higher transconductance, g_m, than that of the BD devices, g_{mb} [3]. The choice between these two configurations depends on the specific requirements of the application, including the power consumption, speed, noise considerations as well as the adopted technology. It must be noted that the BD MOSFETs cannot be integrated with conventional CMOS configurations where the presence of both N and P channel MOSFETs is essential. This is due to the fact that the presence of p/n wells dictates using only NMOS/PMOS transistors. BD MOSFETS also require separate wells during the fabrication process in order to have isolated bulk terminals [3]. These drawbacks require more cost and larger area for fabrication in addition to the difficult matching between differential wells compared to the conventional GD devices.

The remainder of this paper is organized as follows: In section 2, a quick review related to the transimpedance-amplifier design is given including the GD and BD configurations and their employment in particular applications. Section 3 describes the differences of the GD and BD configurations. Section 4 describes the four transimpedance-amplifier topologies. In section 5, a simulation-based comparison between the various GD and BD configurations is presented and discussed with the strong and weak points of each topology emphasized. The impact of technology scaling on the performance of the GD and BD configurations is investigated in Section 6. Finally, Section 7 concludes the paper and directions for future work are presented in Section 8.

2. RELATED WORK

In this section, a brief review on the related work of TIA design is presented. In [4], an innovative topology featuring the implementation of the GD MOSFET was introduced. This topology was designed for operation at intermediate frequencies in optical communication applications. This topology was a single-ended input and differential-output TIA with shunt-shunt feedback. It consists of two cascaded stages, with each stage functioning as a differential amplifier with a resistive load. This TIA was designed to function as a variable gain amplifier achieving a tunable gain range spanning from 51 to 73 dBΩ with a 3-dB bandwidth of 550 MHz. To address the potential issue of unbalanced output signals arising from common-mode signals, a common-mode feedback circuit (CMFB) was employed. Furthermore, to ensure the stability of the topology, compensating capacitances were included.

In [5], two strategies were proposed that aimed to improve the bandwidth of an inverter-based cascode TIA: negative-capacitance compensation (NIC) and inductive peaking. The NIC enhanced the bandwidth by mitigating the overall capacitance. However, it is necessary to carefully design the loop gain of the circuit to avoid any oscillations. Concerning the inductive-peaking approach, the careful selection of inductance becomes crucial to prevent unintended magnitude peaking, thus ensuring that the system operates within the desired performance specification limits. The design was well-suited for applications requiring a data rate up to 20 Gb/s.

The study of [6] discussed a novel regulated cascode-based TIA designed for optical applications operating at speeds up to 5 Gb/s. This TIA achieved a high gain of 60 dBΩ by adding extra cascode transistor to the topology, and its bandwidth was extended through the use of an active inductor, thus avoiding limitations associated with passive inductors. This circuit consumed 760 μW, thus emphasizing a balance between performance and energy efficiency. The TIA was followed by three stages of differential limiting amplifiers to further boost the gain and ensure a large voltage swing which is required in an optical receiver.

The proposed design in [7] relied on a modified cross-coupled (CC) RGC. This design introduced two local feedback mechanisms for transconductance boosting, effectively mitigating the power consumption. The design achieved a low input impedance, thus leading to a wide bandwidth without introducing peaking in the magnitude response. Furthermore, this topology maintains the same gain as the conventional CC RGC, thus exhibiting an efficient and improved solution for achieving broader bandwidth without sacrificing gain in the amplifier design.

The TIA proposed in [8] has a boosted transconductance. This design achieved a remarkably low input resistance by incorporating a negative-feedback stage to enhance the bandwidth. This TIA was designed by a modified long-tailed pair differential amplifier offering high gain. Additionally, this TIA included a compensating capacitor to ensure stability and consumes ultra-low power making it a suitable TIA for biomedical applications.

The TIA suggested in [8] combined the topologies of both the current-mirror and the folded-cascade based designs. The resulting TIA adopts a diode-connected transistor to achieve a low input resistance. The diode-connected transistor plays a key role in isolating the

dominant input capacitance, thereby enhancing the overall performance of the amplifier. As this circuit consumes only very low power (only 315 μW), this TIA is expected to be suitable for biomedical applications.

The research of [9] includes a comparison between various TIA topologies that are suitable for biomedical applications, specifically common-source based TIA, inverter-based cascode TIA, regulated inverter-based cascode TIA, common-gate TIA, and regulated-cascode TIA. This study highlighted the fact that in closed-loop topologies, higher open-loop gain is associated with improved performance. Additionally, this research suggested that employing transconductance-boosting techniques, as seen in inverter-based cascode and regulated cascode stages, significantly enhances the gain-bandwidth product (GBW) and reduces the input-referred noise current. Notably, the inverter-based cascode TIA and the regulated inverter-based cascode TIA exhibit superior performance in terms of the GBW, low input-referred noise current, and low power consumption, making them highly recommended for applications where sensitivity is a primary concern.

The search of [10] introduced a novel optical receiver architecture consisting of a TIA and four stages of differential-limiting amplifiers. The TIA depends on the current-mirror topology with shunt-shunt feedback and incorporates an active inductor at the output node. The active inductor was designed to resonate with the load capacitance, thus introducing a zero that effectively cancels the impact of the output pole. This TIA was followed by the four limiting amplifier stages, each employed two active inductors as a load for extending the bandwidth. These limiting amplifiers enhance the overall gain of the receiver, at the cost of an increased thermal noise. The whole receiver achieves a 3-dB bandwidth of 6.55GHz with a gain of 71.4 dBΩ and consumes only 7.7 mW.

The study of [11] introduced a variable gain inductorless TIA. The TIA is composed of an input stage with a single-ended input and a differential output utilizing a modified cross-coupled RGC followed by a modified f_T-doubler as a second stage employing a unique combination of active inductor and capacitive degeneration for bandwidth enhancement. The second stage also utilized a CMFB circuit. This TIA exhibited a gain range of 37.5–58.7 dBΩ and a bandwidth of 4.15 GHz, thus demonstrating its suitability for high-speed visible light communication applications; specifically those that require variable gain.

The BD MOSFETs were used in [12], [13], [14] to highlight the significance of achieving low-voltage low-power operation in the environment of an implanted biosensor system. A differential-amplifier based multiple input BD MOSFET was presented in [15] employed the 180-nm CMOS technology with a V_{DD} of 0.5 V. Both the circuit complexity and the power dissipation were reduced using this configuration. The open-loop gain of 62 dB was obtained with a 65.4-kHz bandwidth. This configuration is well suitable for low-power low-frequency applications. A BD-based OTA was implemented in [16] adopting a V_{DD} of 0.5 V. This circuit consumed only 31.3 nW, making it the best choice for biomedical applications.

The research in [17] involved a comparison between the GD and the BD MOSFETs with a particular focus on the current-mirror topology. It highlighted the importance of low-power low-voltage circuits in guaranteeing device reliability and mitigating overheating.

3. MOSFET MODELS

In this section, the small-signal equivalent circuit of the GD and BD configurations are presented. These circuits will be used in deriving compact-form expressions for the performance metrics of the TIAs based on these two configurations.

1.1 The Gate-Driven MOSFET

As well known, the GD MOSFET is a voltage-controlled device. The voltage applied on the gate terminal controls the current flowing between the drain and source terminals. The threshold voltage, V_{thn}, places a substantial restriction on the signal swing in this type of configurations, thus limiting the use of low supply voltages. Figure 1 illustrates the small-signal equivalent circuit of the GD MOSFET [18]. The transconductance, g_m, of a MOSFET is a measure of its ability to convert an input-voltage signal into an output-current signal. Its value is usually relatively large.

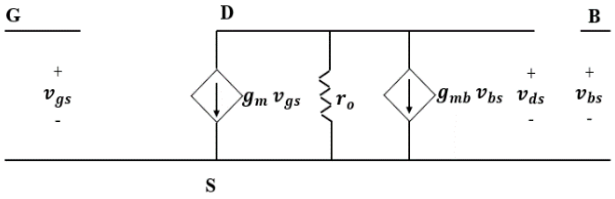


Figure 1: The small-signal equivalent circuit of the GD MOSFET in the saturation region. r_0 is the inverse of g_o where g_o is the drain-to-source conductance [18].

1.2 The Body-Driven MOSFET

In the BD MOSFET, a bias voltage is applied between the gate and source terminals to ensure a continuous and suitable drain current and saturation-region operation while the input signal is applied to the body terminal. In fact, the operation of the MOSFET transistor in this configuration is very similar to that of the junction field-effect transistor (JFET) [3]. A channel exists between the source and the drain of the MOSFET transistor due to the applied gate voltage, with its width remaining constant unless the gate bias varies. The body terminal serves as a second gate (also known as the back gate [3]). It can also operate with bias voltages of negative, zero, or slightly positive values. The operation in the positive direction is limited to slight values in

order to avoid the latch-up which can occur at a forward biasing voltage of typically 0.5 V.

Due to the capability of operation with bipolar voltages, the V_{thn} constraint is entirely eliminated in the BD devices, thus allowing these devices to function with power-supply voltages lower than 1 V without affecting the signal swing significantly [17]. Due to the fact that the value of the transconductance of the body-driven MOSFET, g_{mb}, is lower than g_m, the price paid is the potential reduction in gain and bandwidth for the BD devices assuming identical values for the other parameters [3]. The small-signal gain of a BD-based amplifier can outperform that of the GD-based one only when $V_{SB} \geq 0.5$ V as the g_{mb} becomes larger than g_m in this range [3]. Figure 2 shows the small-signal equivalent circuit of the BD MOSFET [18].

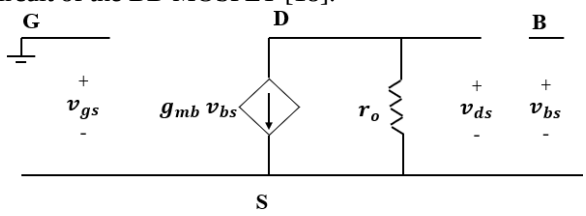


Figure 2: The small-signal equivalent circuit of the BD MOSFET in the saturation region [18].

As well known, the body effect results from the dependence of the threshold voltage, V_{thn}, on the source-to-body voltage, V_{SB}, as follows [18]

$$V_{thn} = V_{thn0} + \gamma \left[\sqrt{2\varphi_f + V_{SB}} - \sqrt{2\varphi_f}\right] \quad (1)$$

where V_{thn0} is the threshold voltage for $V_{SB} = 0$, φ_f is a physical parameter related to the energy-band diagram, and γ is the body-effect coefficient. It is given by

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_s}}{C_{ox}} \quad (2)$$

In the latter equation, q is the magnitude of the electron charge, N_A is the doping concentration of the p-type substrate, $\boldsymbol{\varepsilon}_s$ is the permittivity of silicon, and C_{ox} is the gate-oxide capacitance per unit area. For the case of p-channel devices, N_A must be replaced with N_D which is the doping concentration of the n-type well in which the PMOS transistor is fabricated.

4. TRANSIMPEDANCE-AMPLIFIER TOPOLOGIES

In this section, the various topologies of the TIA are presented including the RGC, the CS, the CMOS inverter, and the composite-cascode topologies. Each topology adopted negative feedback in order to gain various merits such as stabilizing the output signal against any parameter or process variations, expanding the 3-dB bandwidth, and decreasing the input and the output impedances which are good features for the TIA.

4.1 The Regulated-Cascode Topology, RGC

As illustrated in Figure 3, the RGC topology consists of the main amplifier, M_1, with resistive load, R_{D1}, and a feedback network consists of M_2 and R_{D2}. M_1 and M_2 operate in the saturation region. The gains of the GD and BD RGC TIAs are given by

$$TIA\ Gain_{\ RGC,\ GD} = R_{D1}\frac{g_{m1} + g_{mb1} + \frac{1}{r_{o1}} + g_{m1}\, g_{m2}R_{D2}}{\frac{1}{R_S} + g_{m1} + g_{mb1} + \frac{1}{r_{o1}} + g_{m1}\, g_{m2}R_{D2}} \quad (3)$$

$$TIA\ Gain_{\ RGC,\ BD} = \frac{g_{m1}R_{D1}(1 + g_{m2}R_{D2})}{\frac{1}{R_S} + g_{m1} + g_{m1}g_{m2}R_{D2}} \quad (4)$$

respectively. The input impedances of the GD and BD RGC TIAs are given by

$$Z_{in\ RGC,GD} = \frac{1}{g_{m1} + g_{mb1} + g_{m1}g_{m2}R_{D2} + \frac{1}{R_S // \frac{1}{SC_{in}}}} \quad (5)$$

$$Z_{in\ RGC,BD} = \frac{1}{g_{m1} + g_{m1}g_{m2}R_{D2} + \frac{1}{R_S // \frac{1}{SC_{in}}}} \quad (6)$$

respectively. The output impedances of the GD and BD RGC TIAs are approximately the same and are both equal to

$$Z_{out\ RGC} = R_{D1} // \frac{1}{SC_{out}} \quad (7)$$

The 3-dB frequencies of the GD and BD RGC TIAs are given by

$$f_{3-dB\ RGC,GD} \approx \frac{1}{2\pi\, R_{in}\, [C_{in} + C_{gs2} + C_{gd2}(1 + g_{m2}\,(R_{D2} // r_{o2}))]} \quad (8)$$

$$f_{3-dB\ RGC,BD} \approx \frac{1}{2\pi R_{in}\,(C_{in} + C_{gs2})} \quad (9)$$

respectively. In general, the RGC based TIA exhibits notable features, primarily its ability to compensate the effect of the photodiode capacitance on bandwidth, thanks to its low input impedance and the incorporation of local feedback [19]. Despite this advantage, this topology suffers from the instability and the limited voltage headroom. As the RGC is a third-order system, careful design to maintain an acceptable phase margin is necessary. Concerning the voltage-headroom issue and to ensure that the transistors operate in the saturation mode, a DC level shifter, typically implemented by an additional transistor, can be employed. However, this solution comes at the expense of an increased power consumption [20].

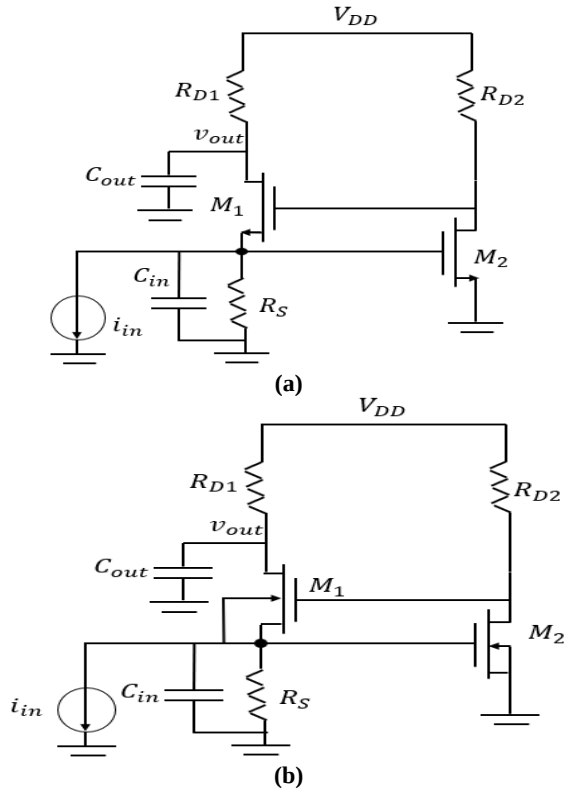


Figure 3: a) The GD conventional TIA RGC topology. b) The BD conventional TIA RGC topology.

4.2 The Common-Source Topology, CS

The CS topology, which is shown in Figure 4, consists of the main amplifier, *M*, with a resistive load, R_D, and a resistive feedback resistor, R_f. *M* operates in the saturation region.

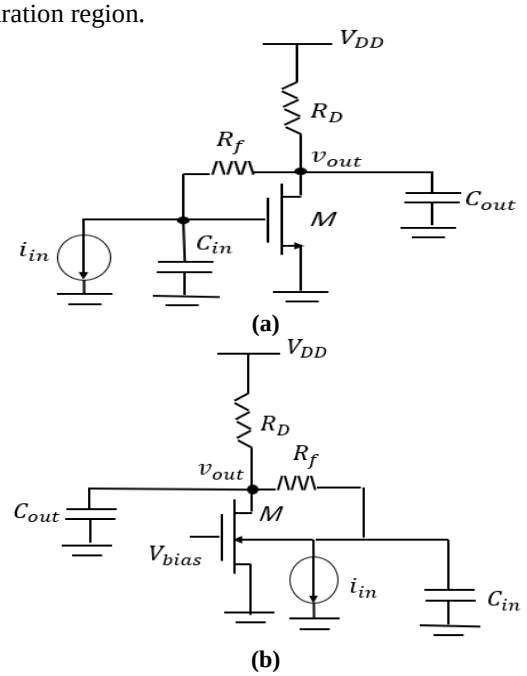


Figure 4: a) The GD common-source with resistive feedback topology. b) The BD common-source with resistive feedback topology.

The gains of the GD and BD common source TIAs with feedback are given by

$$TIA\ Gain_{\ CS,\ GD} = \frac{1 - g_m R_f}{g_m + \frac{1}{R_D // r_o}} \tag{10}$$

$$TIA\ Gain_{\ CS,\ BD} = \frac{1 - g_{mb} R_f}{g_{mb} + \frac{1}{R_D // r_o}} \tag{11}$$

respectively. The input impedances of the GD and BD CS TIAs with feedback are given by

$$Z_{in\ CS,GD} = \frac{1 + \frac{R_f}{R_D // \frac{1}{SC_{out}}}}{g_m + SC_{in} + \frac{1 + SC_{in} R_f}{R_D // \frac{1}{SC_{out}}}} \tag{12}$$

$$Z_{in\ CS,BD} = \frac{1 + \frac{R_f}{R_D // \frac{1}{SC_{out}}}}{g_{mb} + SC_{in} + \frac{1 + SC_{in} R_f}{R_D // \frac{1}{SC_{out}}}} \tag{13}$$

respectively. The output impedances of the GD and BD CS TIAs with feedback are given by

$$Z_{out\ CS,GD} = \frac{1}{\frac{1}{R_f} + \frac{1}{R_D // \frac{1}{SC_{out}}} + \frac{g_m - \frac{1}{R_f}}{1 + R_f SC_{in}}} \tag{14}$$

$$Z_{out\ CS,BD} = \frac{1}{\frac{g_{mb}}{1 + R_f SC_{in}} + \frac{1}{R_D // r_o // \frac{1}{SC_{out}} // (R_f + \frac{1}{SC_{in}})}} \tag{15}$$

respectively. The 3-dB frequencies of the GD and BD CS TIAs with resistive feedback are given by

$$f_{3-dB\ CS,GD} \approx \frac{1}{2\pi\, R_{in}\, [C_{in} + C_{gs} + C_{gd}(1 + g_m (R_D // r_{ds}))]} \tag{16}$$

$$f_{3-dB\ CS,BD} \approx \frac{1}{2\pi\, [(C_{out} + C_{gd}) R_D + (C_{in} + C_{sb})(R_f + (R_D // r_o))]} \tag{17}$$

respectively. In general, the CS based TIA employs a resistive feedback to reduce the input impedance and counteract the impact of the photodiode capacitance on bandwidth [21]. Additionally, the system is inherently stable, as it is a second-order system with only two poles. However, a notable drawback lies in the challenge of achieving a high gain [5].

4.3 The CMOS-Inverter Topology

The CMOS-inverter topology is shown in Figure 5. It consists of M_1, M_2 and R_f which act as a pull-down network, a pull-up network, and a resistive feedback, respectively. In this topology, ensuring impedance matching between the load and the gain stage is crucial for achieving maximum power transfer [22]. The

selection of the aspect ratios, (*W*/*L*), of each transistor must be carefully made in order to prevent any mismatches.

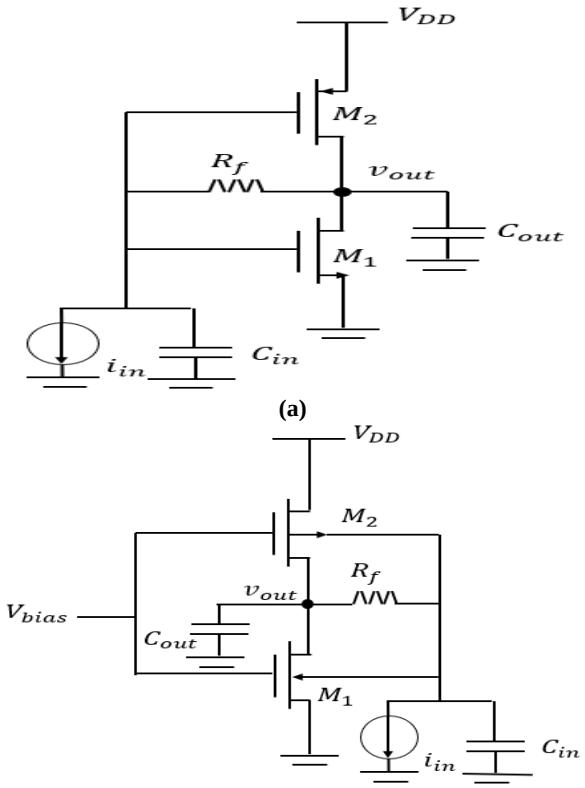


Figure 5: a) The GD CMOS inverter topology. b) The BD CMOS inverter topology.

The gains of the GD and BD CMOS inverter TIAs are given by

$$TIA\ Gain_{CMOS,\ GD} = \frac{1}{g_{m1} + g_{m2}} - R_f \tag{18}$$

$$TIA\ Gain_{CMOS,\ BD} = \frac{1 - (g_{mb1} + g_{mb2})\,R_f}{g_{mb1} + g_{mb2} + \frac{1}{r_{o1}//r_{o2}}} \tag{19}$$

respectively. The input impedances of the GD and BD CMOS inverter TIAs are given by

$$Z_{in\ CMOS,GD} = \frac{1 + SC_{out}R_f}{g_{m1} + g_{m2} + SC_{in} + SC_{out} + R_f S^2 C_{in} C_{out}} \tag{20}$$

$$Z_{in\ CMOS,BD} = \frac{1 + \frac{R_f}{r_{o1}//r_{o2}//\frac{1}{SC_{out}}}}{g_{mb1} + g_{mb2} + SC_{in} + \frac{1 + SC_{in}R_f}{r_{o1}//r_{o2}//\frac{1}{SC_{out}}}} \tag{21}$$

respectively. The output impedances of the GD and BD CMOS inverter TIAs are given by

$$Z_{out\ CMOS,GD} = \frac{1}{\frac{1}{R_f} + SC_{out} + \frac{g_{m1} + g_{m2} - \frac{1}{R_f}}{1 + R_f SC_{in}}} \tag{22}$$

$$Z_{out\ CMOS,BD} = \frac{1}{\frac{g_{mb1} + g_{mb2}}{1 + R_f SC_{in}} + \frac{1}{r_{o1}//\,r_{o2}\,//\frac{1}{SC_{out}}//(R_f + \frac{1}{SC_{in}})}} \tag{23}$$

respectively. The 3-dB frequencies of the GD and BD CMOS inverter TIAs are given by

$$f_{3-dB\ CMOS,GD} \approx \frac{1}{2\pi\left[R_{in}\left(C_{in} + C_{gs1} + C_{gs2}\right) + R_{out}(C_{out} + C_{db1} + C_{db2}) + R_f(C_{gd1} + C_{gd2})\right]} \tag{24}$$

$$f_{3-dB\ CMOS,BD} \approx \frac{1}{2\pi\left[R_{in}(C_{in} + C_{sb1} + C_{sb2}) + R_{out}\left(C_{out} + C_{gd1} + C_{gd2}\right) + R_f(C_{db1} + C_{db2})\right]} \tag{25}$$

respectively. In general, the CMOS inverter-based TIA exhibits the capability of offering a relatively large voltage gain due to adopting both the NMOS and PMOS devices in the amplification process. However, due to connecting the input signal to both the NMOS and PMOS devices, it introduces a significant capacitance at the input node and a large Miller capacitance [5]. This notable capacitance arises from the extensive width of the employed PMOS transistor, which, in turn, occupies a large silicon area. The large capacitances certainly impact the overall bandwidth of the TIA, thus leading to slower response times.

4.4 The Proposed Approach (The Composite-Cascode Topology, CC)

In the GD CC topology, which is shown in Figure 6 (a), the signal source is directly connected to the gates of transistors, M_1 and M_2. The negative-feedback network is formed by the two resistors, R and R_f. This topology outperforms the conventional cascode from the point of view of the power efficiency by providing lower bias currents at the expense of higher Z_{out} [23].

The proposed design employed a BD structure to combine the advantages of both the CC topology and the BD configuration in TIA design. Unlike the GD CC, in the BD CC, shown in Figure 6 (b), the signal source is directly connected to the body terminals of the transistors, M_1 and M_2. The gains of the GD and BD CC TIAs are given by

$$TIA\ Gain_{CC,\ GD} = \frac{(R//R_f)(g_{m2} - \frac{1}{R_f})}{\frac{R\left(\frac{1}{R_f} - g_{m2}\right)}{R + R_f} - \frac{1}{R_f}} \tag{26}$$

$$TIA\ Gain_{CC,\ BD} = \frac{1}{\frac{\frac{1}{R} + \frac{1}{R_f}}{1 + R_f g_{mb1}} - \frac{1}{R_f}} \tag{27}$$

respectively. The input impedances of the GD and BD CC TIAs are given by

$$Z_{in\ CC,GD} = \frac{1}{\frac{1}{R_f} + \frac{1}{R//\frac{1}{SC_{in}}} + \frac{g_{m1} - \frac{1}{R_f}}{1 + R_f SC_{out}}} \quad (28)$$

$$Z_{in\ CC,BD} = \frac{1}{\frac{1}{R_f} + \frac{1}{R//\frac{1}{SC_{in}}} - \frac{\frac{1}{R_f} - g_{mb1}}{1 + R_f SC_{out}}} \quad (29)$$

respectively. The output impedances of the GD and BD CC TIAs are given by

$$Z_{out\ CC,GD} = \frac{1}{\frac{1}{R_f} + SC_{out} + \frac{g_{m1} - \frac{1}{R_f}}{1 - R_f SC_{in}}} \quad (30)$$

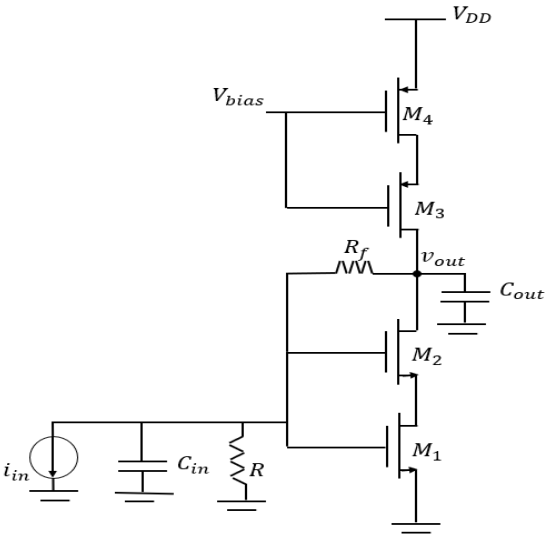
$$Z_{out\ CC,BD} = \frac{1}{SC_{out} + \frac{1 + g_{mb1}(R//\frac{1}{SC_{in}})}{R_f + (R//\frac{1}{SC_{in}})}} \quad (31)$$

respectively. The 3-dB frequencies of GD and BD CC TIAs are given by

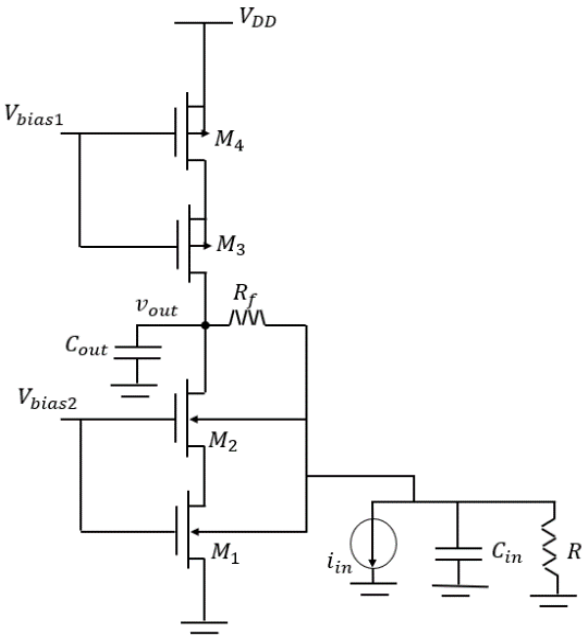
$$f_{3-dB\ CC,GD} \approx \frac{1}{2\pi R_{in}(C_{in} + C_{gs1})} \quad (32)$$

$$f_{3-dB\ CC,BD} \approx \frac{1}{2\pi R_{in} C_{in}} \quad (33)$$

respectively. In general, the CC based TIA offers a high gain. However, it requires a careful design to ensure the stability of the TIA. Despite the design complexity, the cascode devices employed contribute negligible noise. The CC based TIA can be employed in low-voltage applications where power efficiency and voltage constraints are crucial considerations [24].



(a)



(b)

Figure 6: a) The GD composite-cascode topology. b) The BD composite-cascode topology.

5. SIMULATION RESULTS AND DISCUSSIONS

5.1 Simulation Setup

The simulation employed the 130-nm CMOS predictive-technology models with power-supply voltages of 1.2 V and 0.9 V for the GD and BD configurations, respectively. It must be noted that the simulation is performed under different values of V_{DD} for these two configurations. This is because the BD configuration consumes larger power consumption when adopting the same V_{DD} as the GD configuration due to the larger current drawn form the signal applied at the body terminal in contrast to the much smaller current drawn from the signal when applied at the gate terminal in case of the GD configuration.

In the RGC TIA, a load resistance, R_D, of values 200 Ω and 400 Ω was adopted for the GD and BD configurations, respectively. The aspect ratio of the main amplifier was chosen as 20. The CS topology was realized with a load resistance, R_D, of values 100 Ω and 4 kΩ for the GD and BD configurations, respectively. The aspect ratio is taken equal to 0.5 and the feedback resistance was fixed at 10 Ω. For the CMOS inverter with resistive feedback, the aspect ratios of 25 and 7 were adopted for the GD and BD configurations, respectively. The feedback resistance was established at 10 Ω. For the GD composite-cascode topology, the aspect ratios of 15 and 0.7 were adopted for M_1 and M_2, respectively. The resistances, R and R_f, were chosen equal to 11 kΩ and 10 Ω, respectively. Finally, for the BD composite-cascode topology, the aspect ratios of 12 and 1 were chosen for M_1 and M_2, respectively. The

resistances, R and R_f, were chosen equal to 30 kΩ and 10 Ω, respectively.

The TIA gain, 3-dB bandwidth, input/output impedance, noise, distortion, and power dissipation are all evaluated for each topology. To enable a meaningful comparison between the proposed TIA topology and other topologies, the following figure of merit, *FoM*, is proposed and adopted here:

$$FoM = \frac{TIA\ Gain\ (dB\Omega) * 3 - dB\ Bandwidth\ (MHz)}{Area\ (\mu m^2) * P_{diss}\ (mW) * Input - referred\ noise\ \left(\frac{pA}{\sqrt{Hz}}\right) * V_{DD}\ (V)} \quad (34)$$

In order to obtain a fair comparison, the power-supply voltage was included in the defined *FoM* due to the adoption of different power supplies in the simulation of the two configurations. Table 1 presents an overview of the performance metrics of the adopted TIA topologies along with various topologies from previous work. The evaluation of each topology is made by Kiviat graph in which the various performance metrics are evaluated and plotted, each one across a certain axis. According to the performed comparison, there are eight performance metrics. Thus, each axis is separated from its two neighboring ones by an angle of 360°/8 = 45° and vice versa. The value corresponding to the best performance is plotted as far as possible from the origin. For example, Z_{in} of the TIA is preferred to be as small as possible while the 3-dB bandwidth is preferred to be as large as possible. So, the first metric is plotted in Kiviat graph with small values far away from the origin while the second metric is plotted in Kiviat graph with small values close to the origin. Since the shaded area in Kiviat graph is associated with the distances of each metric, the larger the area shaded in Kiviat graph, the better the topology.

Table 1. Comparison of TIA topologies and other works.

	Technology	**Supply voltage [V]**	**Gain [dBΩ]**	**3-dB BW [MHz]**	**Z_{in} [Ω]**	**Z_{out} [Ω]**	**Input-referred noise current [pA/√Hz]**	**THD** [%]**	**Power Consumption [mW]**	**Area [μm²]**	***FoM***
[4]	65 nm	1.2	73	550	NA*	NA*	3.4	NA*	4.8	970	2.113549
[25]	130 nm	1.8	76.8	1000	NA*	NA*	NA*	NA*	47.3	23100	NA*
[26]	130 nm	1.2	104.8	50	NA*	NA*	2.2	NA*	0.34	1200	3.2432
[27]	180 nm	1.8	101.9	91	NA*	NA*	4.4	NA*	0.151	NA*	NA*
[2]	180 nm	1.8	100	9.6	NA*	NA*	8.52	NA*	0.0936	NA*	NA*
[28]	65 nm	1	42	1000	NA*	NA*	33	NA*	0.315	NA*	NA*
GD CS	130 nm	1.2	39.8	762	108	0.2	13	0.0005	0.112	24	723.24
BD CS	130 nm	0.9	55.5	127	598	8.47	2.5	9.97	0.056	22.05	3203.65
GB RGC	130 nm	1.2	42.96	404	192	55.5	14	0.034	1.14	105.3	8.6
BD RGC	130 nm	0.9	48.3	255	243	118	11	0.0011	0.51	104.8	23.28
GD CMOS inverter	130 nm	1.2	36.39	425	76	9.7	16	0.028	1.8	820	0.5457
BD CMOS inverter	130 nm	0.9	55.4	102	598	6.8	7.38	3.2	0.287	234	12.668
GD CC	130 nm	1.2	73.1	12.9	4560	9.5	2.76	2.5678	0.097	522.4	5.61858
BD CC	130 nm	0.9	84.4	4.2	16650	9	2.2	6.852	0.023	436	17.853

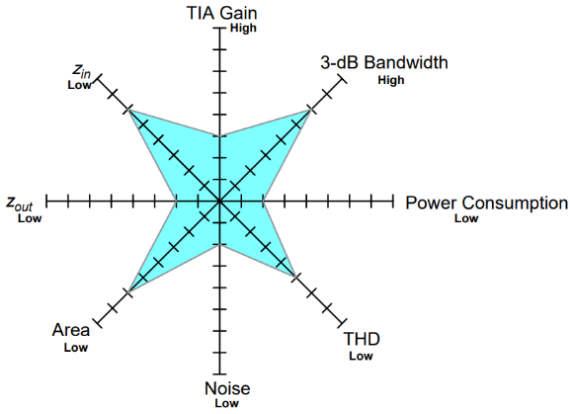
* NA refers to not available.

** THD refers to total harmonic distortion.

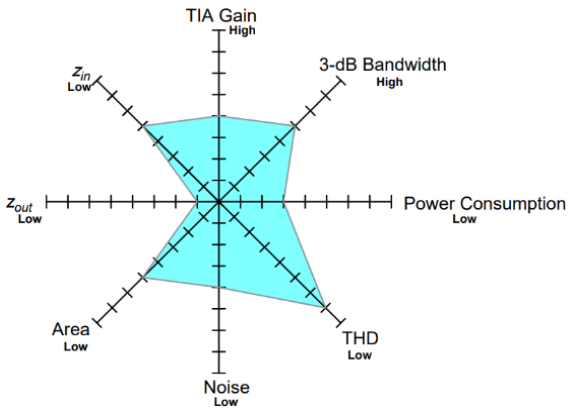
5.2 The Regulated-Cascode Topology, RGC

In the GD configuration, the RGC demonstrated remarkable performance characteristics as the circuit meets the requirements of applications demanding moderate-frequency operation and moderate-speed data transmission. However, it is important to note that the GD configuration requires a remarkable power dissipation.

In the BD configuration, on the other hand, the RGC showcased its suitability for biomedical applications. The circuit demonstrated lower power consumption compared to that of the GD configuration. Furthermore, it exhibited lower THD (as shown in Figure 7) that is crucial in biomedical applications where precise and reliable signal amplification are both required.



(a)



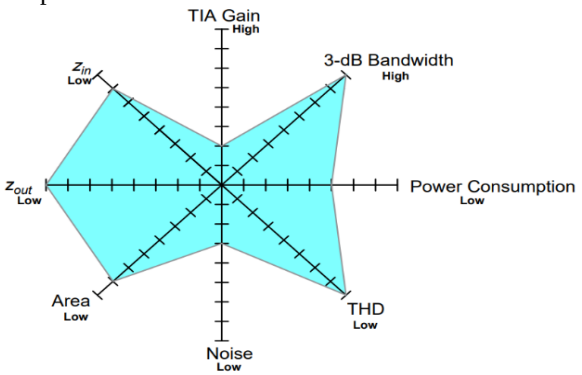
(b)

Figure 7: a) Kiviat graph of the GD RGC topology. b) Kiviat graph of the BD RGC topology.

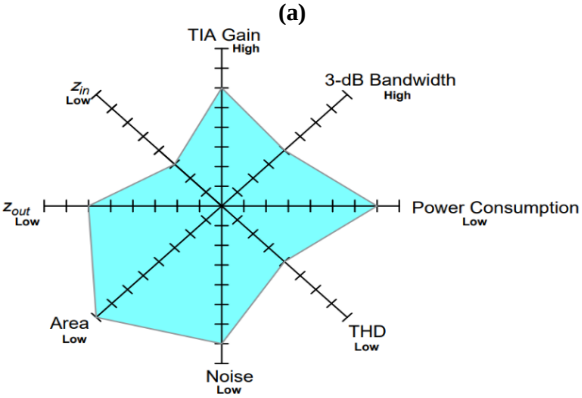
5.2 The Common-Source Topology, CS

As shown in Figure 8, the GD configuration exhibits competitive performance in terms of bandwidth (BW), total harmonic distortion (*THD*), and Z_{out}. This makes it particularly well-suited for fiber optic applications where high-speed signal processing and high-speed data transmission are paramount. However, it may have certain limitations in terms of gain, input-referred noise current, and power consumption.

The BD configuration outperforms in terms of area, power dissipation, making it highly suitable for portable devices. Its size and lower power consumption make it an excellent choice for applications where size and power constraints are critical.



(a)

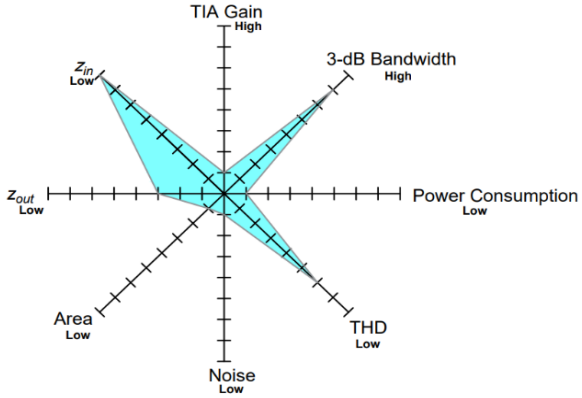


(b)

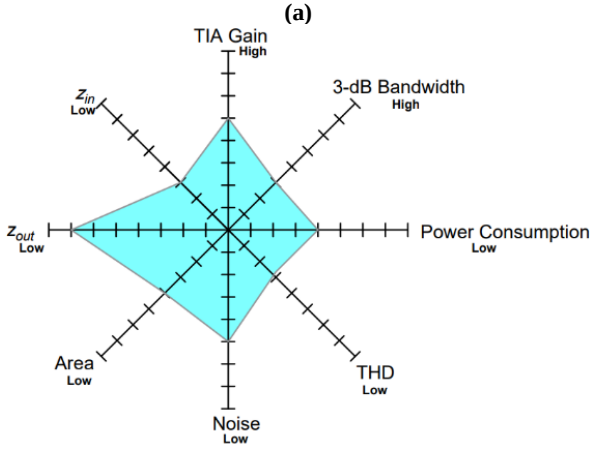
Figure 8: a) Kiviat graph of the GD CS with resistive feedback topology. b) Kiviat graph of the BD CS with resistive feedback topology.

5.3 The CMOS-Inverter Topology

The GD configuration exhibits higher BW, lower gain, higher power consumption, and occupies a larger area compared to the BD configuration (refer to Figure 9). The higher gain achieved with the BD configuration is in contrast to what is mentioned in Section 3 as g_{mb} is smaller than g_m. However, it must be noted that the adopted power supply is different for the GD and BD configurations. The GD configuration outperforms the BD one in terms of Z_{in}. It could still be suitable for certain applications where the need of moderate BW is required; however, this comes at the expense of lower gain, larger area, and larger power consumption. In contrast, the BD configuration excels in terms of Z_{out}, so a higher voltage can be delivered to the load by minimizing the voltage drop across Z_{out}.



(a)

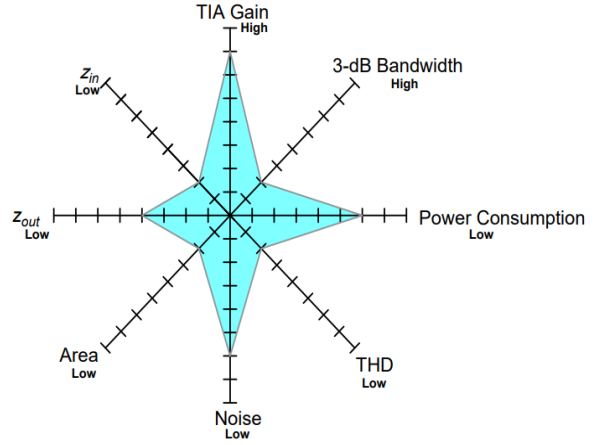


(b)

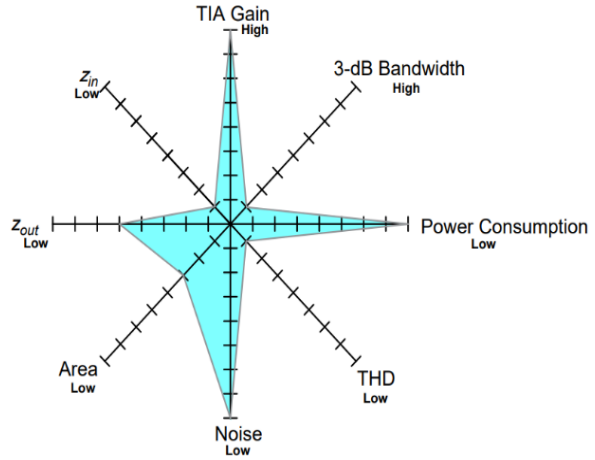
Figure 9: a) Kiviat graph of the GD CMOS inverter topology. b) Kiviat graph of the BD CMOS inverter topology.

5.4 The Composite-Cascode Topology, CC

The GD and BD configurations of the CC topology excels in terms of gain, power efficiency, and noise performance (Figure 10). Given its strengths, the two configurations are well-suited for biomedical applications as these types of applications require precise and low-noise signal amplification.



(a)



(b)

Figure 10: a) Kiviat graph of the GD composite-cascode topology. b) Kiviat graph of the BD composite-cascode topology.

6. IMPACT OF TECHNOLOGY SCALING

In this section, the impact of technology scaling on the performance of the GD and BD configurations is investigated.

6.1 The Velocity-Saturation and the Mobility-Degradation Effects

Due to the reduction of the channel length with technology scaling, the horizontal electric field applied across the channel increases, thus degrading the mobility of the charge carriers. The result is that the velocity of the free electrons saturates and is no longer dependent on the applied electric field [29]. The effect of velocity saturation on the current-voltage relationship in the saturation region is that it becomes linear. On the other hand, the mobility-degradation effect is due to the degradation of the mobility of the charge carriers due to the increase of the electric field in the vertical direction across the gate oxide [29].

In fact, the mobility-degradation effect becomes more perceptible with technology scaling due to the reduction of the gate-oxide thickness. Reducing the gate-oxide thickness was done in order to mitigate the short-channel effects [30]. These two effects certainly reduce the current-driving capability of the transistors and also result in a degraded gate transconductance. Thus, the gain of the GD configuration is expected to decrease with technology scaling compared to the BD one.

The reduction of g_m results in an increase in the input resistance of the GD configuration which is related to the inverse of g_m.

6.2 Reduction of the Early Voltage

The reduction of the channel length with technology scaling causes the Early voltage, V_A, to decrease. Thus, the effect of r_o will be more significant with technology scaling. The result is that the intrinsic gain, $g_m r_o$, decreases.

6.3 Reduction of the V_{DD}/V_{thn} Ratio

This effect is due to the fact that V_{DD} decreases with technology scaling in order to reduce the power consumption and reduce the probability of oxide breakdown [31], [32], [33]. Also, V_{thn} decreases with technology scaling in order not to degrade the speed [34], [35]. However, the rate of the reduction of the power-supply voltage is faster than that of V_{thn} [36], [37], [38], [39]. So, the ratio, V_{DD}/V_{thn} degrades with technology scaling. Thus, the portion of the dc power supply, that is required to turn on the transistor and achieves a considerable transistor action in accordance with the conventional GD configuration, increases. This seems to be a relative advantage for the BD configuration.

6.4 Reduction of the Body Effect

Returning to Eq. (2) for the body-effect parameter, it must be noted that N_A increases with technology scaling in order to reduce the depletion-region thickness and C_{ox} increases due to the reduction of the gate-oxide thickness. Both N_A and C_{ox} increase by the same rate. So, γ decreases with technology scaling. Thus, g_{mb} and accordingly the gain of the body-driven configuration decreases with technology scaling.

6.5 Reduction of the Internal Capacitances

Since the values of the internal capacitances are proportional to the device dimensions [40], the internal capacitances certainly decrease with technology scaling. This indicates an increase in the bandwidth of both the GD and BD configurations. However, the number of metal layers of the interconnections increases with technology scaling [30], thus acting to counterbalance the previous effect on the bandwidth. However, since the fan-out is not large in analog circuits on contrary to the digital ones, the former effect is the dominant one and the bandwidth is expected to increase with technology scaling.

7. CONCLUSIONS

In this paper, four topologies of the transimpedance amplifier are simulated and compared, each realized using the gate-driven and the body-driven configurations. The choice between the GD and BD configurations for each topology depends on the specific performance requirements and constraints of the application. The BD configuration is chosen for low-power, low-noise, and high-gain applications while the GD configuration might be preferred for higher bandwidth requirements. Understanding the trade-offs of each configuration is essential for selecting the most appropriate topology for a given application. Finally, the effects of CMOS technology scaling on the performance of the GD and BD configurations were investigated in a qualitative manner.

8. FUTURE WORK

In this section, two points are presented as suggestions for future work:

1. First, the work performed in this paper can be extended to include operating the devices in the subthreshold region. This region is suitable for biomedical applications or other applications that require very low power but does not require high speed. Also, the various levels of inversion including moderate and weak inversions can be adopted.
2. Second, the sizes of the transistors and the resistance values adopted in this paper are not optimum in that they do not correspond to the optimum performance of the adopted topologies. The reader is encouraged to seek optimum values for the adopted components. This can be achieved either by evaluating the figure of merit or evaluating the shaded area in Kiviat graph at several values for these parameters, then deciding on the values that correspond to the largest *FoM* or the largest shaded area.

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