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Experimental Validation of the Static and Dynamic Characteristics of a Power MOSFET

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Abstract

Metal Oxide Semiconductor Field Effect Transistor "MOSFET" devices are crucial to all of the modern electronic technology and expected to be for some years to come. The aim of this paper is to experimentally validate the vital characteristics of an N- channel enhancement mode power MOSFET. Static and dynamic characteristics are investigated and graphed alongside extracting the main device static parameters that well-describe the device behavior. These parameters are the threshold voltage, the on-state and output resistances, the early voltage, the channel length modulation parameter and the conduction parameter. The input, output and reverse transfer capacitances are measured as functions of the drain-source voltage. Finally, the switching characteristics are examined with calculating graphically all the controlling on/off-states switching times needed.

Keywords: Dynamic characterization, power MOSFET, physical parameters, static characterization.

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I. Introduction

Almost four decades and yet, the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has been the backbone of all modern electronic technology [1]. This is attributed to the significant performance characteristics; high switching speed [2], high input impedance [3] and high operating frequencies [4]. A major branch category of the MOSFET family is the power MOSFET which acts as the corner stone in many advanced high power applications. With positive temperature coefficient on-resistance [5], great capability of working in parallel [2], power MOSFETs excel at driving high current loads. This can be done with extremely small controlling currents compared to other power transistor [4]. Under heavy duty conditions, malfunctioning driving circuits can cause serious high-cost equipment damages. Good circuit design requires accurate device modeling and simulation [6]. These procedures bank on full knowledge of device parameters which can be obtained from datasheets or experimentally for precise parameter designation. Many papers, over the years, have been made to calibrate, compare and illustrate characteristic curves for several MOSFETs validating relevant data for successful circuit designs [6]–[18]. The purpose of this paper is to experimentally validate static and dynamic characteristics of a power MOSFET and to extract its physical parameters affecting its behavior.

II. Device and experimental setup

Fig (1) shows the DUT power MOSFET IRF630. This device is an N- channel enhancement mode power MOSFET manufactured by STMicroelectronics with a To-220 package. The three leads, G, D and S are the gate, drain and source respectively.

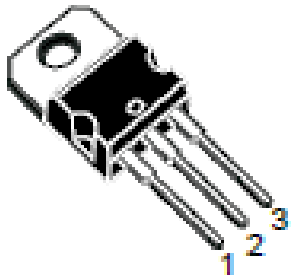

Fig (1): IRF630 power MOSFET

A. *Measuring setup for device static characteristics*

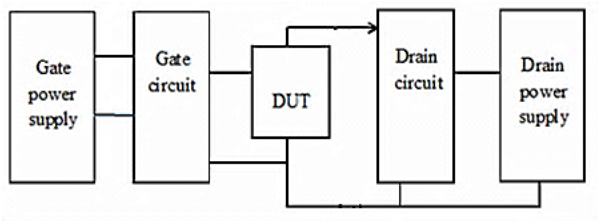

Fig (2): Measuring setup for device static characteristics.

Fig (2) shows the general block diagram for the system that has been used to determine the DC characterization of MOSFET device under test "DUT". Static characterization

includes the measurement of device output characteristics (I_D versus V_{DS}) and transfer characteristics (I_D versus V_{GS}). The static physical parameters of the power MOSFET are extracted from the measured data which is analyzed and plotted using MATLAB.

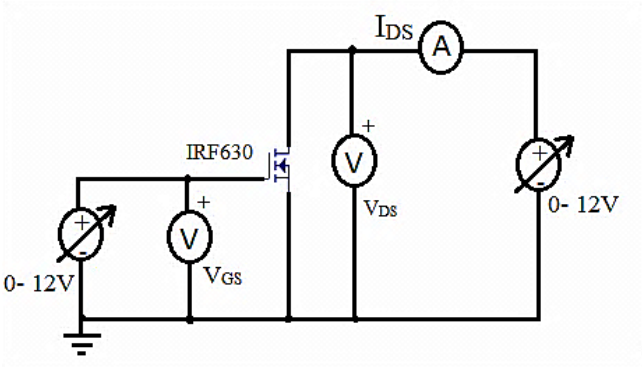

Fig (3): Circuit for static measurements.

The electric circuit corresponding to the block diagram (Fig (2)) is shown in Fig (3). In this circuit the drain of the DUT is connected to a variable voltage source ranging from 0V to 12V. The gate is connected to another voltage source with the same range (0- 12V).

B. Measuring setup for device dynamic characteristics

1) Device Capacitance setup

Capacitance vs. Voltage (C-V) measurement setups, shown in Fig (4), (5) and (6) are used to measure the required capacitances of the test device under consideration. These capacitances are the input capacitance (C_{iss}), the output capacitance (C_{oss}) and the reverse transfer capacitance (C_{rss}) respectively. All measurements are achieved using U2826 LCR Meter at frequency of 1.5 MHz with a variable bias voltage applied to the drain using a variable voltage source ranging from 0 to 26 V. The data is analyzed and plotted using MATLAB.

The input capacitance C_{iss} measurement:

The measurement circuit of C_{iss} is shown in Fig (4), where gate of the device is connected to the "High" terminal of the LCR meter while the source is connected to the "Low" terminal. An AC short capacitor is connected between the drain and the source of the device when measuring C_{iss}.

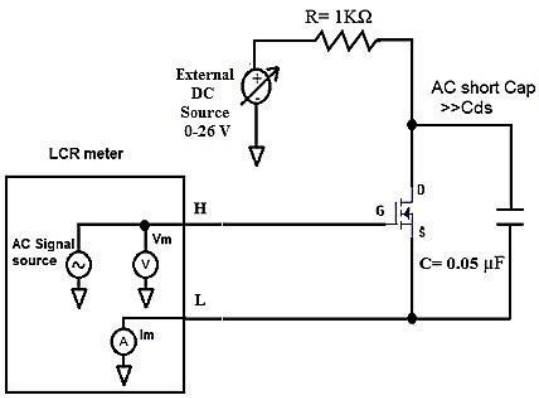

Fig (4): The measurement circuit for C_{iss}.

The output capacitance C_{oss} measurement:

Fig (5) shows the measurement circuit for C_{oss} of the DUT where the drain is connected to the "High" terminal of the LCR through the blocking capacitor. The gate and the source are shorted and connected to the "Low" terminal of the LCR. A blocking capacitor is necessary to superimpose the measurement AC signal on the voltage bias source. In addition, a resistor is needed at the output of the external DC source to avoid leakage of the measurement AC signal.

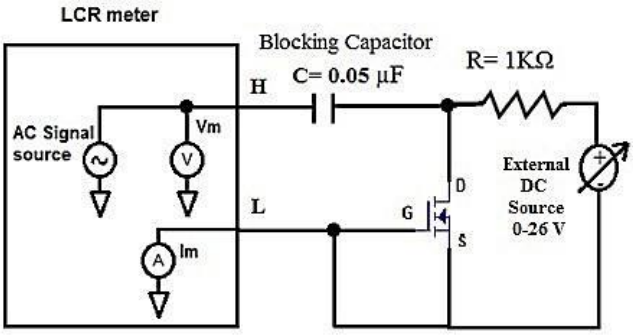

Fig (5): The measurement circuit for C_{oss}

The reverse transfer capacitance C_{rss}:

As shown in Fig (6), the drain terminal is connected to the "High" terminal of the LCR through the blocking capacitor, while the gate is connected to the "Low" terminal. The source is connected to the AC guard of the LCR.

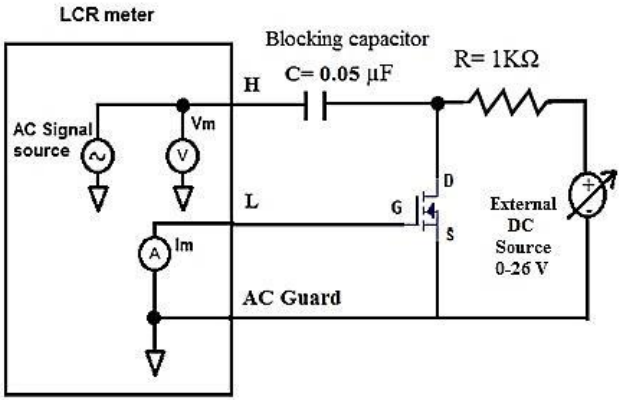

Fig (6): The measurement circuit for C_{rss}

2) Switching setup

Switching circuit, shown in Fig (7), is used for measuring switching characteristics to study the dynamic behavior of switching device. A function generator is used to apply an input signal to the gate through the gate resistance RG at two frequencies, 10KHz and 20KHz. A DC bias source is also used at the drain through a load resistance RL = 1 KΩ as shown in Fig (7). A Signal Oscilloscope is used for measuring the input and output signals on the device. Switching

measurements are taken at two different values of the gate resistance, 0 and 1 KΩ.

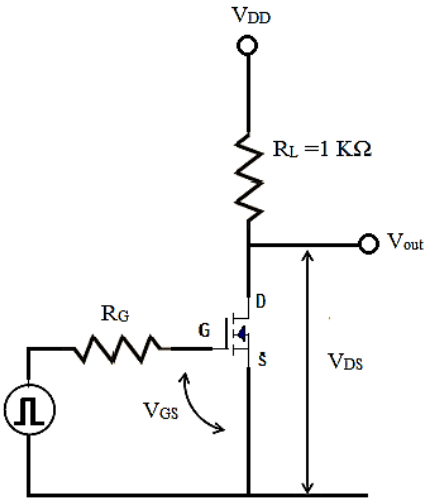

Fig (7): Switching test circuit.

III. Results and discussion

This section is divided mainly into three parts: the first part is for exploring the static characteristics of the power MOSFET device including the output and the transfer characteristic at different values of the gate voltages V_{GS} and drain voltages V_{DS} respectively. The second part is to extract the physical parameters related to the static characteristics defining the power MOSFET from the DC measurements. The third part is for exploring the dynamic characteristics of the device including the three capacitances and switching characteristics.

C. The output characteristics

The measured output characteristics of the power MOSFET at room temperature is shown in Fig (8). The drain current I_{DS} is measured as a function of drain voltage V_{DS} at different values of the gate voltage V_{GS}, 4, 4.1, 4.2, 4.4, 4.6, 4.8, 5 V and the dash line is the maximum slope of the linear region.

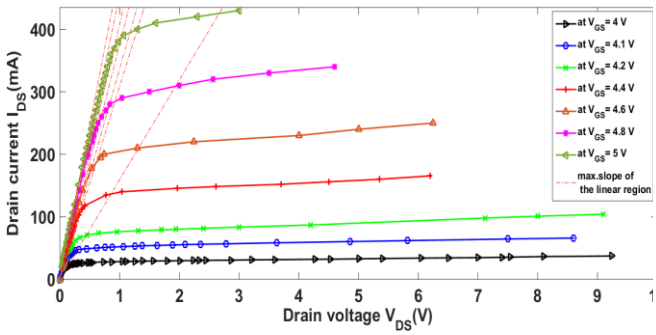

Fig (8): Output characteristics I_{DS} versus V_{DS} for different V_{DS} in saturation region

The I_{DS} – V_{DS} curves exhibit the typical behavior well-known for such devices. The drain current increases linearly for small drain voltage V_{DS} (from 0 V to 0.2V for V_{GS} = 4 V up to 0.9 V for V_{GS} = 5 V) then saturates at the saturation region with values of 25 mA up to 400 mA for V_{GS} = 4 and 5 V respectively).

D. The Transfer Characteristics

The transfer characteristic curves illustrate the variation of drain current I_{DS} with gate voltage V_{GS} at different values of V_{DS} at linear and saturation regions.

Transfer Characteristics in the Linear Region

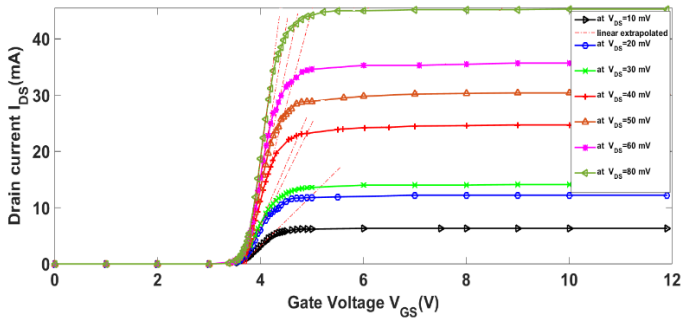

Fig (9): Transfer characteristics of the device for V_{DS} in the linear region.

Fig (9) shows the transfer characteristics in the linear region for values of V_{DS} ranging from 10 mV to 80 mV. The drain current is zero for Gate voltage less than ~ 3.3 V for all values of V_{DS}. For higher values of drain-source voltage, the current increases till a saturation value ranging from about 6.5 mA to 45 mA for V_{DS} = 10 and 80 mA respectively.

Transfer Characteristics at Saturation region

The transfer characteristics curves for the saturation region are shown in Fig (10). The data shown is for measured drain current versus gate voltage for three selected values of the drain-source voltage V_{DS} =2V, 3V and 3.5V. It is clear that I_{DS} = 0 for V_{GS} less than 3.5 V for all V_{DS} values. While for values higher than 4.25 V, the current increases linearly in the region preceding saturation zone for V_{GS} larger than 5 V.

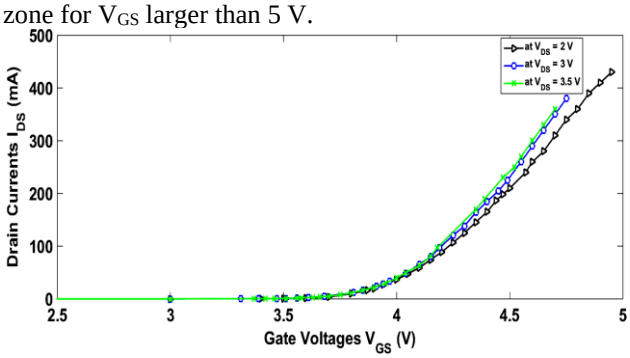

Fig (10): Transfer characteristics of the device at different V_{DS} in saturation region.

E. Parameters extraction of power MOSFET

Threshold Voltage V_{TH}

The threshold voltage of the MOSFET is one of the fundamental parameters in simulation and testing necessary in circuit designs. It is defined as the gate voltage at which an inversion layer (a conductive channel) at the interface between the insulating layer (oxide) and the substrate (body) of the transistor is formed and represents the onset of significant drain current flow between the source and drain terminals [17]. A typical power MOSFET V_{TH} are 2 to 4 V for high voltage devices with thicker gate oxides and 1 to 2 V for lower voltage devices with thinner gate oxides [19].

Threshold voltage can be extracted graphically through extrapolation in either the linear region or the saturation region.

Extraction of V_{TH} from extrapolation in the linear region method

For the linear region, V_{TH} is the point of interception of the gate- voltage axis with the linear extrapolation of the I_D -V_{GS} curve at its maximum first derivative (slope) as shown in Fig (9) [1]. The extracted V_{TH} from this method is found to be 3.68 ± 0.027 V.

Extraction of V_{TH} from extrapolation in the saturation region method

For the saturation region, V_{TH} is the point of interception of the gate voltage axis with the linear extrapolation of the curve $(I_{D\,sat}^{0.5} - V_G)$ at its maximum first derivative (slope) as shown in Fig (11) [16]. The extracted value is equal to 3.66 ± 0.015 V.

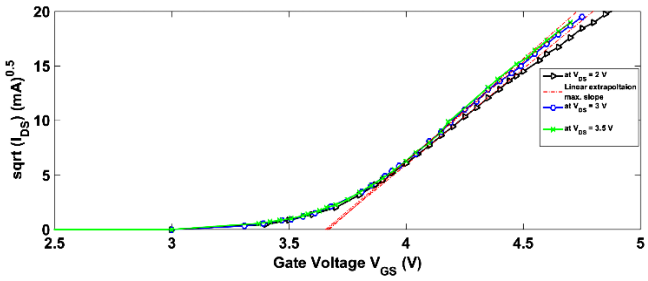

Fig (11): Extraction of V_{TH} from linear extrapolation method in the saturation region from $(I_{DS\,sat}^{0.5} - V_{GS})$ characteristics at different V_{DS}.

On-state Resistance $R_{(ON)}$

Another important parameter of MOSFET devices is the on-resistance which limits the current that can be conducted by the device before it is damaged by the heat. $R_{(ON)}$ for a power MOSFET structure is defined as the total resistance to current flow between the drain and source electrodes when a gate bias is applied to turn on the device [20].

$R_{(ON)}$ is extracted from the tangent drawn at the linear region of the drain current in the output characteristics. The value of $R_{(ON)}$ determined experimentally from the inverse maximum slope of the linear region of I_{DS} versus V_{DS} characteristics as shown in Fig (9). The value of $R_{(ON)}$ is obtained experimentally to be 2.025 Ω at gate voltage of 5 V.

Extracted values of $R_{(ON)}$ for different values of V_{GS} obtained from the output characteristics show that the $R_{(ON)}$ decreases with increasing the gate voltage V_{GS} as shown in Fig (12).

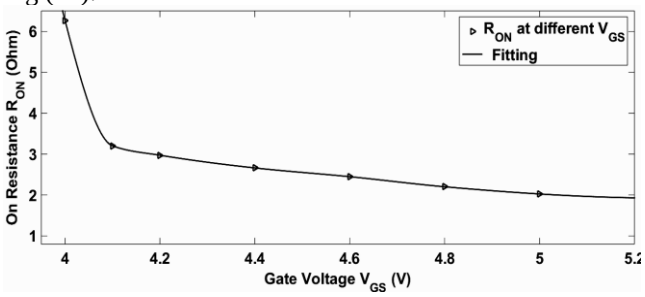

Fig (12): $R_{(ON)}$ for different values of V_{GS}.

Early Voltage V_A (-1/λ)

In most cases the I_{DS} - V_{DS} characteristics of the device in saturation can be approximated by linear saturation behavior characteristics at different V_{GS} values converging to I_{DS} = 0 at common voltage V_A known as early voltage. This value is the intersection of the axis of the drain voltage with the extended tangents of the linear curves as shown in Fig (13). Early voltage for the DUT is found to be -26.54 V yielding channel length modulation parameter λ of a value of 0.038 V^{-1}.

The Output Resistance r_o

The output resistance, as the reciprocal of the slope of the output characteristic curve in saturation region, is shown versus the gate voltage V_{GS} in Fig (14). The experimental values are displayed alongside the estimated ones emphasizing a good agreement over most of the range. The minor differences are owed to possible experimental uncertainties.

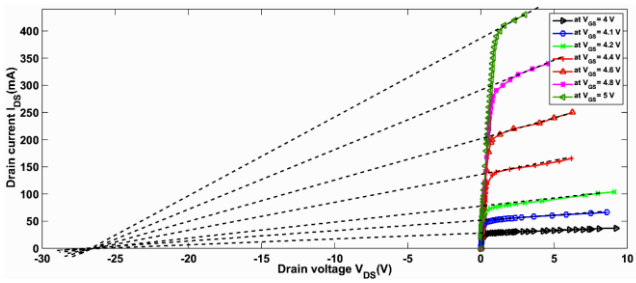

Fig (13): Channel length modulation parameter extraction from an I_{DS}-V_{DS} characteristics curve.

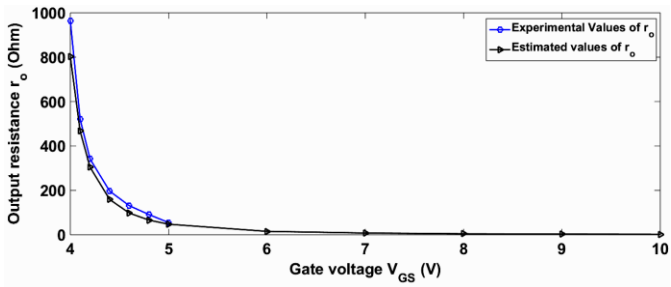

Fig (14): Output resistance r_o versus gate voltage V_{GS}.

Conduction Parameter K_n

The conduction parameter K_n for the n-channel MOSFET is a constant that depends on the device geometry. The value of $\sqrt{K_n}$ parameter is extracted experimentally from the slope of $\sqrt{I_D}$ versus V_{GS} curve in the saturation region as shown in Fig (11). The extracted value of K_n is 320 mA/V^2.

F. Capacitance measurements

As mentioned before, the three device capacitances in power MOSFET that are of major interest are the input capacitances (C_{iss}), the output capacitance (C_{oss}) and the reverse transfer capacitance (C_{rss}). All of these are to be measured for specified testing conditions.

The device capacitances are not constant and change with the voltage applied between the terminals [21]. These capacitances are independent of temperature, so MOSFET switching speed is also insensitive to temperature [7].

The input capacitance is measured between the gate and source terminals with the drain shorted to the source for AC signals. C_{iss} is made up of the gate to drain capacitance C_{gd} in parallel with the gate to source capacitance C_{gs}.

$$C_{iss} = C_{gs} + C_{gd} \quad (1)$$

The output capacitance is measured between the drain and source terminals with the gate shorted to the source for AC voltages. C_{oss} is made up of the drain to source capacitance C_{ds} in parallel with the gate to drain capacitance C_{gd}, or

$$C_{oss} = C_{ds} + C_{gd} \quad (2)$$

The reverse transfer capacitance is measured between the drain and gate terminals with the source connected to ground. The reverse transfer capacitance is equal to the gate to drain capacitance.

$$C_{rss} = C_{gd} \quad (3)$$

The input capacitance is measured between the gate and source terminals with the drain shorted to the source for AC signals. C_{iss} is made up of the gate to drain capacitance C_{gd} in parallel with the gate to source capacitance C_{gs}.

$$C_{iss} = C_{gs} + C_{gd} \quad (1)$$

The output capacitance is measured between the drain and source terminals with the gate shorted to the source for AC voltages. C_{oss} is made up of the drain to source capacitance C_{ds} in parallel with the gate to drain capacitance C_{gd}, or

$$C_{oss} = C_{ds} + C_{gd} \quad (2)$$

The reverse transfer capacitance is measured between the drain and gate terminals with the source connected to ground. The reverse transfer capacitance is equal to the gate to drain capacitance.

$$C_{rss} = C_{gd} \quad (3)$$

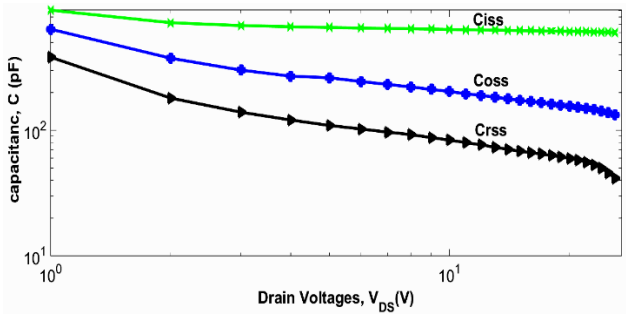

Fig (15): Capacitance versus Voltage.

Fig (11) shows all the three capacitances values versus drain-source voltage. C_{iss} has a value of 905.7 pF at drain source voltage V_{DS} of value of 1 V and reaches 599.7pF at V_{DS} = 26 V while C_{oss} has a value of 639.5 pF at V_{DS} = 1V and reaches a value of 133 pF at V_{DS} = 26 V and finally C_{rss} has a value of 382.7 pF at V_{DS} = 1V and reaches a value of 41.4 pF at V_{DS} = 26 V.

The capacitances decrease over a range of increasing drain source voltage. The considerable decrease in value is noticed for the C_{rss} capacitor which is the smallest of the three along the whole range while the highest capacitance, C_{iss} decreases over the whole range to a much smaller extent.

A. Switching characteristics

The switching characteristics of the devices is observed for two frequency 10 KHz and 20 KHz at two different gate series resistance R_G = 0 Ω and 1KΩ. The on-state and off-state waveforms for the two frequencies and the two gate resistances are shown in Fig (16-19). The times taken to turn the device on and off are to be calculated from input and output waveforms.

From the on-state waveform of the device, the turn-on delay time $t_{d\,(on)}$ is calculated as the time taken from when the gate-source voltage rises over 10% of V_{GS} until the drain-source voltage reaches 90% of V_{DS}, the rise time t_r is the time taken for the drain-source voltage to fall from 90% to 10% of V_{DS}. So, the total turn-on time t_{on} is equal to $t_{d\,(on)}$ + t_r as shown in Fig (16 a).

From the off state wave form of the device, the turn-off delay time $t_{d(off)}$ is calculated as the time from when the gate-source voltage drops below 90% of V_{GS} until the drain-source voltage reaches 10% of V_{DS}, the fall time t_f is calculated as the time taken for the drain-source voltage to rise from 10% to 90% of V_{DS}. So, the total turn-off time t_{off} is equal to $t_{d\,(off)}$ + t_f as shown in Fig (16 b).

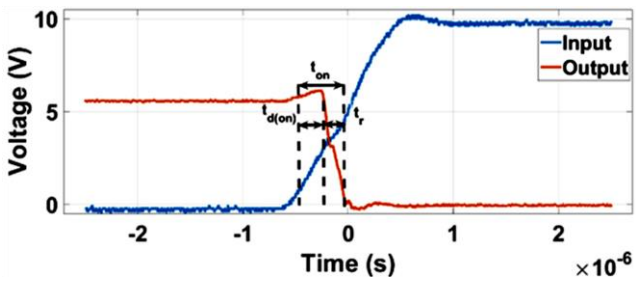

Fig (16): (a) On state waveform of the device at F= 10KHz and R_G = 0Ω.

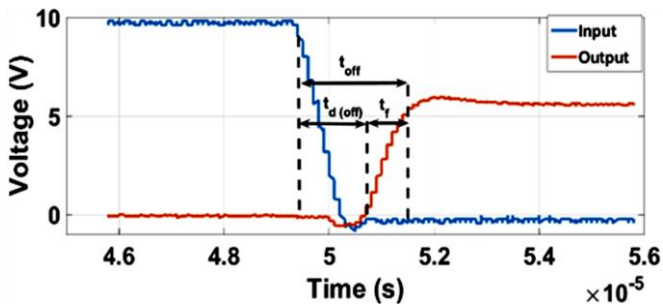

Fig (16): (b) Off state waveform of the device at F= 10KHz and R_G = 0Ω.

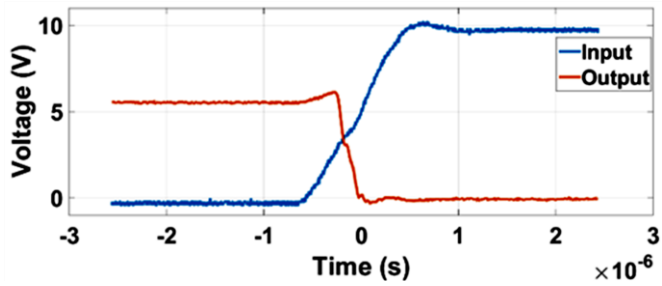

Fig (17): (a) On state waveform of the device at F= 20KHz and R_G = 0Ω.

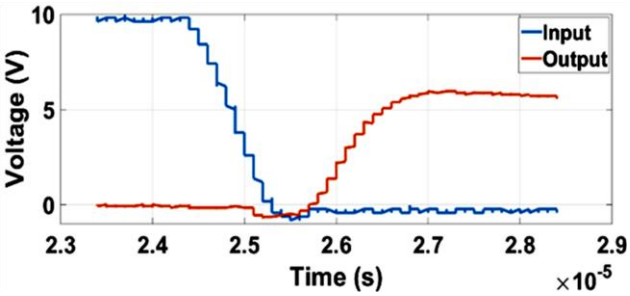

Fig (17): (b) Off state waveform of the device at F= 20KHz and $R_G = 0\Omega$.

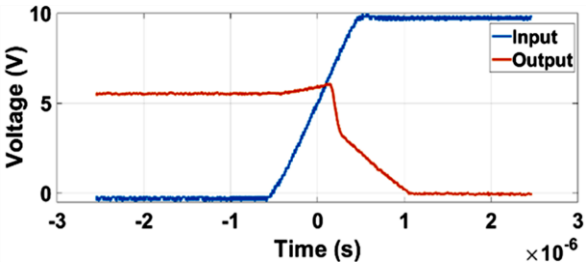

Fig (18): (a) On state waveformof the device at F= 10KHz and $R_G = 1K\Omega$.

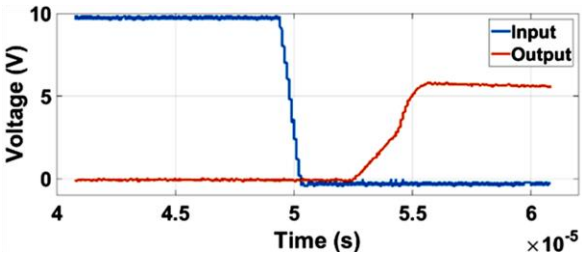

Fig (18): (b) Off state waveform of the device at F= 10KHz and $R_G = 1K\Omega$

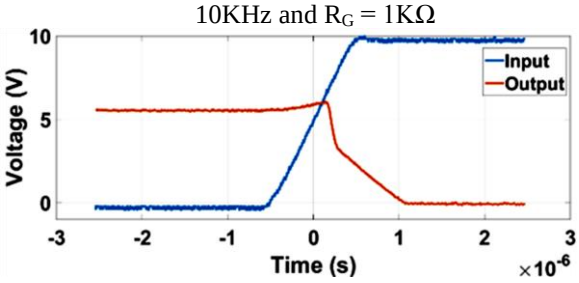

Fig (19): (a) On state waveform of the device at F= 20KHz and $R_G = 1K\Omega$.

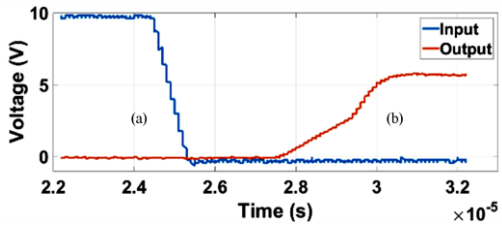

Fig (19): (b) Off state waveform of the device at F= 20KHz and $R_G = 1K\Omega$.

The values of all times calculated from the on and off states for the input and output waveforms of the MOSFET are recorded in Table (1).

TABLE (1)
SWITCHING TIMES FOR ON AND OFF STATE OF THE DEVICE

	$R_G = 0\Omega$ F= 10 KHZ	$R_G = 0\Omega$ F= 20 KHZ	$R_G = 1K\Omega$ F= 10 KHZ	$R_G = 1K\Omega$ F= 20 KHZ
$t_{d(on)}$	0.266 µs	0.267 µs	0.62 µs	0.63 µs
t_r	0.2 µs	0.18 µs	0.733 µs	0.733 µs
t_{on}	0.466 µs	0.447 µs	1.35 µs	1.36 µs
$t_{d(off)}$	1.2 µs	1.17 µs	3.33 µs	3.4 µs
t_f	0.9 µs	0.933 µs	2.15 µs	1.8 µs
t_{off}	2.1 µs	2.1 µs	5.48 µs	5.2 µs

From the results shown in Table (1), the values of the turn on time t_{on} and the turn off time t_{off} increase with increasing the gate resistance from 0Ω to 1KΩ but the increase is less considerable with increasing frequency from 10KHz to 20KHz.

IV. Conclusion

The authors have investigated an N- channel enhancement mode power MOSFET IRF630. The I_{DS}-V_{DS} curves are experimentally demonstrated at different values of the gate voltage followed by the I_{DS}-V_{GS} curves as the transfer characteristics at both the linear and saturation regions. The most important parameters of the DUT are extracted from the graphical data presented. This includes the threshold voltage V_{th} which is found to be equal to 3.67 V, the on-state and output resistances R_{on} and r_o for a range of V_{GS}, the early voltage V_A = -26.54 V, channel length modulation parameter λ = 0.038 V^{-1}, and the conduction parameter K_n = 320 mA/V^2.

The three major DUT capacitances, representing the dynamic characteristics are measured and graphed versus the V_{DS} showing the general expected behavior of these capacitances emphasizing the decrease of their values with increasing drain-source voltage. While for switching characteristics, the on/off-states switching times are calculated from the corresponding waveforms at two different frequencies 10KHz and 20KHz and two different gate series resistance RG = 0 Ω and 1 KΩ. All respective switching timings are tabulated exclusively in Table I

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