SVU-International Journal of Engineering Sciences and Applications (2025) 6(1): 61-68
Print ISSN 2785-9967| Online ISSN 2735-4571
DOI 10.21608/svusrc.2024.337701.1249

A Low Power and Flat Gain CMOS RFPA For UWB Applications Using Complementary Current Reuse Stage

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Abstract A low power, high linearity, and flat gain ultra-wideband radio frequency power amplifier (UWB RFPA) circuit design for 3.1-10.6 GHz is proposed in 0.18 um CMOS process. To achieve linear and flat gain over the whole frequency band, the UWB RFPA is built using two stage circuits. A complementary Current-reused topology is applied to minimize the number of coils and present self-bias with improved power gain for the driver stage in the whole frequency band. In the meantime, each RF transistor's input and output terminals have a feedback network coupled by a resistor and a capacitor in series to enhance the gain flatness throughout the entire frequency range. The simulation results demonstrate that the UWB RFPA achieves the saturation output power of 15 dBm at 7.5 GHz. The UWB RFPA has a flat power gain (||S21||) of 21±0.5dB, output 1-dB compression point of 11±0.5dBm, maximum power-added efficiency (PAE) of 22±2%. The amplifier exhibits input and output reflection coefficients of less than -10dB and -10±3dB, respectively. Additionally, the reverse isolation is approximately -40dB, with a power consumption of 23.4 mW and 47 mW from a 1.8 V supply for driver stage and power stage respectively.

Keywords: Ultra-Wideband (UWB); CMOS Power Amplifier; Feedback Network; Complementary Current-Reused; Power Added Efficiency (PAE); linearity; Self-Bias.

1 Introduction

With the rapid growth of ultra-wideband technology, especially in wireless communication systems, ultra-wideband power amplifiers with wide bandwidth, high efficiency, and low power consumption are highly in demand. The UWB systems are applied between 3.1 GHz to 10.6 GHz; this kind of system requires power amplifiers which must provide a high gain, substantial output power, minimal signal distortion, and less group delay variation over the whole spectrum. Recently, numerous CMOS-based PA designs have been presented addressing specific challenges and optimized differently for different UWB applications. This section will offer an overview of the designs focusing on comparison methodologies and performance metrics.

One of the early CMOS PAs for UWB designed with a distributed amplifier topology, achieved performance covering the frequency range of 3-12.6 GHz: for the first time in this design, low-pass and high-pass transmission lines were combined in order to combine wide bandwidth with high-power output, making the amplifier suitable for full-band UWB transmitters. This PA implemented in 180 nm RF CMOS technology realizes a gain of 10.46 dB, OP1dB over 5.6 dBm within the 3–10 GHz range and return loss below -10 dB with minimal group delay dispersion to enable wideband signal transmission [1]. This early design forms a basis for further improvement concerning bandwidth and efficiency.

Further developments in CMOS PA design have been directed at special applications, such as biomedical systems. Among those is a low-power PA in implantable biomedical UWB applications for a frequency range from 3.0 to 6.2 GHz, proposed using three stages. The first stage is a CG input stage that provides wideband impedance matching, while the second stage is a common-source amplifier with RC feedback, which increases gain, flatness, and linearity. The third stage adopts source-follower for output matching. This PA implemented in 0.18 µm CMOS technology has a gain of

Received: 19 November 2024/ Accepted: 2 December 2024
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11 dB on average with return losses less than -14 dB and dissipates only 13 mW, fitting into low-power biomedical applications [2].

Various other designs fall into the general application category in UWB, where there is a balance among gain, efficiency, and linearity. One recently developed two-stage CMOS PA operates from 3.0 to 7.9 GHz. It uses a cascode topology to improve gain and bandwidth in the input stage, following it with a common-source amplifier to provide maximum output power. It employed source degeneration inductors which improve linearity and stability. This PA has a gain of 18.8 dB while S11 and S22 return losses are -2 dB and -6.6 dB at 4 GHz, respectively. It consumes 30mW of power and hence may be used in UWB systems for various applications [3].

Another important improvement in UWB PA design involves stagger tuning methods to realize gain flatness and efficiency over wide frequency ranges. One such CMOS PA operates from 5.0 to 10.6 GHz that staggers the first stage at approximately 6.5 GHz and the second stage at approximately 9.6 GHz to realize a 14 ±1 dB gain with only a very slight ± 40 ps group delay deviation across the band. A design approach like that has granted stability and efficiency for the UWB application, while PAE is around 10% power consumption at about 20 mW [4].

With this, several developments for improving the gain flatness and linearity have been built upon. In the more recent design in 2016, stagger tuning deployment into a two-stage cascode topology enhances the gain flatness and linearity within frequencies between 3.1 to 10.6 GHz. Utilizing current-reuse topology with resistive shunt feedback, the PA has an excellent gain of 18 ± 0.2 dB in input return loss below -10 dB, variation group delay of ±25 ps. It provides an IIP3 of 2.25 dBm at 7 GHz while consuming only 16 mW of power and is hence very apt for UWB applications [5].

It was targeted for medical use, design of a fully differential CMOS PA that operates between 3 and 5 GHz using one single-stage AB-class topology. The matching of this wideband and the flatness of the power gain are allowed using the bandpass filter network and the implementation of shunt feedback. This design operates at high linearity, with minimum group delay for a gain of 15.5 ± 0.4 dB, return losses lower than -13 dB, and consume only 25.46 mW with 9.13 dBm of output power, which optimized for low-power medical use [6].

Newer designs have pursued high power delivery with conjugated matching using feedback networks. The PA implemented using drain-gate feedback for realizing simultaneous power and conjugate matching. This PA operates between 6 and 9 GHz and can achieve an output power of 7 dBm at peak power with a PAE of 20%, thus showing effective impedance matching for wideband applications [7]. In [8], another UWB PA as part of the same-year article provided with two-stage staggered tuning technique with an inter-stage matching circuit. The amplifier provided a gain of 11.5 ± 0.8 dB with a low variation of group delay and 26% PAE for further optimized efficiency with little distortion of the UWB transmission.

Very recently, a PA for IEEE 802.15.3a UWB applications utilizing current-reuse topology and source inductive degeneration achieves both high efficiency and linearity over a wide frequency range from 3.1 to 10.6 GHz. The designed PA achieves a PAE of 24% and the peak output power of 9.3 dB and is highly suitable for high-efficient UWB systems [9].

This study presents a low-power Complementary UWB CMOS power amplifier with good input and output matching operating from 2.9 to 10.8 GHz frequency range. The amplifier is designed for low-power UWB applications and features high linearity and improved flat gain. Section 2 details the circuit's design description and analysis. Section 3 presents the Simulation Results and Discussion. In section 4, we introduce the conclusion.

2 Circuit Description and Analysis

Herein presented is a low-power and high-linearity ultra-wideband (UWB) radio frequency power amplifier (RFPA) circuit operating in the frequency range of 2.9 ~ 10.8 GHz designed in the 0.18 μm CMOS process. For realizing a flat gain and high linearity over the whole frequency band, a two-stage topology architecture with a driver stage and a power stage is utilized as shown in Fig.1 and Fig. 2. A complementary current-reused topology at the driver stage is adopted to save the count of inductor without degrading the high-power gain throughout the whole bandwidth. This stage exploits both N-MOS and P-MOS transistors in a common-source topology, sharing the same current for efficient operation. The used second stage is CS, providing high output power.

2.1 Complementary Current Reuse Driver Stage

At the driver stage, a complementary current-reuse approach is adopted where the N-MOS (M_1) and P-MOS (M_2) transistors are arranged in a common-source topology. For M_1 and M_2, a single coil is used as the common drain choked inductor to minimize the number of coils, hence shrinking the design area for better efficiency. However, the common drain coil ($L_{D1,2}$)

ensures that this RF output power from the first CS_1 circuit M_1 flows into the second CS_2 circuit M_2 with a minimum loss [10].

The first stage design combines the input capacitance (C_{in}), with the gate inductance (L_{g1}) for matching the N-MOS transistor M_1 to the input RF power for optimum impedance matching. In addition, two feedback networks assigned to M_1 are composed of resistor, capacitor (R_{f1}, C_{f1}) and inductor (L_{s1}). These also enhance stability and impedance matching to ensure 50 ohms impedance matching throughout the whole UWB frequency range. The transistor M_1 is biased using a voltage divider circuit comprising resistors (R_{G1}) and (R_{G2}) with 0.9 V from the supply voltage V_{dd}.

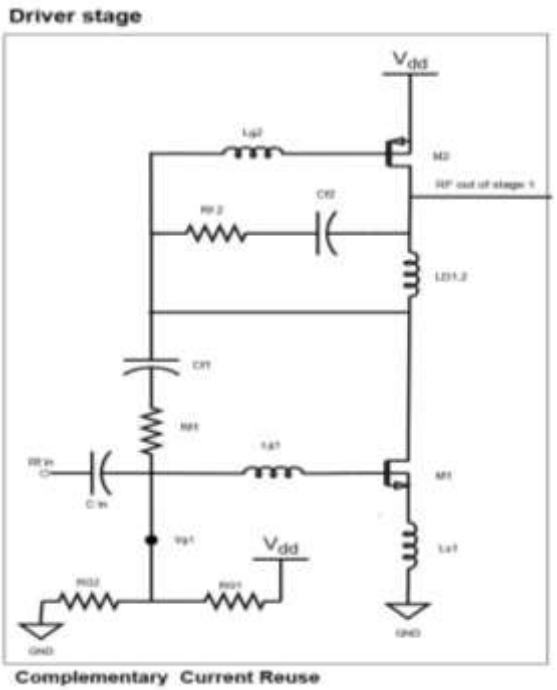


Fig.1 Schematic of the proposed CMOS PA (stage 1).

The second common-source CS_2 of the first stage where the P-MOS transistor M_2 is used, is biased via L_{g2} inductor from the drain of M_1 with 0.73 V. As in the N-MOS transistor stage, M_2 uses resistor and capacitor (R_{f2}, C_{f2}) feedback network that provides further improvement to gain flatness and provides impedance matching over all bandwidth. M_1 and M_2 have a common current of 13 mA with W/L ratio of 112 um / 0.18 um and 192 um / 0.18 um respectively.

2.2 Common Source Power Stage

The power stage employs a third common-source circuit (CS_3), with an N-MOS transistor (M_3) designed to increase the output swing, enhancing output power. The output from the driver stage is connected to M_3 via an inductor (Lg3) with a DC bias voltage of 0.84 V, and a feedback network (R_{f3}, C_{f3}) is used to optimize the matching impedance of the power stage. M_3 has a W / L ratio of 230.4 um / 0.18 um which passes 26 mA current.

The RF output power connected two UWB antenna as a load with 50 ohms impedance in the total bandwidth. This design ensures efficient power delivery, leading to high linearity and improved overall performance in terms of output power.

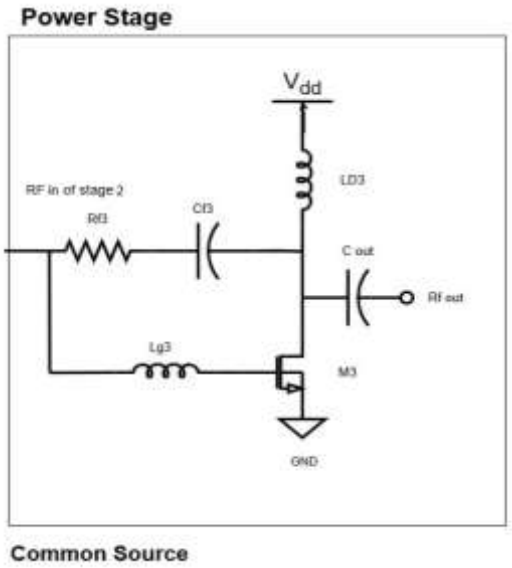


Fig.2 Schematic of the proposed CMOS PA (stage 2).

2.3 Input Impedance Analysis

The design of input matching circuit for UWB operating is very difficult since its matching performance is related to the performance of the whole system. Because of the limited output power density of UWB system, UWB PA is generally operating at the small-signal operation. The small-signal equivalent circuit of two stage UWB RFPA is presented in Fig. 3. The first stage of the proposed power amplifier adopted three feedback networks (L_{s1}), (R_{f1}, C_{f1}) and (R_{f2}, C_{f2}) to cover the whole bandwidth of UWB system, achieving good linearity and stability. The second stage also uses a single feedback network (R_{f3}, C_{f3}) to achieve a good gain flatness throughout the UWB frequency range as shown in Fig. 3 and Fig. 4.

To estimate an approximation for the input impedance,

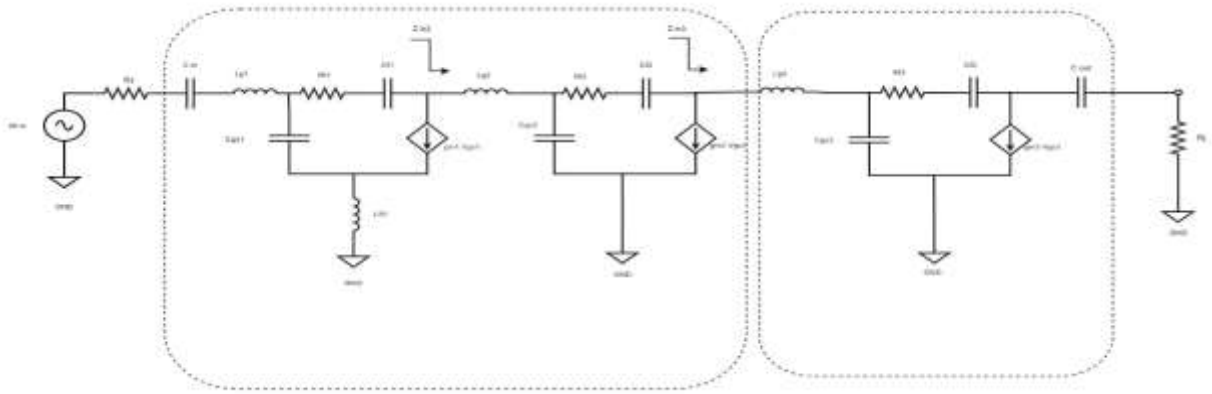


Fig. 3 The small-signal equivalent circuit of Complementary UWB RFPA

the miller theorem is used. The proposed configuration employs a shunt resistive-capacitive feedback technique combined with a conventional design that includes a gate inductor (L_{g1}), and a source degeneration inductor (L_{s1}).

$$Z_{in}(s) = \mathrm{j}\omega L_{g1} + (Z_{f1-Miller} \left|\right| \left(SL_{s1} + \omega_{\tau 1} L_{s1} + \frac{1}{SC_{gs1}}\right)) \quad (1)$$

$$\omega_{\tau 1} = \frac{g_{m1}}{C_{gs1}}$$

$$Z_{f1-Miller} = \frac{Z_{f1}}{1 + A_{v1}}$$

$$Z_{f1} = R_{f1} + \frac{1}{SC_{f1}}$$

Where $\omega\tau 1$ is the current-gain cut-off frequency, g_m and C_{gs} are the transconductances and gate to source capacitances of the transistors and Av_1 is the voltage gain of common source transistor M_1. Based on these equations, the shunt RC feedback and the gate inductor should be selected accurately, as smaller Z_{f1} enhances the input matching largely but decreases the stage gain.

3 Simulation Results and Discussion

The proposed UWB RFPA was designed and simulated in cadence virtuoso software using a TSMC 0.18 µm 1P-6M CMOS process, focusing on delivering high linearity, flat gain, and efficient power operation across the UWB range. The CMOS amplifier consumes 23.4 mW and 47 mW from a 1.8 V supply for driver stage and power stage respectively, which is an efficient power consumption profile for an amplifier operating across such a wide frequency band. This low-power consumption makes the design particularly suitable for portable or battery-operated devices that require energy-efficient operation without sacrificing performance.

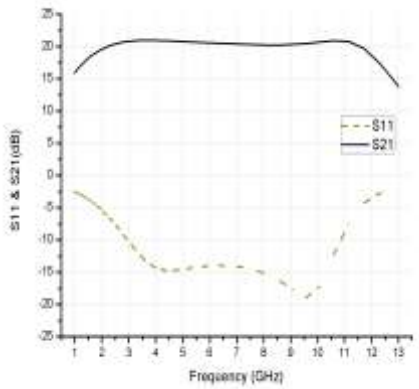


Fig. 4 Simulated $|S_{11}|$ and $|S_{21}|$ of the proposed Complementary UWB RFPA

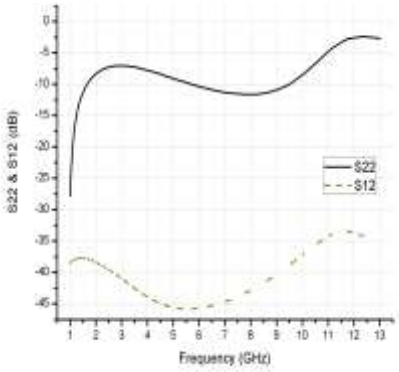


Fig. 5 Simulated $|S_{22}|$ and $|S_{12}|$ of the proposed Complementary UWB RFPA

3.1 S-Parameter Performance

The simulated S-Parameters Response is presented in Fig. 4 and Fig. 5. The amplifier achieves an input reflection coefficient ($|S_{11}|$) below -10 dB from 2.9 GHz to 10.8 GHz as shown in Fig. 4, this low reflection coefficient ensures efficient power transfer from the input RF generator to the amplifier and minimal signal reflection at the output.

The amplifier achieves a flat gain ($|S_{21}|$) of 21 ± 0.5 dB, indicating excellent gain flatness throughout the UWB frequency range as shown in Fig. 4. The carefully use of implemented feedback networks helps for this impressive result, ensuring that the amplifier maintains a consistent performance across the entire band.

The reverse isolation, indicated by (|S12|) in Fig. 5, demonstrates a consistent isolation of approximately -40 dB across the band. This high level of isolation is essential for minimizing signal leakage from the output back to the input and preventing unwanted feedback loops in UWB systems.

The output reflection coefficient ($|S_{22}|$), were simulated to be around -10 dB across the band, as seen in the graph, Fig. 5. These results validate the effectiveness

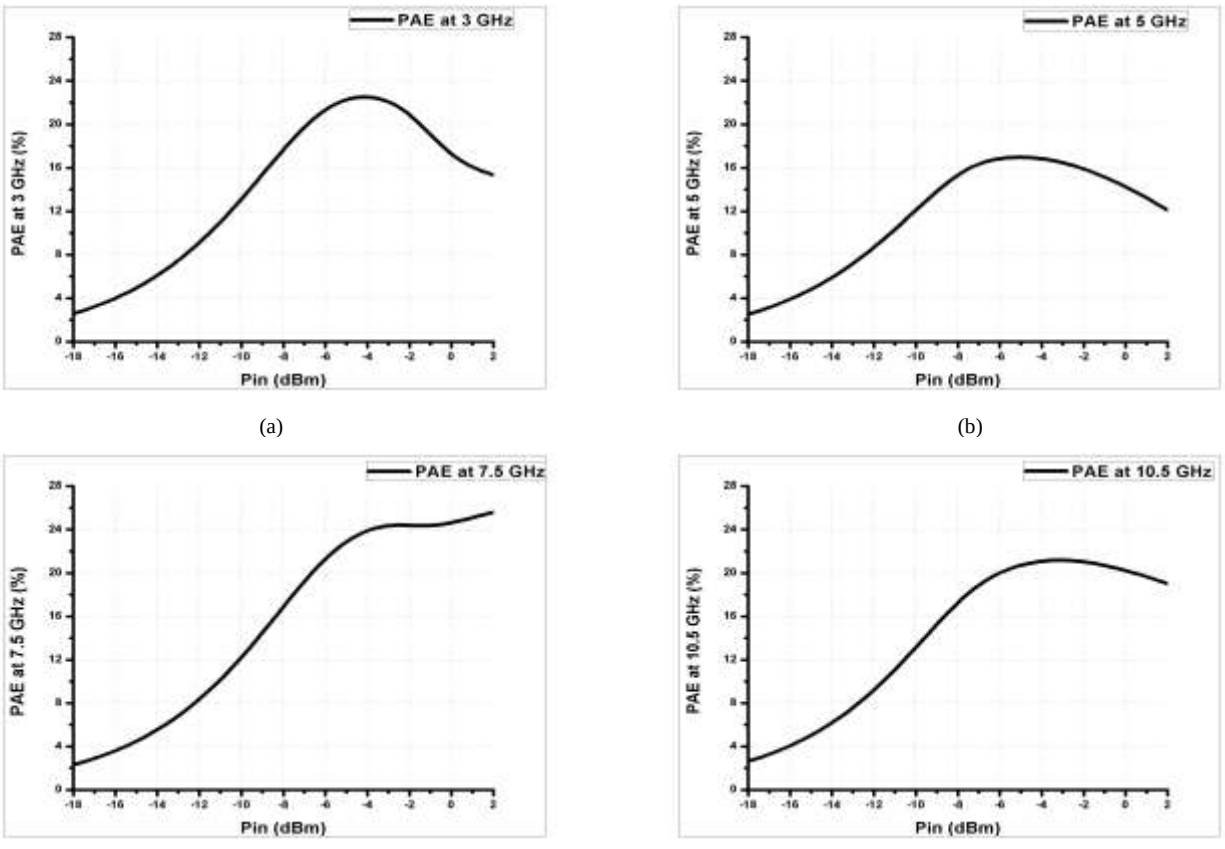


Fig. 6 The small-signal equivalent circuit of Complementary UWB RFPA

of the matching networks and feedback paths used in the design to maintain proper impedance matching over the ultra-wide bandwidth.

3.2 Power-Added Efficiency (PAE) and Output Power

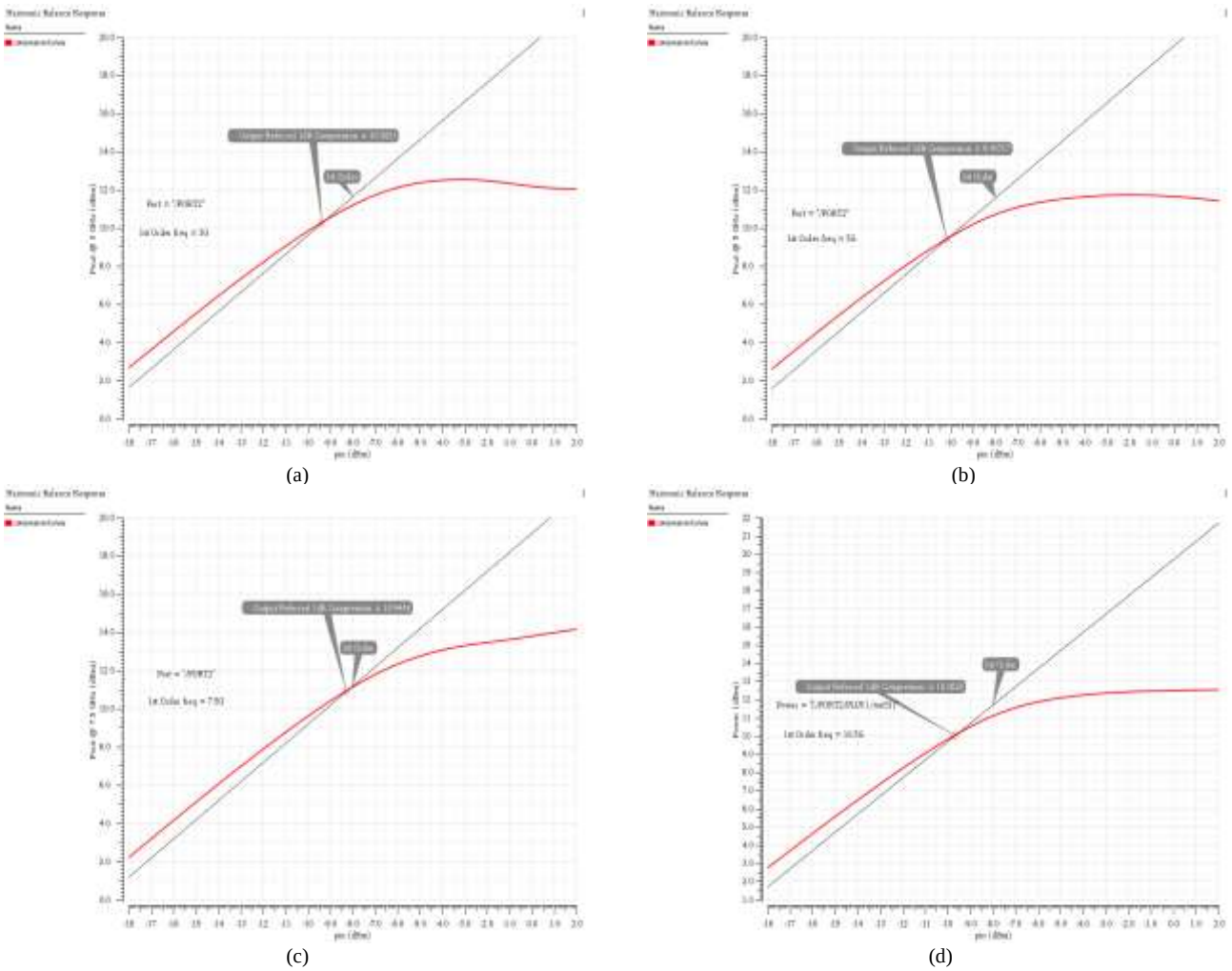
The power-added efficiency (PAE) of the UWB CMOS RFPA was evaluated at different frequencies, specifically at 3 GHz, 5 GHz, 7.5 GHz, and 10.5 GHz, as illustrated in the respective PAE Response Fig. 6. Across these frequencies, the PAE peaked at 22 ± 2%, with the 24% highest PAE occurring near the design's peak output power levels. This efficiency reflects the ability of the amplifier to effectively convert DC power into RF output power, minimizing energy loss. The PAE trends observed across the frequency band align with typical amplifier behaviour, where efficiency improves with increasing input power and flattens near the amplifier's saturation region.

The saturation output power reached 15 dBm at 7.5 GHz, which is a solid result for ultra-wideband applications. This output power ensures sufficient RF transmission strength, an important characteristic for UWB communication systems needing high-speed data transmission over a wide frequency range [11-14].

3.3 Linearity and Compression Behavior

One-dB compression point is an important criterion on the amplifier's linearity and is simulated over different frequencies, where the gain reduces by 1 dB due to saturation effects. Fig. 7 shows the harmonic balance simulation results. The amplifier achieves an output 1 dB compression point of 11 ± 0.5 dBm, which agrees well

with the target specifications for our design. The compression curves for 3 GHz, 5 GHz, 7.5 GHz, and 10.5 GHz have a similar shape, with slight differences only in



(a) (b) (c) (d)

Fig. 7 The simulated output power verses input power and 1-dB compression point at deferent frequencies: (a) 3 GHz (b) 5 GHz (c) 7.5 GHz (d) 10.5 GHz

the levels of output power, which maintain linearity close to saturation in the frequency range.

3.4 Results Comparison and Discussion

By tuning the circuit elements, the simulated results achieved improved performance for linearity and output power. Table 1 introduces the features of RFPA using Complementary Current Reuse Stage by highlighting a comparison with recently published articles. These features of 1 dB compression point demonstrate that the amplifier can provide high output power at linear operation conditions, therefore being suitable for wideband signals amplification applications such as UWB communication and radar systems.

Optimizing the antenna design with power amplifier on the same PCB minimizes the power loss [10]. The capability of operating close to saturation with efficiency and with extremely minimal distortion further reinforces the utility of the design in the power-sensitive environment such as UWB Antennas.

Table 1 The Features of RFPA Using Complementary Current Reuse Stage in Comparison to Recent Published Papers.

Ref.	[4]	[7]	[8]	[9]	This Work
CMOS Process	0.18 µm	0.13 µm	0.18 µm	0.18 µm	0.18 µm
Frequency (GHz)	5-10.6	6-9	3.1-10.6	3.1-10.6	2.9-10.8
Gain (dB)	14±1	8	11.5±0.7	28.7±2	21±0.5
S11 (dB)	<-5.5	<-8.5	<-8	<-10.2	<-10
S22 (dB)	<-7	<-9.5	<-10	<-13.7	<-8
PAE (%)	10	23.2	26	33	24
OP1dB (dBm)	2	7	9	5.6	11.5
Pdc (mW)	20	24	34	23	70.4
Year	2015	2018	2019	2021	2024

4 Conclusion

A radio frequency power amplifier with low power and high linearity has been proposed, implemented in the 0.18 µm CMOS process for ultra-wideband application. The proposed design uses multiple feedback networks at both input and output terminals of each configuration to improve the gain flatness, impedance matching, and power efficiency. It is found that the proposed RFPA shows a flat gain of 21 ± 0.5 dB to ensure consistent amplification over the UWB spectrum. It also provides a saturated output power of 15 dBm at 7.5 GHz, while the 1-dB compression point is 11±0.5 dBm. The maximum PAE is 24 % and proves very formidable in converting energy with the best efficiency. The input and output reflection coefficients are very small and also ensure that there will be negligible signal loss and very effective power transfer within this wide-band frequency. The amplifier has a DC power consumption of 23.4 mW and 47 mW from a 1.8 V supply for driver stage and power stage respectively, which makes it suitable for UWB devices with batteries.

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