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Performance Enhancement of Electrical Power System Using FACTS Devices

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Abstract. : In this paper, the objective is to promote the power system performance by using Unified Power Flow Control (UPFC) and Static VAR Compensator (SVC) then comparing the results in different networks. The results are tested on the IEEE 5 bus, IEEE 9 bus, and IEEE 30 bus, by using computer software MATLAB/PSAT. The Optimal location of FACTS is determined by using Continuation Power Flow (CPF) in PSAT to find the weakest point. Particle Swarm Optimization (PSO) is used to reach the optimal location of FACTS.Theobjective function is the voltage deviation of the bus and the power losses.

To get appropriate FACTS locations easier and with more flexibility, In this paper, a new interface that depends on PSO to detect the most suitable positions is used to select the ratings of FACTS equipment in power system networks. This application called the Optimal Power Flow (OPF) toolbox, It enables the servant to choose a power system network and define the PSO settings. Then, the operation that relies on PSO to obtain the best conditions is carried out to increase the system's stable load capacity. The emulation outcomes obtained by IEEE test networks using 118 buses prove the appropriate effectiveness and flexibility of the FACTS OPF toolbox.

Keywords.: Power system, FACTS, UPFC, SVC and particle swarm optimization algorithm (PSO).

1. INTRODUCTION

Generating station is the source of power, this power is carried out via Transmission Line until it becomes available to the end-user. It is important for arrangement, activity, financial planning and density trade between facilities. Load flow studies are performed using the Newton Raphson strategy. Transmission line is characterized by resistance, inductance, and capacitance. This can cause losses. These losses cannot be completely removed; however, they can be reduced. Voltage breakdown [1-4] generally occurs on the power system that is heavily loaded and is further spread with low reactive power. The most effective way to cope with a voltage breakdown event is either to reduce the VAR power load or to supply the system with more reactive energy before the system reaches the voltage breakdown. The power of power system is an important perspective to consider the structure and activity of power system. System administrators must understand power system security breakpoints to create a basic step to make them stable.

The power system necessarily be worked while power and line voltages remain within a range without caring to variations in loads. The variation in VAR power is the reason for voltage irregularity in the power system. The more loading, the more the line will administer the price of relying on the VAR energy that the system gives to it [5], and under this condition the power loss components are peaked. Taking all these considerations, to build a steady system is produced by decreasing the VAR power or by

applying a source of VAR power, capacitors for example or FACTS equipment at the perfect position before the system reaches the voltage breakdown point. FACTS devices provide rapid and reliable control on voltage value, phase, and line reactance. FACTS support the system regularity with no modification in generator constants [6]. UPFC gives higher voltage dominance once confronted with SVC and Static Synchronous compensator (STATCOM). Many directrices are suggested that depend on the voltage-stability margin of the system. Data concerning voltage regularity can be specified with the help of those directrices [7]. Different techniques were introduced for voltage stability examination, as an example, Eigen values of the Jacobian grid, L index and P-V curve.

The simulation is carried out with the help of the power system Analysis Toolbox (PSAT) of MATLAB and the best position is specified by CPF and stability indicators, VCPI and FVSI. The most crucial line is one with minimal voltage or the one having the greatest value of the index for the largest allowed load concerning a line, monitor that line (wrong information). It is found that by suitable selection of UPFC and SVC positions, the acceptable variation in the load value of any system would be largely extended to enhance the voltage regularity.

1.1. PRINCIPLE OF UPFC

Currently, many power electronic devices are applied to promote the development of a large amount of energy. These electronic circuits are named as FACTs equipment. The first part of this equipment is manic with voltage source converters (VSC), also they can supply the potential of fast and adaptable control of power stream in the power system. On such buses, the main controller on energy flow is the amount of VAR power that flows within the transmission line of the power system. Subsequently, a reduction in the VAR power margin would result in a drop in the voltage on the other hand, a rise in the VAR power margin will lead to a climb in voltage value [8-9].UPFC [10] is used to command power flows within transmission line, voltage value and angle in a power system. Figure1shows the basic structure of UPFC.

The UPFC concept was intended as supportive devices that give fast-acting VAR power transmission on a high voltage power system. IT could be a combination of a STATCOM and an SSSC combined together via a typical DC voltage connection, it is formed of two VSC with semiconductor technology with switching off capability that share the same dc capacitor and related to a powerful framework via a transformer with unit turns ratio.

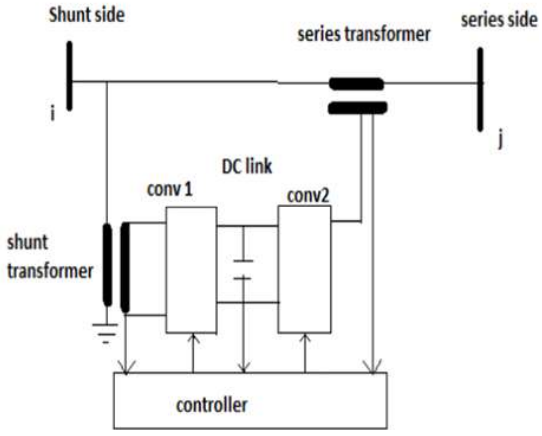

Fig1: UPFC Basic structure of SSSC, STATCOM

By injecting voltage V_{pq} with terminal voltage Vo, the UPFC helps in series and parallel alongside angle shifting power flow as shown In figure2

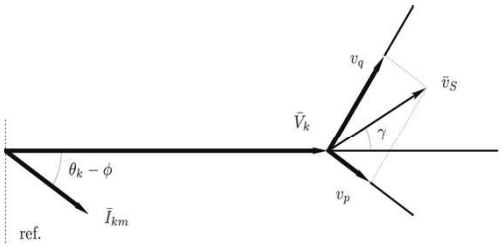

Fig2: UPFC Phasor Diagram

When two VSC are utilized in UPFC mode at the point, the converters in series works as SSSC while the parallel one acts as STATCOM that amend the voltage at the link by varying the VAR power by either absorption or generation of it. So, the wattage power could be authorized to pass in a series converter via DC link. The general domination of VAR power could be done by changing the DC link volt.

If UPFC is absent, at an ideal power stream, zero volts are supplied through the line by the series converter, whereas within the UPFC point of view, both value and angle of the volt supplied in series could be changed consequently, the VAR and Wattage power could be planned. At the point, while the supplied voltage goes to its extreme rating and the stage boundary is passed 0º

to 360º, at that point we will get the controllable area for UPFC is obtained [20]. In PSAT software [11-13] the executed UPFC paradigm is performed according to [14-16]. The paradigm is done by combining a STATCOM with SSSC. It is illustrated by a series voltage source $\overline{v}_s$ and by a parallel current source $\overline{i}_{SH}$, as indicated in Figure 3.

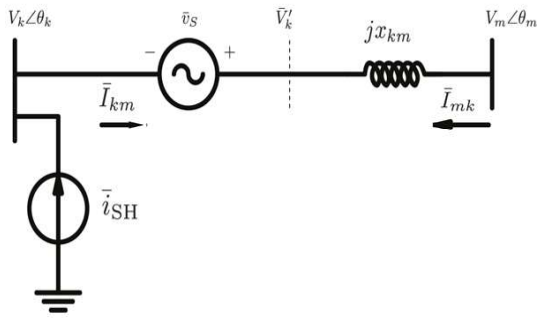

Fig3: UPFC Circuit

Both volt and current supplies can be defined as following

$$\overline{v}_s = (v_p + v_s)e^{j\phi} = rV_k e^{j\gamma} \quad (1)$$

$$\overline{i}_{SH} = (i_p + i_q)e^{j\phi_k} \quad (2)$$

The equivalent phas or representation of a series voltage source is displayed in Figure 2, and the power equations that represent the power injection model of the UPFC are [11]:

$$P_{km} = brV_k V_m \sin(\gamma + \theta_k - \theta_m), \quad (3)$$

$$Q_{km} = brV_k^2 \cos(\gamma) - i_q V_k, \quad (4)$$

$$P_{mk} = -brV_k V_m \sin(\gamma + \theta_k - \theta_m), \quad (5)$$

$$Q_{mk} = -brV_k V_m \cos(\gamma + \theta_k - \theta_m). \quad (6)$$

Figure 4 shows that the Power Oscillation Damper (POD) controller can be used to modulate any of UPFC parameters v_p , v_q and i_q . The system can be described by the following equations [11]:

$$\dot{v}_p = (\frac{1}{T_r})(v_{p0} + u_1 v_{POD} - v_p) \quad (7)$$

$$\dot{v}_q = (\frac{1}{T_r})(v_{q0} + u_2 v_{POD} - v_q) \quad (8)$$

$$\dot{i}_q = (\frac{1}{T_r})\left[K_r(V_{ref} + u_3 v_{POD}) - i_q \right] \quad (9)$$

Where u_i and *i = 1, 2, 3* is set to 1 if the correspondent stabilizing POD signal is enabled, 0otherwise.Table 1 reports the data and control parameter format for the UPFC.

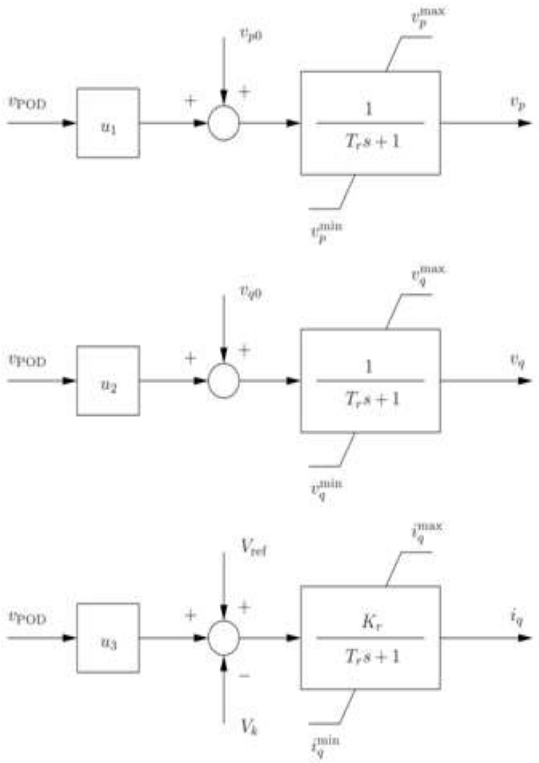

Fig4: UPFC controller diagrams

Table 1: UPFC Data Format on PSAT

Column	Variable	Description	Unit
1	i	Line number	int
2	-	Operation mode 1 Constant voltage 2 Constant reactance	int
3	S_n	Power rating	MVA
4	V_n	Voltage rating	kV
5	f_n	Frequency rating	Hz
6	C_p	Percentage of series compensation	%
7	K_r	Regulator gain	p.u./p.u.
8	T_r	Regulator time constant	s
9	$v_p^{\max}$	Maximum v_p	p.u.
10	$v_p^{\min}$	Minimum v_p	p.u.
11	$v_q^{\max}$	Maximum v_q	p.u.
12	$v_q^{\min}$	Minimum v_q	p.u.
13	$i_q^{\max}$	Maximum i_q	p.u.
14	$i_q^{\min}$	Minimum i_q	p.u.
15	-	Stabilizing v_p signal	$\{0,1\}$
16	-	Stabilizing v_q signal	$\{0,1\}$
17	-	Stabilizing i_q signal	$\{0,1\}$
18	u	Connection status	$\{0,1\}$

1.2. PRINCIPLE OF SVC

SVC is a section of FACT equipment and it is a set of electrical devices for providing rapid VAR power on transmission networks [17-20]. SVC is designed with the aim of achieving matching and reach unity Power Factor (PF). SVC is needed in one of two cases:

- Connected to the power system, to regulate the transmission voltage.
- Connected near large industrial loads, to improve power quality.

The design of the SVC is indicated in Figure 5. In PSAT, SVC design uses a time constant regulator, as indicated in Figure 6 and the system equation is described by [11]:

$$\dot{b}_{svc} = (K_r(V_{ref} + v_{POD} - V) - b_{scv})/T_r \quad (10)$$

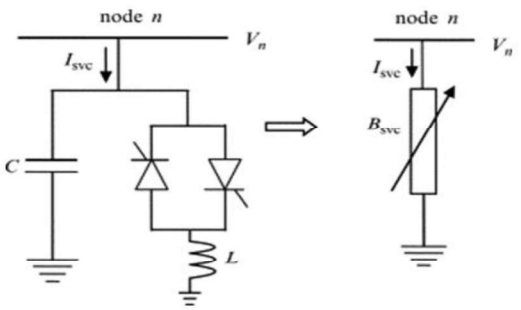

Fig 5: SVC basic structure

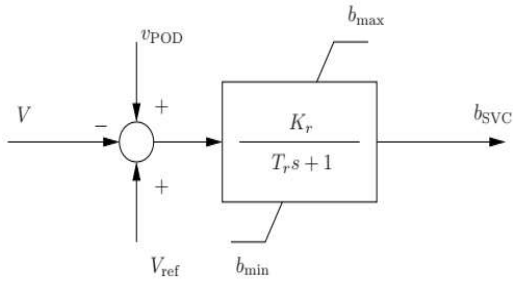

Fig 6: SVC block Diagram

VAR power also is expressed by [11]:

$$Q = b_{SVC} V^2 \quad (11)$$

Table 2gives the variable description and units for the SVC.

Table 2: SVC Data Format on PSAT

Column	Variable	Description	Unit
1	-	Bus number	int
2	S_n	Power rating	MVA
3	V_n	Voltage rating	kV
4	f_n	Frequency rating	Hz
5	1	Model type	int
6	T_r	Regulator time constant	s
7	K_r	Regulator gain	p.u./p.u.
8	V_{ref}	Reference Voltage	p.u.
9	$b_{\max}$	Maximum susceptance	p.u.
10	$b_{\min}$	Minimum susceptance	p.u.
17	u	Connection status	$\{0,1\}$

2. Steady State Stability

Simulation results will be achieved for different IEEE test systems without and with FACTS. The types of FACTs that will be used is SVC and UPFC.

2.1. Results and Discussion for IEEE 5 Bus

IEEE 5 bus system is totally consisting of 2 Generator Buses (GB), 4 Load Buses (LB) and 7 transmission lines. In Figure 7 there are 5 buses, bus No. 1 is kept as a slack bus which maintains its voltage at 1.06 p.u. and bus 2 generator (PV) Bus.

2.2. Steady state study

By utilizing PSAT programming, as shown in Figure 7 and using CPF to obtain the PV curve of the IEEE 5 bus system and to determine weak bus during voltage collapse, and it is taken as the ideal bus for FACTS location. The PV curve of the IEEE 5 bus system is shown figure 8.

As shown in Figure 8, the voltage collapse happens at the most extreme loading parameter of λ_{max}=4.9051 and voltage magnitude of 0.5852 p.u. at bus 5 (Dark line). The weakest bus is taken as bus5. and it will be taken as the best location for FACTS.

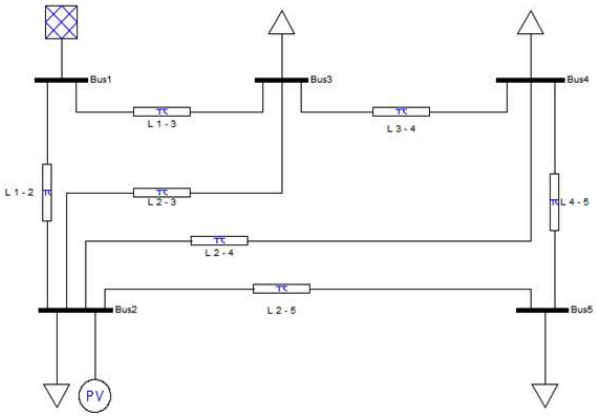

Fig 7: PSAT Model of IEEE 5 Bus System

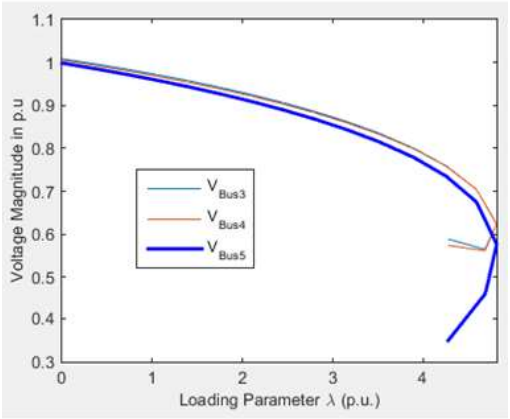

Fig 8: PV curve of IEEE 5 bus system without FACTS

As depicted previously, the SVC was injected with 49 MVARin the weakest bus each in turn and it is obvious that voltage profile and PV curve for IEEE 5 bus system with SVC at the bus no. 5 is improved. From Figure 9,it is observed the most extreme loading factor of λ_{max}=5.0037 has incremented when contrasted with the base case, for example, λ_{max}=4.9051 and likewise improve the voltage profile. Along these lines, bus 5 is the ideal area of SVC.

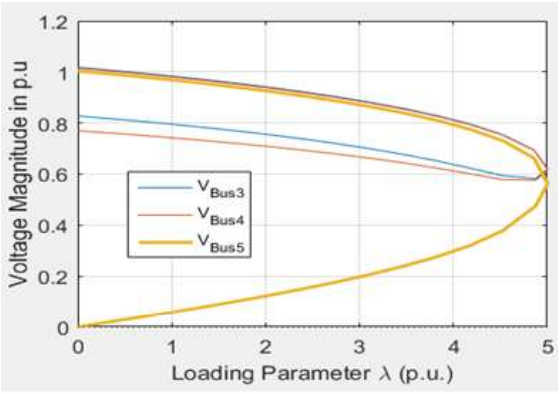

Fig: 9 PV curve of IEEE 5 bus system with SVC

Likely, UPFC with I_{SH} =3 p.u,V_{SE} =0.0076252 p.uwasplaced in between bus 4 and 5at a time and it was found that voltage profile and PV curve for IEEE 5 bus system with UPFC is improved. From Figure 10, it is observedthat the maximum loading factor of λ_{max}=5.6392has been increased when compared to the SVC case i.e. λ_{max}=5.0037, also improve the voltage profile.

Figure 10 shows that with UPFC between 4 and 5 the load system buses have been increased and reached the voltage collapse at the bifurcation point at λ=5.6392 . In other words, with UPFC the load factor can be increased by 12.7% before reaching voltage collapse if UPFC is used instead of SVC. And can be increased 15% compared to no FACTS devices.

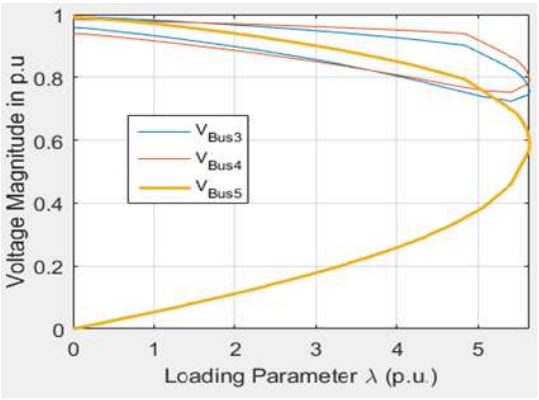

Fig 10: PV curve of IEEE 5 bus system with UPFC

2.3. Results and Discussion for IEEE 9 Bus

IEEE 9 bus system is totally consisting of 3 GB, 3 LB and 6 transmission line. In Figure 11 there are 9 buses; bus No. 1 is kept as slack bus which maintains its voltage at 1.04p.u. Bus 2 and bus 3 are generator (PV) Buses.

2.4. Steady state study

By using PSAT software, the PV curve of IEEE 9 is shown in figure 12.

Figure 12 shows that the voltage collapse occurs at the maximum loading parameter of λ_{max}=2.4933 and voltage magnitude of 0.7261 p.u. at bus 5 (Dark line). So, weakest bus is taken as bus 5 and it is taken as optimal bus for placement of FACTS.

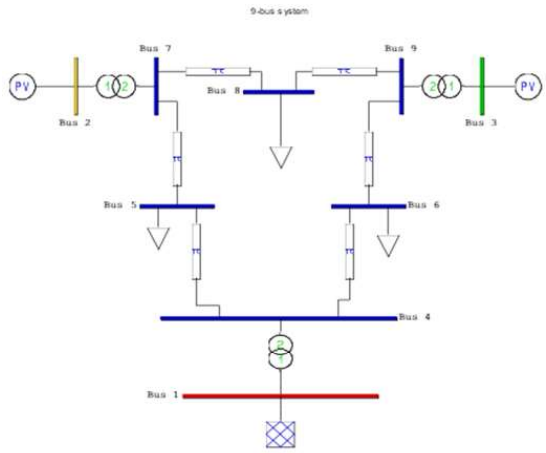

Fig 11: PSAT Model of IEEE 9 Bus System

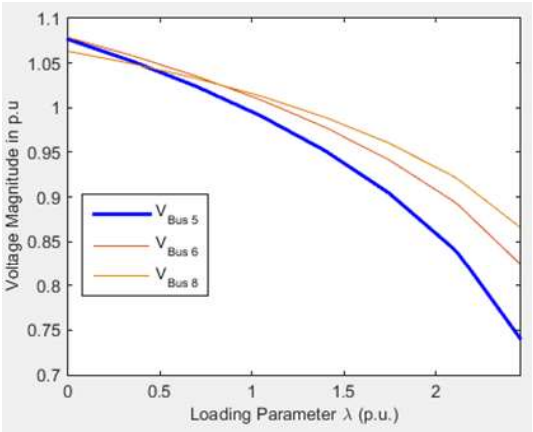

Fig 12: PV curve of IEEE 9 bus system without FACTS

As described in the above section, the SVC has injected 20 MVAR in the weakest bus one at a time and it is found that the voltage profile and PV curve for IEEE 9 bus system with SVC at bus no. 5 is improved. In Figure 13, it is observed that the maximum loading factor of λ_{max}=2.756 has increased compared to the base case i.e. λ_{max}=2.4933.. So, bus 5 is the optimal location of SVC.

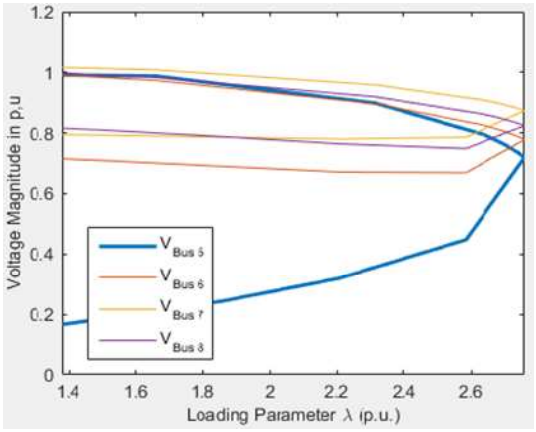

Fig 13: PV curve of IEEE 9 bus system with SVC

Similarly, UPFC was placed, with I_{SH} =3 p.u ,V_{SE} =.0011985 p.u , between bus 4 and 5 at a time and it was found voltage profile of PV curve for IEEE 9 bus system with UPFC is improved. From Figure 14 the maximum loading factor of λ_{max} = 3.3124has increased when compared to the SVC case i.e. λ_{max} = 2.756, also the voltage profile was improved.

Figure 14 shows that with UPFC between bus 4 and 5 the load system buses have been increased and the voltage collapse will be reached at the bifurcation point at λ_{max}=3.3124. In other words, with UPFC the load factor can be increased by 21% before reaching voltage collapse if UPFC is used instead of SVC and increased to 33% compared to no FACTS.

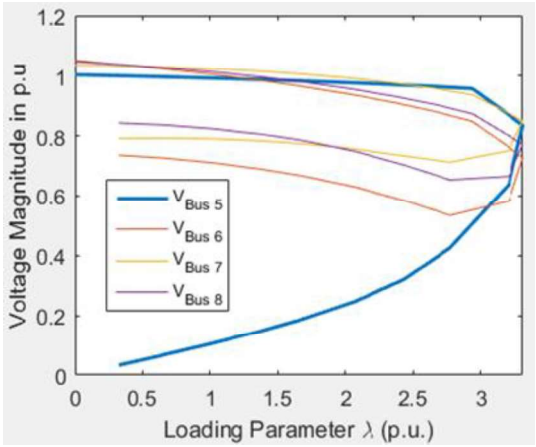

Fig 14: PV curve of IEEE 9 bus system with UPFC

2.5. Results and Discussion for IEEE 30 Bus

IEEE 30 bus system is totally consisting of 6 GB, 24 LB, and 41 transmission lines. IEEE 30 bus system consists of 6 generators buses, 24 load bus and furthermore 41 transmission lines. Bus 1 is

taken as the slack bus. By applying PSAT programming and using the NR load flow method, the resultant power flow is obtained i.e voltage magnitude and phase, wattage and VAR power generation, and load.

By using the CPF on PSAT programming can get the PV curve of the IEEE 30 bus system and furthermore recognize the weakest bus during voltage collapse, and it is taken as the ideal bus for FACTS location situation. The PV curve of the IEEE 30 bus system is shown in figure 16. Figure 16 shows the PV for buses 26, bus 29, bus 30.

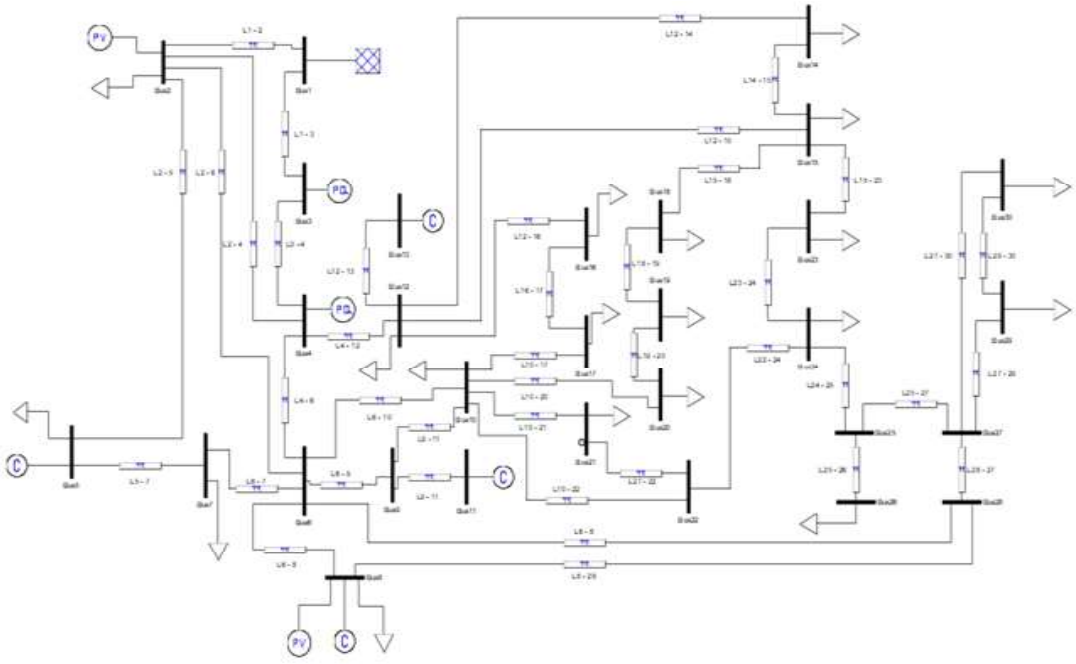

Fig 15: PSAT Model of IEEE 30 Bus Systems

2.6. Steady state study

By using CPF on PSAT programming, the PV curve of IEEE 30 bus system is obtained and further more recognize the weak bus during voltage collapse. It is considered as the ideal bus for FACTS location.

Figure 16 shows that the voltage collapse happens at the most maximum loading parameter of λ_{max}=2.188 and voltage magnitude is 0.4962p.u. at bus no.30 (Dark line). In this way, weakest bus is taken as bus 30. Also, it is taken as ideal bus for FACTS location.

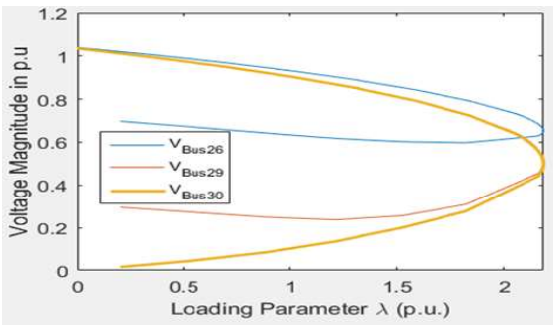

Fig 16: PV curve of IEEE 30 bus system without FACTS

As described before, the SVC injected 80 MVAR and placed at the weakest bus one at a time. It is found that voltage profile and from the PV curve for IEEE 30 bus system with SVC at bus 30 is improved. From Figure 17 the maximum loading factor of λ_{max}=3.1318has increased compared to the base case i.e. λ_{max}=2.188,and also improve the voltage profile. Therefore, bus 30 is the optimal location of SVC.

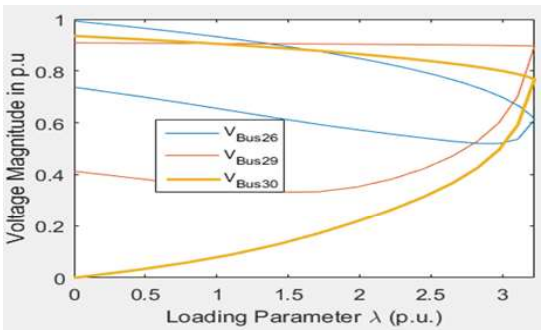

Fig 17: PV curve of IEEE 30 bus system with SVC

Similarly, UPFC is placed with I_{SH} =3 p.u ,V_{SE} =.0011985 p.u between bus 29 and 30 at a time and it was found that voltage profile and PV curve for IEEE 30 bus system with UPFC is improved. Figure 18shows that the maximum loading factor isλ_{max}=3.222and it has been increased when compared by the SVC.Figure 18 shows that with UPFC between bus 29 and 30 the voltage profile of the load buses has been increased and the voltage collapse will be reached at the bifurcation point λ=3.222.

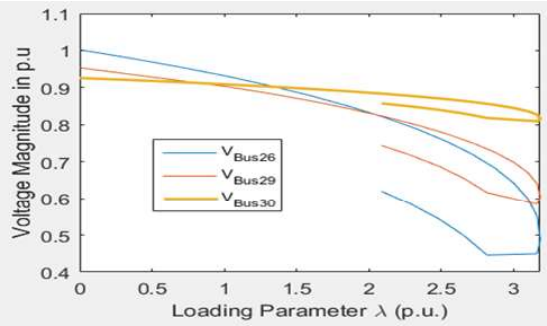

Fig 18: PV curve of IEEE 30 bus system with UPFC.

In other words, with UPFC the load factor can be increased by 2.8% before reaching voltage collapse if UPFC is used instead of SVC and hence it can be increased 68% compared to no FACTS.

3. PSO algorithm

PSO is used to determine the busses where FACTS devices can be located as shown in figure 19.

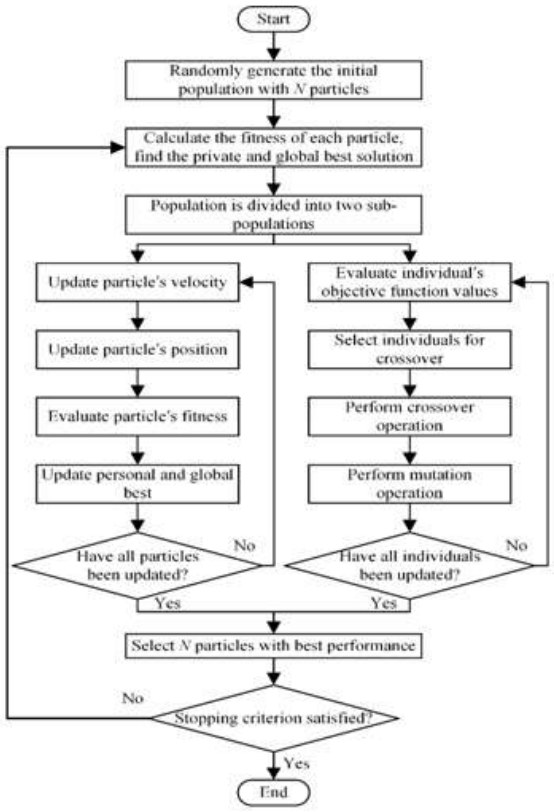

Fig19: flow chart PSO algorithm

3.1. Fitness Function

Considering power loss as the target function:

$f(x)$ = *fitness func. (variable)* (12)

$f(x)$ = *loss + sum* $((1.1-abs(v)^2)$ (13)

3.2. Constraints

In this section, some constraints were considered to minimize the problem [7]

3.2.1. Equality Constraints

The wattage and VAR power constraints are indicated by the following two equality equation [8]:

$$Pi=|Ui|\ {}^{n}\textstyle\sum_{k=1}|U_k||Y_{ik}|cos(\Delta_{ik}+\delta_k-\delta_i) \quad (14)$$

$$Qi=-|Ui|{}^{n}\textstyle\sum_{k=1}|U_k||Y_{ik}|sin(\Delta_{ik}+\delta_k-\delta_i) \quad (15)$$

Where n is the number of buses i=1, 2, 3...n

3.2.2. Inequality Constraints

- Voltage value,

$$|Ui|_{min}\leq|Ui|\leq|Ui|_{max} \quad (16)$$

- Bus Voltage angle inequality constraint:

$$|\delta i-\delta k|\leq|\delta i-\delta k_{max}| \quad (17)$$

- Real power inequality constraint:

$PG_{imin} \leq PG_i \leq PG_{imax}$ (18)

- Reactive power inequality constraint:

$QG_{imin} \leq QG_i \leq QG_{imax}$ (19)

3.3. Simulation Results

Now, by applying PSO for IEEE 30-bus network. The number of links and FACTS optimal positions was obtained, and the target functions were improved. The values used for PSO are recorded in Table 3

.

Table 3: PSO settings.

Population size, N:	25
Maximum iteration, t_{max}	100
Number of runs, Nru	1
Cognitive constant, C1	2
Social constant, C2	2
Max inertia weight, w1	0.9
Min inertia weight, w2	0.4

3.4. GUI Description

GUI interface is shown in Figure 20, the user firstly select the network standard ranges (6-118 buses), then choose the target parameter and the used algorithm, finally insert algorithm parameters based on values in Table 3.

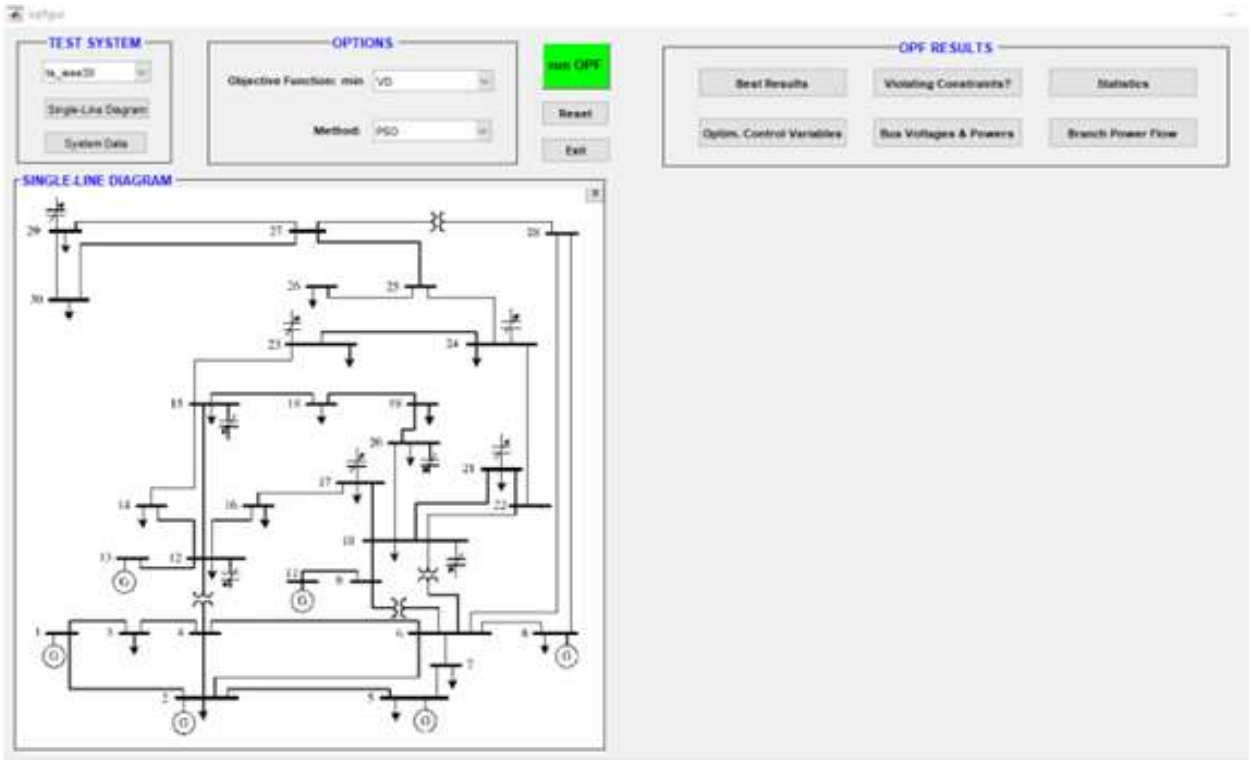

Fig 20: FACTS GUI

3.4.1. Case study (IEEE 30 bus)

Voltage deviation is used as a target function, the average convergence rate is presented in Figure 21. the result shows that FACTs can be placed at multiple buses. The voltage profile before placing UPFC shows that the best location of UPFC is between buses 21 – 22. Hence, the power loss has been calculated. Table 4 illustrates the bus voltage using PSAT and PSO for IEEE 30 bus system.

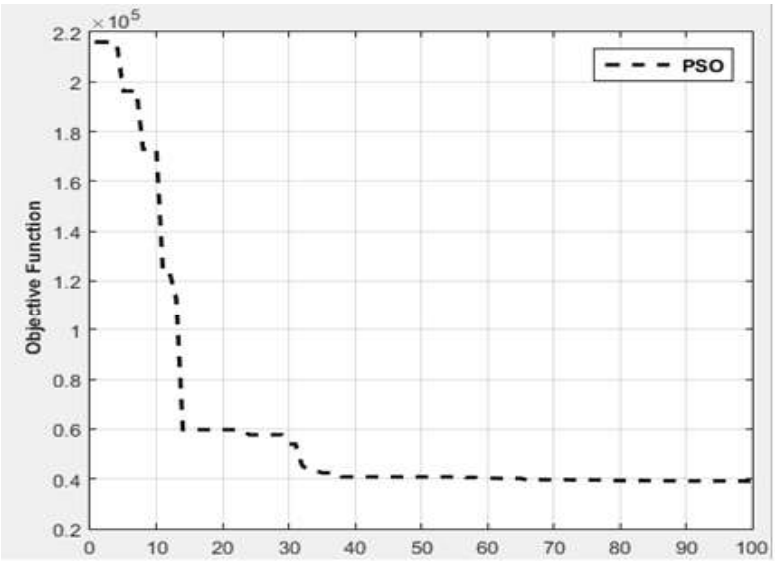

Fig 21: Convergence Speed of PSO for IEEE 30 bus

The voltage values are listed in table 4.A par chart that compares the values before and after adding UPFC is shown in Figure 22.

Table 4: Bus voltage between PSAT and PSO for IEEE 30 bus

BUS NO	PSO(P.U)	Psat(P.U)	BUS NO	PSO(P.U)	Psat(P.U)	BUS NO	PSO(P.U)	Psat(P.U)
BUS 1	1.0309	1.06	BUS 11	1.0907	1.082	BUS 21	0.9991	0.9786
BUS 2	1.0204	1.043	BUS 12	1.0091	1.0214	BUS 22	1	0.9787
BUS 3	1.0061	1.027	BUS 13	0.9907	1.071	BUS 23	0.9998	0.9745
BUS 4	1	1.018	BUS 14	0.9995	1.0009	BUS 24	0.9948	0.9606
BUS 5	1.0139	1.01	BUS 15	0.9999	0.9916	BUS 25	1.002	0.9512
BUS 6	1.0028	1.010	BUS 16	1.0016	1.0020	BUS 26	0.9841	0.9322
BUS 7	0.9993	1.002	BUS 17	1.0015	0.9902	BUS 27	1.0153	0.9545
BUS 8	1.0018	1.01	BUS 18	0.9943	0.9679	BUS 28	0.9999	1.0042
BUS 9	1.0051	1.019	BUS 19	0.9943	0.9680	BUS 29	1.0101	0.9061
BUS 10	1.0094	0.993	BUS 20	0.9998	0.9738	BUS 30	0.9923	0.9049

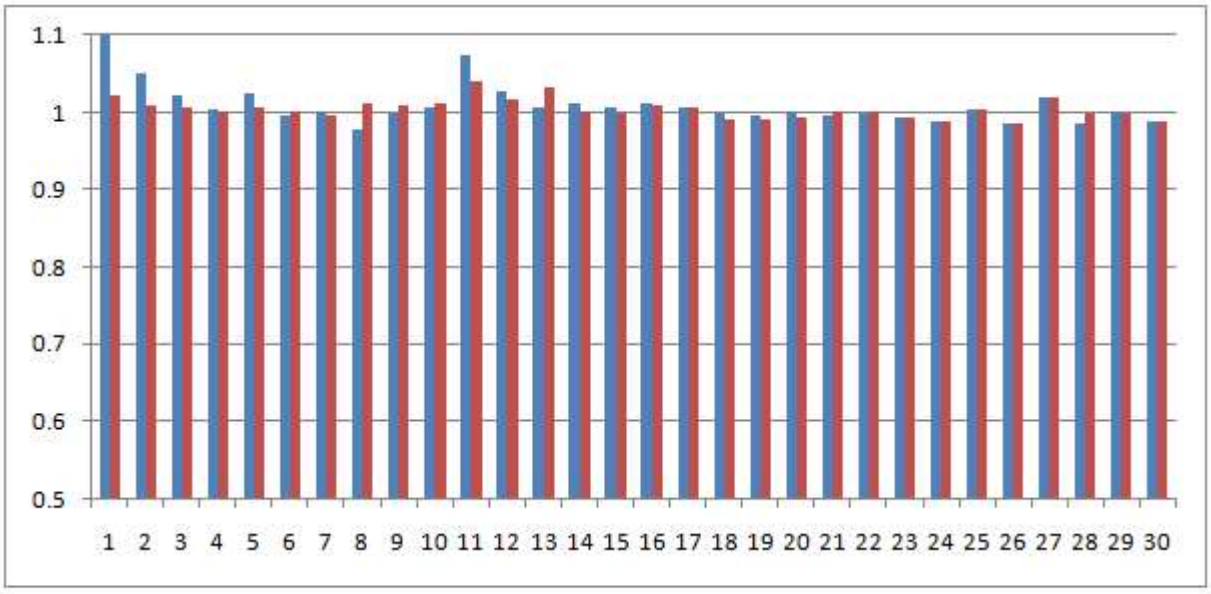

Fig 22: Voltage Profile after placing UPFC.

As mentioned above,By using PSAT the real power losses in IEEE 30 bus without using FACTS devices is **16.415** MW and voltage deviation is **0.164 (p.u.)** and after using PSO algorithm and placing FACTs device,the power losses will be reduced to **7.411** MW and voltage deviation to**0.106 (p.u.)**

4. Conclusion

The main objective in this paper is to minimize the power loss and to improve the voltage profile of power system by adjusting the power control parameters. FACTS devices have importance in the power system because they offer increased power transfer capability and better controllability of power flow. In this paper, UPFC has been employed to get the voltage improvement and loss minimization using PSAT and the continuation power flow technique. By using PSAT software, the optimal location of FACTS can be found; also the voltage magnitude was improved and power losses were minimized.CPF finds the weakest bus when voltage collapse occurs. The proposed algorithm was used to determine the optimal placement of the UPFC controller to enhance the voltage regularity and to reduce the power losses within real power and VAR power generation limits, and UPFC operation limits. The algorithm was applied in different IEEE test systems. All results were tested and compared with no FACTS installed in the power system and then compared after installation of SVC and UPFC. It was observed that FACTS enhance the performance of the systems from a steady-state stability perspective.

The PSO was used to find the best location for UPFC in power system under several loading conditions. The power flow in transmission lines is enhanced by using UPFC, the voltage magnitudes were increased, and the power losses were reduced.

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