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Review paper

Voltage Mode Drivers for Serial-Link Applications: Review

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Abstract

Serial links have emerged as a pivotal and widely adopted solution for enabling high- speed data communication among various devices and components in modern electronic systems, serving critical roles across diverse applications, including networking, computing, and data storage. Their increasing popularity can be attributed to their ability to facilitate efficient and reliable data transfer, which is essential for the optimal performance of increasingly complex electronic environments characterized by the need for rapid data exchange and real-time processing. However, the design and implementation of effective serial links present a myriad of significant challenges that engineers must adeptly navigate. Achieving high data rates is often accompanied by the pressing need to maintain low power consumption, a crucial factor in mobile and embedded systems where energy efficiency is paramount. Additionally, ensuring robust signal integrity is vital, as even minor deviations in voltage levels or timing can lead to substantial errors in data transmission, which can critically impact system performance and reliability. This article aims to explore the various innovative techniques proposed for voltage mode (VM) transmitters specifically tailored for serial-link applications. By thoroughly examining the strengths and limitations of these techniques, we seek to shed light on the cutting-edge approaches that not only enhance performance but also effectively address the inherent design challenges. Our goal is to contribute to the advancement and development of high-performance se- rial communication systems that meet the demanding requirements of today's technology landscape, ensuring that they can support the ever-increasing data rates and complexity of modern applications while maintaining the necessary reliability and efficiency. Through this exploration, we aim to provide insights that will be valuable to engineers and researchers working in the field, facilitating the ongoing evolution of serial communication technology and its applications.

Keywords: VM; CM; NRZ; PAM-4; RLM.

1 Introduction

Integrated circuit (IC) design is fundamental to a wide range of sectors, including consumer electronics, computing, telecommunications, automotive systems, medical devices [1], and industrial automation. These circuits serve as the backbone of modern technology, enabling the functionality of essential devices such as smartphones, computers, and various household appliances. Moreover, ICs are critical in emerging fields like the Internet of Things (IoT), aerospace, power management, and embedded systems, where they facilitate seamless communication and control among inter- connected components.

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One of the most prevalent solutions for high-speed data communication between devices is the use of serial links. These links have become a widely accepted solution for high-speed data communication among various devices and components. However, designing effective serial links presents significant challenges, as they must achieve high data rates while ensuring low power consumption and maintaining signal integrity. Although these links occupy less board space and chip perimeter, their engineering complexity, can introduce considerable risks to the first-pass success of ASICs [2]. One promising technique that has emerged to tackle these challenges is pulse amplitude modulation with four levels (PAM-4). By encoding two bits of information per symbol, PAM-4 effectively doubles the achievable data rate compared to traditional non-return-to-zero (NRZ) schemes. Nonetheless, the implementation of PAM-4 transmitters and receivers is inherently more complex and power-hungry than their NRZ counterparts. This trade-off between enhanced data rates and increased system complexity and power consumption is a critical factor to consider when designing and deploying serial-link communication systems.

PAM-4 signaling, which allows for the transmission of 2 bits per symbol, presents significant advantages for achieving higher data rates [3–5]. This is primarily because the clock frequency required for PAM-4 is only half that of NRZ signaling when transmitting the same data rate [6]. This characteristic makes PAM-4 particularly attractive in applications where bandwidth efficiency is critical. However, the PAM-4 signaling method also introduces challenges. One notable drawback is that PAM-4 signals have only one-third the eye height of NRZ signals. This reduced eye height results in a significant attenuation of signal-to-noise ratio (SNR) by approximately 9.5 dB [7, 8], which can adversely affect the reliability of data transmission. The diminished eye height makes PAM-4 signals more susceptible to noise and other distortions, which can complicate signal detection and integrity. Moreover, the non-linear characteristics of the transmitter output can lead to further SNR degradation [6]. This non-linearity may create imbalances between the various PAM-4 signal levels, resulting in inconsistencies that can impair the quality of the transmitted data. Since the overall performance of the system hinges on the smallest eye height produced by the transmitter, addressing these challenges is crucial. To optimize performance, it is essential to equalize the voltage differences between the PAM-4 signal levels [6]. This equalization helps to ensure that the levels are balanced, thereby improving the reliability of signal detection. Additionally, matching the channel impedance at each signal level is vital for minimizing reflections and maximizing signal integrity. By carefully managing these factors, designers can enhance the overall effectiveness of PAM-4 signaling in high-speed data communication systems.

Recently voltage mode (VM) drivers have become preferred over current mode (CM) drivers due to their lower power consumption. However, designing VM drivers presents several challenges for three primary reasons. First, the output swing is managed by varying the supply voltage of the driver, which requires effective supply regulation [9, 10]. Second, output impedance matching is influenced by the sizes of the devices and their terminal voltages, both of which are impacted by the output swing [10, 11]. Finally, incorporating de-emphasis can alter the terminal voltages of the output transistors, leading to degradation in impedance matching [10].

This review aims to provide a comprehensive literature review on the design of VM drivers for serial-link applications. We begin by highlighting the significance of serial links, which offer advantages such as high data rates, low power consumption, and improved signal integrity

compared to traditional parallel bus architectures. However, the design of effective serial links presents various challenges, including the need to achieve increasing data rates while ensuring robust signal integrity and low power usage. To address these challenges, we explore emerging techniques, particularly the adoption of PAM-4, which allows for the doubling of achievable data rates compared to conventional NRZ signaling. The structure of this review article is as follows: Section 2 covers the basic principles; Section 3 discusses NRZ and PAM-4 signaling; Section 4 presents the current state of VM drivers; Section 5 addresses the limitations; and Section 6 concludes the discussion.

2 BASIC PRINCIPLES

In the realm of high-speed data transmission and signal processing, driver circuits play a crucial role in ensuring reliable communication between components. A wireline transmitter (TX) performs three essential functions Fig.1: it converts multiple parallel, low-speed data streams into a single high-speed output through serialization, employs equalization techniques to mitigate signal degradation encountered during transmission, and ensures adequate output swings for accurate interpretation by the receiver. To facilitate these operations, various clock frequencies and phases are generated using a phase-locked loop (PLL), which synchronizes the timing of the transmitted signals. Additionally, the output transistors are safeguarded by electrostatic discharge (ESD) devices, which protect against voltage spikes and enhance the overall reliability and durability of the transmitter.

Two predominant types of drivers are used in a TX circuit are CM drivers [12–17] and VM drivers [18–25]. Each type offers distinct advantages and challenges that make them suitable for different operational scenarios.

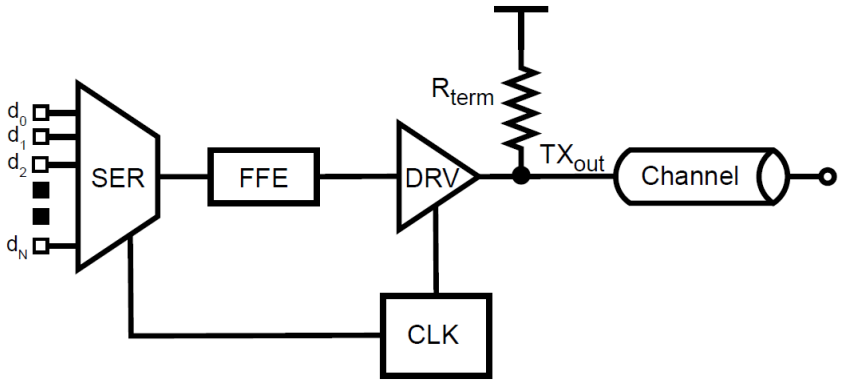

Figure 1: Generic wireline transmitter

2.1 Basic CM Drivers

CM drivers Fig.2 operate by controlling the output current rather than the output voltage. This approach allows for faster response times and improved signal integrity, particularly in high-frequency applications [26]. By focusing on current, these drivers can effectively handle variations in load conditions, making them ideal for environments where impedance may fluctuate. However, CM drivers often require more complex circuitry and can consume more power, especially at higher data rates. Their performance is also sensitive to temperature variations and other external factors [27], which can introduce noise and degrade signal quality.

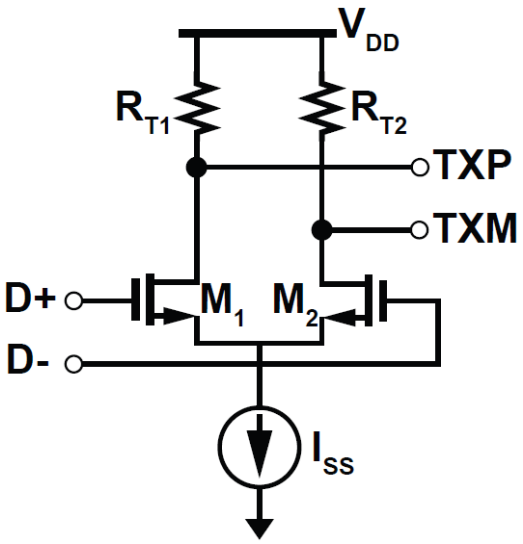

Figure 2: Basic CM driver circuit

2.2 Basic VM Drivers

In contrast, VM drivers Fig.3 control the output voltage levels directly. This method simplifies the design and implementation of the driver circuit, leading to reduced complexity and potentially lower power consumption. VM drivers are particularly advantageous for applications where consistent output swing is essential [10]. They are widely used in systems that prioritize energy efficiency and are increasingly favored in modern designs. However, one of the challenges with VM drivers is maintaining output impedance matching [28], particularly as the output swing varies. This requires careful design considerations to ensure stable performance across various operating conditions.

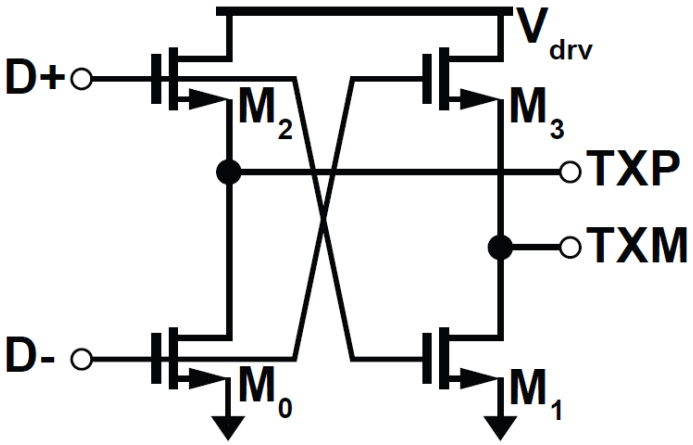

Figure 3: Basic VM driver circuit

VM drivers can be categorized into two primary configurations [10]: N-over-N Fig.4(a) and P-over-N Fig.4(b) drivers, each with distinct operational characteristics and advantages. N-over-N VM Drivers utilize n-channel transistors for both the pull-up and pull-down functions. This design is particularly advantageous in low-voltage applications, where n-channel transistors generally offer better electron mobility compared to their p-channel counterparts. As a result, N- over-N drivers provide high drive capability, enabling fast switching speeds and strong output swings, which are critical for driving capacitive loads effectively. Their efficiency in handling rapid transitions makes

them suitable for modern high-speed interfaces, such as those found in data centers, telecommunications, and high-performance computing systems. Additionally, N-over-N configurations often exhibit lower power consumption during switching, contributing to overall system efficiency. In contrast, P-over-N VM Drivers employ a combination of p-channel transistors for pull-up functions and n-channel transistors for pull-down functions. This configuration facilitates effective level shifting, which is

Actually, beneficial in applications where higher output voltage levels are necessary. P-over-N drivers are designed to deliver improved voltage swings, making them ideal for systems that require robust signal levels to ensure reliable data interpretation. These drivers are commonly used in battery-operated devices and low-power applications, where energy efficiency is paramount. Their ability to maintain signal integrity in varying load conditions further enhances their utility in diverse electronic designs. Both N-over-N and P-over-N VM drivers are integral to modern communication systems, ensuring reliable data transmission across various platforms. The choice between these configurations depends on specific application requirements, including factors such as power consumption, drive strength, switching speed, and overall signal integrity. Understanding the unique characteristics and benefits of each driver type is essential for engineers and designers aiming to optimize performance in high-speed digital circuits.

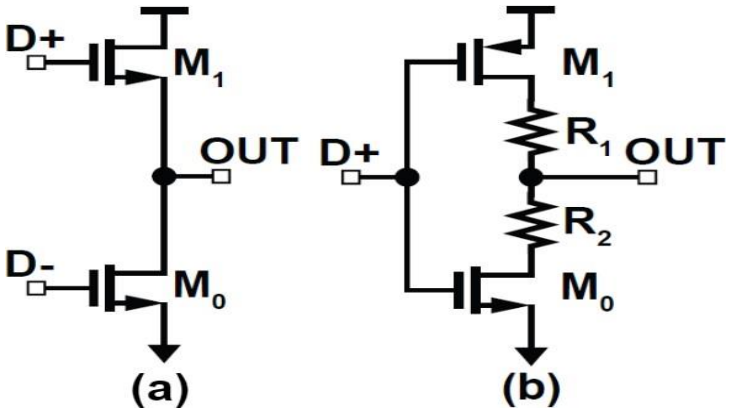

Figure 4: Schematics for (a) N-over-N and (b) P-over-N VM drivers.

3 NRZ AND PAM-4 SIGNALING

NRZ Fig.5(a) and PAM-4 Fig.5(b) are two prominent encoding schemes utilized in communication systems for the representation and transmission of binary data. These encoding techniques play a critical role in how information is formatted and sent over various media, impacting both bandwidth efficiency and signal integrity.

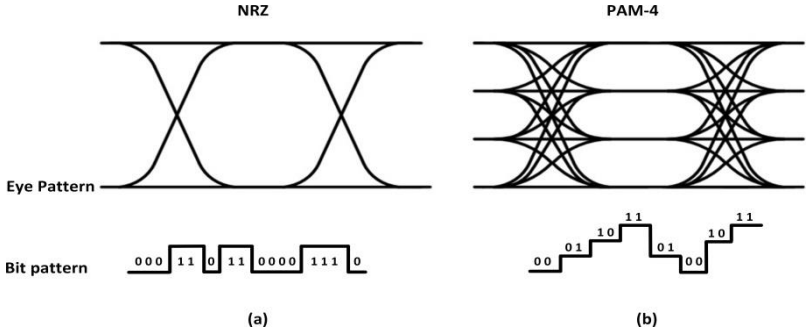

Figure 5: Eye Pattern and Bit Pattern for a) NRZ and b) PAM-4

3.1 NRZ

NRZ is one of the simplest and most widely used encoding methods, where binary data is conveyed using two distinct signal levels typically one voltage for a binary ’1’ and another for a binary ’0’. This method is efficient in terms of bandwidth usage, as it allows for a continuous signal that does not return to a baseline state between bits, hence the name ”Non-Return-to-Zero’ [29, 30]. The binary nature of NRZ data requires a single signal path with, in principle, no need for linearity [9]. Thus, NRZ signal swings are dictated by primarily speed and power considerations. However, while NRZ is straightforward and easy to implement, it faces challenges, particularly in maintaining synchronization and managing data integrity during long sequences of identical bits, which can lead to timing issues.

3.2 PAM-4

In contrast, PAM-4 is a more sophisticated encoding scheme that enhances data transmission capabilities by utilizing four distinct voltage levels to represent two bits of information per symbol. This approach effectively doubles the amount of data transmitted without requiring additional bandwidth, making PAM-4 particularly advantageous for high-speed applications, such as data centers and advanced telecommunication systems. However, the increased complexity of PAM-4 introduces challenges related to signal quality, as the closer proximity of voltage levels can make the system more susceptible to noise and other interferences. The primary issue at hand is the reduction in eye height, which can lead to an increase in the error rate of the receiver. This phenomenon is measured by the ”ratio of level mismatch” (RLM) Fig.6, defined as the smallest eye height divided by one-third of the total eye height equation (1) [9]. As a result, PAM-4 necessitates sophisticated equalization techniques and strong error correction methods to guarantee reliable transmission over extended distances.

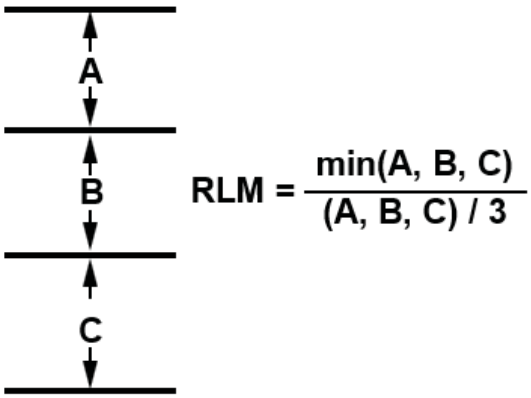

Figure 6: PAM4 transmitter output levels and linearity definition

$$RLM = \frac{min(A,B,C)}{(A+B+C)/3} \qquad (1)$$

In summary, both NRZ and PAM-4 serve as vital methods for encoding binary data in digital communication systems, each with its unique advantages and limitations. The choice between these encoding schemes is influenced by factors such as data rate requirements, bandwidth availability, and the overall complexity of the communication infrastructure, highlighting the importance of understanding their characteristics in the design of efficient digital networks.

4 State-of-the-Arts VM transmitters

In recent years, VM transmitters have seen substantial advancements, primarily driven by the escalating demands for high-speed data transmission in today's communication systems. As data rates continue to soar, it has become increasingly essential for drivers to not only handle these elevated speeds but also to improve power efficiency and maintain signal integrity. This evolution is vital, as it has a direct impact on the performance and reliability of high- speed digital interfaces, which are critical for applications ranging from telecommunications to data centers. In this context, understanding the underlying mechanisms and components of VM transmitters is key to addressing these challenges. This section offers a comprehensive literature review focusing on the primary functional building blocks of VM transmitters, examining their roles, advancements, and contributions to enhancing overall system performance.

4.1 Serialization

A serializer is an essential component that transforms parallel input words into serial data, facilitating high-speed data transmission. The delay difference between the clock path and the data path at each stage of the serializer can have a considerable effect on performance. This delay difference is affected by variation in the process, supply voltage, and temperature (PVT), which can increase jitter in the data eye and degrade the performance of the interface. Moreover, a delay difference greater than 1 unit interval (UI) may lead to setup and hold violations [31]. A commonly adopted and effective solution to address this challenge is the insertion of replica clock buffers in the clock path. One of the most widely used architectures is the binary tree serializer, which operates as a 2^N : 1 multiplexer made up of series 2:1 multiplexers. This design is particularly power-efficient in its initial stages, where static CMOS flip-flops and multiplexers can be employed due to the lower data rates. Also, the binary tree architecture can operate at half-rate to save power, but this will be sensitive to any duty-cycle distortion. In [32, 33], the binary tree architecture was operating at full-rate. In [34, 35], the binary tree architecture was operating at half-rate. This architecture becomes power hungry and sensitive to any process, supply voltage, and temperature variation if the serializer is multi-stage. Also, another disadvantage of it is the difficulty in implementing this architecture in the case of input data other than 2^N : 1 such as 10b or 20b input data. Another architecture commonly used for the implementation of any number of input parallel bits is the shift register as in [10, 31].

4.2 Driver

VM drivers are essential components in high-speed serial communication systems, where rapid and reliable data trans- mission is of utmost importance. These drivers function by converting digital signals into appropriate voltage levels that can effectively drive the transmission line, thereby ensuring that data integrity is preserved over extended distances and across various transmission media. However, power consumption remains a critical factor in the design, as excessive power usage can become a significant bottleneck. Research has shown that current-mode (CM) drivers can consume up to four times the power of their voltage-mode (VM) counterparts [36–39].

Among the various configurations, source series terminated (SST) drivers are the most prevalent topology used in VM drivers [10, 33, 40–42]. In this configuration, a resistor is placed in series with the output, effectively matching the driver's impedance to that of the transmission line, as illustrated in Fig.4b. This approach offers dual benefits: first, it divides the termination resistance between the transistor and the series resistor, thereby improving impedance matching - most designs typically employ a larger resistor compared to the inherent resistance of the transistor. Second, the configuration drives the transistor into deep-triode operation, where its resistance is primarily controlled by the gate voltage. This effectively decouples the termination from the voltage swing, allowing for a more stable performance.

By ensuring a proper impedance match, the SST driver can generate a robust voltage swing while minimizing signal distortion. This makes them particularly suitable for high-speed applications such as PCIe, SATA, and Ethernet, where maintaining high data rates is critical. Furthermore, SST drivers can integrate advanced features like pre-emphasis and equalization, which help to combat inter-symbol interference and other channel impairments. This combination of performance enhancements and design simplicity makes SST drivers an attractive choice for modern communication systems, balancing the need for efficiency with the demands of high-speed data transmission.

In summary, as the demand for faster and more reliable data transmission continues to grow, VM drivers, particularly those utilizing SST configurations, will remain at the forefront of innovation in high-speed communication technologies. Their ability to maintain signal integrity while minimizing power consumption positions them as vital components in the evolving landscape of data communication.

4.3 Equalization

Feedforward Equalization (FFE) is a type of equalization that compensates for the signal degradation by amplifying or attenuating specific frequency components of the signal. FFE is implemented using a linear filter, which boosts or attenuates the high-frequency components of the signal. It consists of several taps, each representing a coefficient that processes the input signal as shown in Fig.7. The FFE circuit uses an equalizer tap to adjust the filter coefficients. The number of taps determines the filter's complexity and its ability to compensate for the channel impairments. FFE can compensate for channel impairments such as attenuation, dispersion, and crosstalk. However, FFE is not effective in mitigating inter-symbol interference (ISI). The filter operates by attenuating low-frequency content when a stream of 1's or 0's is present, while allowing full signal swing during data transitions, effectively creating a high-pass filtering effect to counteract channel low-pass filtering. Common voltage mode equalization techniques include segmenting the driver into parts assigned to main, post, or pre cursors with inverted polarity, or using binary weighted slices for better decoupling. However, these methods tend to incur a high-power penalty due to opposing current flow needed for signal attenuation. To mitigate power penalties, several solutions have been proposed, such as adding a shunt network to stabilize current regardless of equalization settings as in [10, 28] or implementing a half-rate decoder to further reduce power consumption as in [43]. These designs may still face challenges like degraded return loss, which could affect signal integrity, especially in industrial applications that require compliance with standards.

4.4 Impedance Matching

The primary challenge of VM drivers is managing the termination in relation to the voltage swing. As the voltage levels change, it is crucial to keep the termination impedance properly matched to maintain signal integrity. Fluctuations in swing can result in reflections and distortions if the termination isn't adjusted accordingly, potentially degrading the performance of high-speed digital

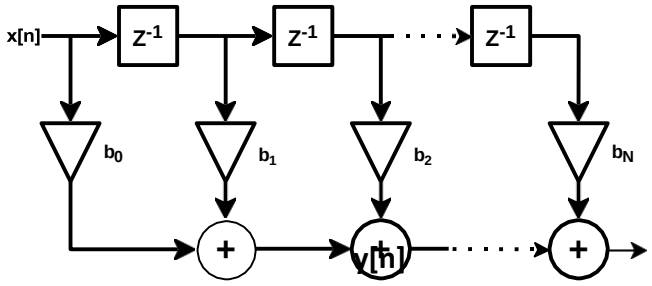

Figure 7: Block diagram of a 'N' order FIR filter

Communication systems In [40], a straightforward method for controlling the output impedance of a high-swing VM driver is to incorporate redundant segments that can be digitally activated to align with the channel impedance. In [10], a regulator was used to control the supply of the pre-driver in order to achieve the appropriate termination resistance.

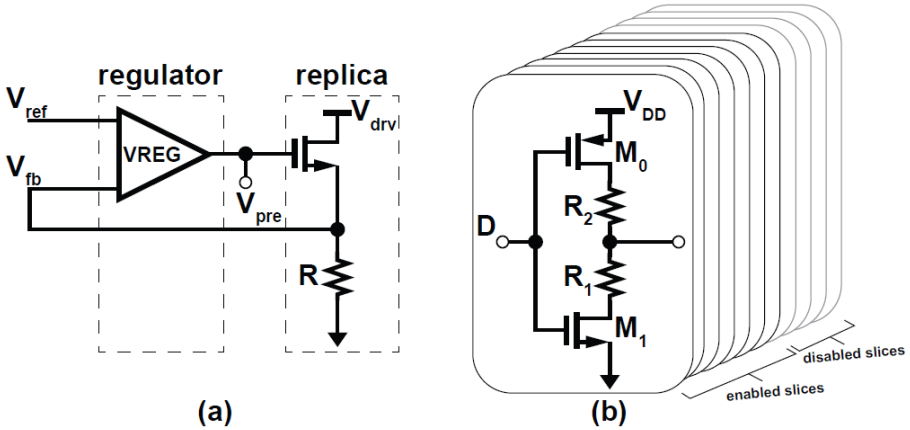

Figure 8: Impedance calibration using (a) analog calibration and (b) digital calibration

5 LIMITATIONS

VM drivers in high-speed data transmission face several critical limitations despite their technological advancements. While generally more power-efficient than CM alternatives, their power consumption increases significantly when implementing advanced features like pre-emphasis and PAM-4 signaling, which require additional circuitry for managing multiple signal levels and maintaining signal integrity. Signal integrity poses another major challenge, particularly at higher data rates where noise susceptibility increases and signal-to-noise ratio (SNR) may be compromised, especially with PAM-4's reduced eye height. The complexity of designing these drivers is compounded by the need for precise impedance matching, output swing regulation, and integration of sophisticated features like dynamic load control and impedance modulation, all of which must work harmoniously to maintain optimal performance across varying operating conditions. Additionally, the limited flexibility in adapting to various communication standards

presents a significant hurdle, as the inherent trade-offs between performance, power efficiency, and complexity can restrict their applicability in multi-standard applications, where adaptability is essential for meeting diverse communication requirements. These challenges collectively highlight the ongoing need for innovative solutions that can enhance VM driver performance while addressing these fundamental limitations in high-speed communication systems.

Table 1 illustrates a comparison between different VM drivers.

Table 1: Comparison between techniques

Parameter	[10]	[33]	[28]	[40]	[39]	[42]
CMOS Technology	65nm	28-nm	65-nm	65-nm	12-nm	28-nm
Type	NRZ	hybrid	NRZ	PAM-4	PAM-4	hybrid
Supply (V)	1.2	1	1.2	1.2	1	1
Swing (Vpp)	0.3-1	0.5	0.2	0.5	0.8	-
Power (mW)	5	5.5	10	-	48.5	72.96
Data rate (Gb/s)	1.5-12	21	10	18	50	48

6 CONCLUSION

This article provides a comprehensive review of VM drivers for serial-link applications, highlighting their growing preference over CM drivers due to lower power consumption, despite challenges in output swing management and impedance matching. It explores the two main VM driver configurations (N-over-N and P-over-N) and compares the traditional NRZ signaling with PAM-4, noting that while PAM-4 offers double the data rate, it faces significant challenges in signal integrity with its reduced eye height. The review demonstrates that despite significant advances in VM driver technology, several key challenges persist, including increased power consumption when implementing advanced features like pre-emphasis and PAM-4 signaling, signal integrity issues at higher data rates, complex design requirements for impedance matching and output swing regulation, and limited flexibility in adapting to various communication standards, all of which impact their performance and applicability in modern high-speed communication systems.

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