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Current-Mode Readout of Dynamic Random-Access Memories

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Abstract

During the reading of one-transistor one-capacitor dynamic random-access memory (1T-1C DRAM) cells, the need arises to amplify a small voltage difference (in the order of 30 to 100 mV) by a suitable sense amplifier. The net result is that the higher voltage will rise to V_{DD} while the lower one will decrease to 0 V. Simulation results for the 0.13 µm CMOS technology with V_{DD}=1.2 V reveals that about 40% of the read access time is associated with the sense amplifier operation in addition to the area required by each sense amplifier for each column in the memory array. In this paper, a novel current-mode readout technique for use with DRAM cells is presented. This method depends on converting the bitline voltage to a current to be compared with a reference current. The positive-feedback effect of the current comparator then comes into action with the result that one of its outputs will be the required output data taken at a much smaller parasitic capacitance compared with the bitline parasitic capacitance. Simulation results for the 0.13 µm CMOS technology show that about 10% of the read access time can be saved. The, the power-delay products in case of reading "1" (the worst case from the point of view of PDP) are 388.5 fJ and 188 fJ for the conventional and proposed schemes, respectively.

Key Words: *dynamic random-access memory, read cycle time, sense amplifier, current comparator.*

I. INTRODUCTION

Dynamic random-access memories (DRAMs) are widely used in computer systems as the primary storage due to its relatively fast access especially if compared with hard disks and due to its relatively high density compared to static RAMs. However, DRAMs suffer from bad retention due to the inevitable leakage currents that discharge the storage capacitor. In this paper, the conventional reading scheme of 1T-1C DRAM cells is discussed and a proposed current-mode reading scheme is presented. The proposed scheme depends on converting the bitline voltage to a current to be compared with a reference current. The positive-feedback effect of the current comparator then comes into action with the result that one of its outputs will be the required output data taken at a much smaller parasitic capacitance compared with the bitline parasitic capacitance. The dynamic-power consumption is consequently reduced.

The remainder of this paper is organized as follows: Section II presents the conventional reading scheme for 1T-1C DRAM cells while the proposed reading scheme is presented in Section III. The proposed reading scheme will be investigated quantitatively in Section IV. The impact of CMOS technology scaling on the proposed scheme is discussed in Section V. The proposed scheme will be simulated adopting the 0.13 µm CMOS technology with the simulation results presented in Section VI. Finally, the paper will be concluded in Section VII.

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II. CONVENTIONAL SCHEME

Although a variety of DRAM storage cells have been proposed over the years [1-5], a particular cell, shown in Fig. 1, has become the industry standard. The cell consists of a single access transistor, *M*, and a storage capacitor, C_s, and thus is known as the 1T-1C DRAM cell. The cell stores one bit of information in the form of charge on C_s.

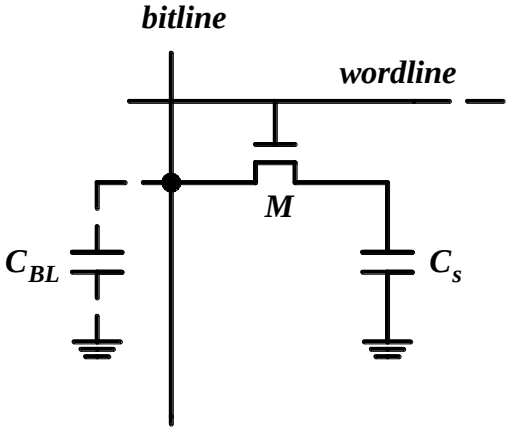


Fig. 1 The one-transistor one-capacitor dynamic RAM cell [6].

The write operation proceeds as follows: The wordline, *WL*, is first activated to a boosted voltage of V_{DD} + V_{thn}. Depending on whether the data to be written is logic "1" or logic "0", the bitline, *BL*, will be activated to V_{DD} or 0 V, thus causing the storage capacitor, C_s, to be charged to V_{DD} or discharge it to 0 V, respectively.

Now, the conventional reading operation of the DRAM memory cells will be discussed. Refer to Fig. 2 for illustration [7]. First, the two bitlines, *BL* and $\overline{BL}$, connected to the sense amplifier terminals will be pre-

charged to $V_{DD}/2$ and equalized to that voltage in order to block the effect of any noise on these lines where the complementary bitline is connected to a dummy cell. This is due to the fact that the differential voltage generated between the two bitlines, *BL* and $\overline{BL}$, is small (typically 30 mV) for modern CMOS technologies. The wordline, *WL*, is then activated to a boosted voltage, $V_{DD} + V_{thn}$. This turns on Q_c and charge sharing occurs between the cell capacitor, C_s, and the bitline parasitic capacitance, C_{BL}. If the cell to be read stores "1", then the cell capacitor, C_s, is initially charged to V_{DD} and thus the bitline voltage, V_{BL}, rises from $V_{DD}/2$ to $V_{DD}/2+\Delta V$. The small differential voltage, ΔV, between the two bitlines, *BL* and $\overline{BL}$, will be amplified by virtue of the sense amplifier until the *BL* rises to V_{DD} and $\overline{BL}$ decreases to 0 V. The final bitline voltage, V_{DD}, is used to writeback the stored data to the memory cell as the access transistor, Q_c, is still activated.

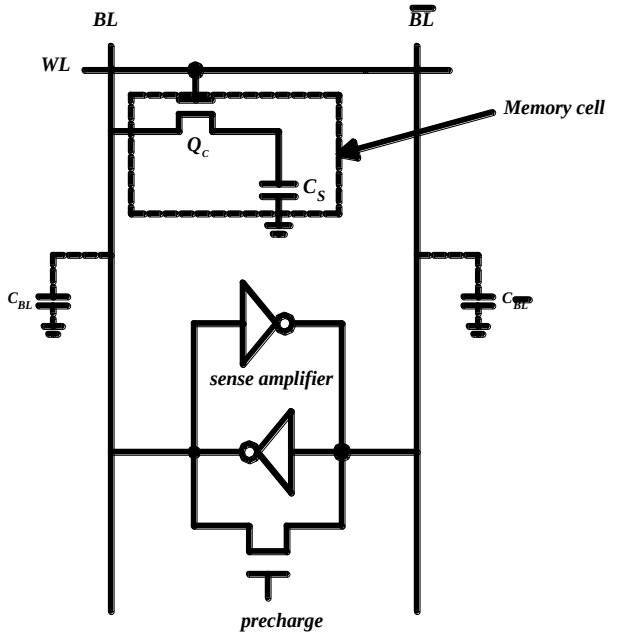


Fig. 2 The conventional reading scheme of the 1T-1C DRAM cell [7].

Had we assumed that the cell stores "0", the cell capacitor, C_s, is initially discharged to 0 V and thus upon charge sharing between C_{BL} and C_s, the bitline voltage, V_{BL}, will decrease from $V_{DD}/2$ to $V_{DD}/2 - \Delta V$. By virtue of the positive feedback effect of the sense amplifier, the bitline voltage finally decreases to 0 V which will also be used to writeback the stored data on the memory cell.

The steady-state voltages of the bitline can be found from the principle of charge conservation, that is; the charge lost by one capacitance equals that acquired by the other. In case of "1" storage, the cell capacitor, C_s, discharges from V_{DD} to V_{BL1} while C_{BL} charges from $V_{DD}/2$ to V_{BL1}. So, the amount of the charge lost by C_s is equal to that acquired by C_{BL}, i.e.

$$C_s\left[V_{DD} - V_{BL1}\right] = C_{BL}\left[V_{BL1} - \frac{V_{DD}}{2}\right] \quad (1)$$

$$V_{BL1} = \frac{C_s V_{DD} + C_{BL}\dfrac{V_{DD}}{2}}{C_s + C_{BL}}. \quad (2)$$

On the other hand, in case of "0" storage the capacitor, C_s, charges from 0 to V_{BL0} while C_{BL} discharges from $V_{DD}/2$ to V_{BL0}. So,

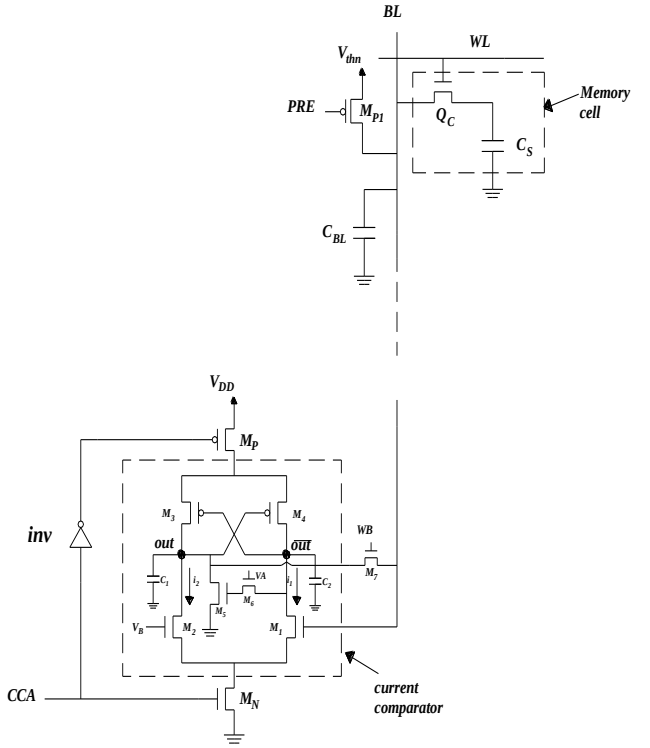
$$C_s\left[V_{BL0} - 0\right] = C_{BL}\left[\frac{V_{DD}}{2} - V_{BL0}\right] \quad (3)$$

$$V_{BL0} = \frac{C_{BL}\dfrac{V_{DD}}{2}}{C_s + C_{BL}}. \quad (4)$$

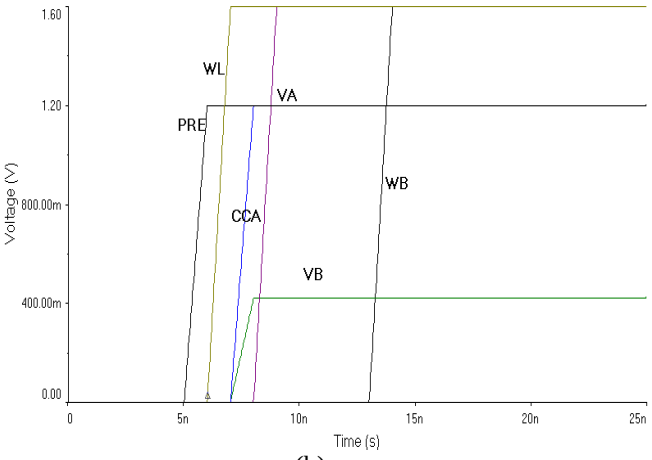
The main disadvantage of this reading scheme is the following: The output data will be available at the bitline after a relatively long time (21 ns according to our simulation for the 0.13 µm CMOS technology). This is due to the need to rise or decrease the voltage of the bitline parasitic capacitance, C_{BL}, which is relatively large (typically 256 fF for the 0.13 µm CMOS technology) due to its connection to the access transistors in all the memory cells in the columns (typically there are 128 cells in each column).

III. PROPOSED SCHEME

In this section, a current-mode readout scheme for reading the 1T-1C DRAM cell is presented. Refer to Fig. 3 (a) for the peripheral circuitry needed to precharge the bitline and read the stored data in each column and to Fig. 3 (b) for the timing diagram showing the synchronization of the employed signals. According to this technique, there will be no sense amplifier, however, there will be a current comparator. Basically, during the reading access, there will be a voltage signal generated on the bitline. This voltage signal will be converted to a current by M_1 that acts as a voltage-to-current converter. At the beginning of the reading access, the precharge signal, *PRE*, will be at logic "0", thus activating the PMOS transistor, M_{p1}. This will cause the bitline parasitic capacitance, C_{BL}, to precharge to V_{thn}. Note that the threshold voltage of the precharge transistor, M_{p1}, must be adjusted in order to allow conduction of the this transistor.



(a)



(b)

Fig. 3 (a) The circuit schematic of the peripheral circuitry of the current-mode readout scheme, (b) The timing diagram showing the signals, *PRE*, *WL*, V_A, V_B, *CCA*, and *WB*.

The wordline, *WL*, will be activated to a boosted voltage, $V_{DD} + V_{thn}$, thus activating the access transistor, Q_c, while the signal, V_A, is still at logic "0", thus deactivating M_6. If the cell stores "1", then its cell capacitor, C_s, will be initially charged to V_{DD}. So, C_s will lose some of its charge to C_{BL} through the access transistor, Q_c, as in the previous method. The final voltage on C_{BL} in case of "1" storage will thus be

$$V_{BL1} = \frac{C_s V_{DD} + C_{BL} V_{thn}}{\left(C_{BL} + C_s\right)}, \tag{5}$$

which is certainly larger than V_{thn}. Now, refer to the current comparator used at each column in the memory array instead of the sense amplifier which will be activated by the *CCA* (current-comparator activation) signal. It consists of four transistors, M_1, M_2, M_3, and M_4. M_1 and M_2 operate as voltage-to-current converters that convert their two gate voltages, V_{BL} and V_B, (the biasing voltage of M_2) into two currents, i_1 and i_2, respectively. The reference current, i_2, acts as a reference for comparison with i_1 that depends on the stored data. If the cell stores "1", then V_B is adjusted such that i_1 will be larger than i_2 for "1" storage, thus pulling the voltage at node $\overline{out}$ down and by the effect of the positive feedback caused by M_3 and M_4 the voltage at node *out* will be at V_{DD} which is the required output data.

On the other hand, if the cell stores "0", then due to the charge sharing between C_s and C_{BL}, V_{BL} will decrease from V_{thn} to

$$V_{BL0} = \frac{C_{BL} V_{thn}}{\left(C_{BL} + C_s\right)} \tag{6}$$

which is certainly lower than V_{thn}. So, i_1 will be zero except for the subthreshold-leakage current of M_1. If V_B is chosen to be larger than V_{thn}, then i_1 will be smaller than i_2 for "0" storage. So, the $\overline{out}$ node voltage will rise to V_{DD} and by the effect of the positive feedback of M_3 and M_4, the *out* node voltage will be decreased to 0 V as it must do.

The reading operation according to this method is obviously destructive. So, the stored data must be written back. This is in fact the role of the three transistors, M_5, M_6, and M_7. In order to write back the stored data, the two signals, V_A and *WB*, are activated. Obviously, if the read data is logic "1", then the voltage at $\overline{out}$ will be at 0 V. This causes the voltage at the gate of M_5 to be at 0 V, thus deactivating it. The read data will then be written back through M_7. Oppositely, if the read data is logic "0", then the voltage at $\overline{out}$ will be at V_{DD}. This activates the transistor, M_5, thus pulling down the voltage at node, *out*, to 0 V.

It must be noted that the connection of the transistor, M_5, not only contributes in writing back the read data, but also speeds-up the reading process and enhances the noise margin in case of "0" storage. In fact, if M_5 is eliminated, the data will be erroneously read in case of "0" storage. This point will be returned to in Section VI.

Specifically, in case of "0" storage, the voltage at node *out* will not be at precisely 0 V. Instead, it will be at a voltage that is higher than 0 V which is considered a poor "0". This is due to the continuous conduction of M_2 by the biasing voltage source, V_B, with the result that M_3 and M_2 form a voltage divider. This causes not only the noise margin to be poor in case of "0" storage, but also there will be a short circuit current through the M_p-M_3-M_2-M_N branch, thus increasing the power consumption associated with reading "0". Pulling down the voltage at *out* by increasing the voltage, V_B, has a deleterious effect in case of reading "1" as the current, i_2, will be larger than i_1 in case of reading "1" or smaller than it by a slight amount. However, with the connection of M_5, the V_{DD} voltage at the $\overline{out}$ node activates the transistor, M_5, thus pulling down the voltage at node *out* to perfect 0 V.

Speeding-up the reading process in case of "0" storage id due to the following: When the voltage at $\overline{out}$ increases, the voltage at *out* decreases further by the effect of *M*. This causes the PMOS transistor, M_4, to charge the parasitic capacitance, C_2, at node $\overline{out}$. This positive-feedback effect results in faster operation.

A word of caution here concerning the instant of time at which the *WB* signal is activated is in order. If this signal is activated earlier than necessary, the voltage at node *out* will not rise to V_{DD} in case of reading "1"; instead it will discharge through M_7 resulting in wrong output data.

It should be noted that the read data cannot be written back by the use of a single NMOS transistor connected between the node *out* and the bitline. This is due to that in the case of stored "1", the bitline parasitic capacitance, C_{BL}, will discharge to 0 V through the series connection of the fictitious write-back transistor and M_2, thus resulting in an erroneous output. However, in case of stored "0", both C_{BL} and C_1 discharge through the same path resulting in correct reading and write back. As a final remark on this scheme, any other current comparator can be used. Also, there will be no need to use an equalization circuitry or dummy cells as in the conventional scheme.

IV. QUANTITATIVE ANALYSIS

In this section, the proposed scheme will be analyzed quantitatively seeking to discuss the range within which we can choose the biasing voltage, V_B, along with the optimum value for this voltage, V_{Bopt}.

The Optimum Value of the Biasing Voltage, V_B

From the qualitative discussion of the proposed readout scheme in Section III, it is apparent that the biasing voltage, V_B, must be chosen such that the current flowing through M_2, i_2, is larger than that flowing through M_1, i_1, in case of "0" storage and smaller than i_1 in case of "1" storage. A quick look at the circuit of the proposed scheme may reveal that a suitable value for V_B is V_{thn} as the voltage to which the bitline, *BL*, is initially precharged is V_{thn}. However, the simulation results contradict with this guess and prove that $V_B = V_{thn}$ is not a right choice as the stored "0" will be misread.

The reason behind this is that the voltage difference between the bitline parasitic capacitance, C_{BL}, and the storage capacitor, C_s, in case of stored "1" is larger than that in case of stored "0". In the former, it is V_{DD} - V_{thn} while in the latter it is V_{thn}. So, the differential voltage signal appearing on the bitline in case of stored "1" will certainly be larger than that in case of stored "0". This can be quantified by the following equations:

$$V_{BL1} = \frac{C_s V_{DD} + C_{BL} V_{thn}}{C_s + C_{BL}} \tag{7}$$

$$V_{BL0} = \frac{C_{BL} V_{thn}}{(C_{BL} + C_s)}. \tag{8}$$

Eqs. (7) and (8) for the final values of the bitline voltages in case of stored "1" and stored "0", respectively. Refer to Fig. 4 for illustration.

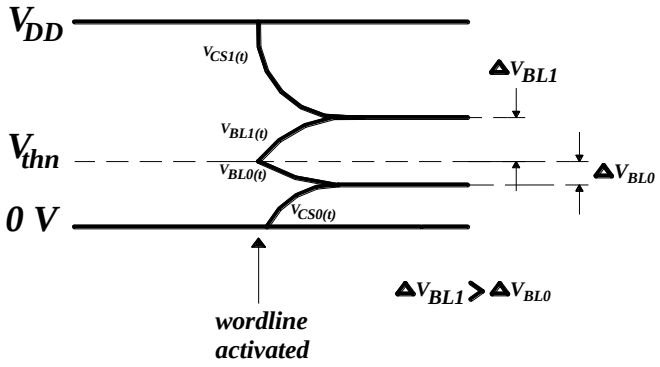


Fig. 4 A qualitative plot showing the change of the voltages across the bitline parasitic capacitance, V_{BL}, and the cell storage capacitor, V_{Cs}, in case of stored "1" and stored "0" upon charge sharing between C_{BL} and C_s. Note the larger change in case of stored "1" (The graph is not to scale).

Consequently, it is expected that V_B must be larger than V_{thn} in order to compensate for this difference. This must be compared to the conventional readout method in which the other input terminal of the sense amplifier is connected to a voltage of $V_{DD}/2$ through say a dummy cell [1].

The key point behind the determination of the optimum value for V_B, V_{Bopt}, is the following statement: The sum of the differences between the reference current and the two currents generated from M_1 in case of stored "1" and "0" is maximized and these two differences are equalized. Toward this target, the reference current, i_2, will be put equal to the arithmetic average of the two currents passing through M_1 in case of "1" storage, i_{11}, and "0" storage, i_{10}, respectively, that is

$$i_2 = \frac{i_{11} + i_{10}}{2} \tag{9}$$

Since in case of stored "0", V_{BL0} will be smaller than V_{thn}, i_{10} will ideally be zero. However, in case of stored "1", V_{BL1} will be slightly larger than V_{thn}, so M_1 will certainly operate in the saturation region since its V_{DS} will be larger than its overdrive voltage, V_{GS} - V_{thn}. So,

$$i_{11} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_1 \left[V_{BL1} - V_{thn}\right]^2 \tag{10}$$

where the channel-length modulation effect is neglected. The final voltage on the bitline in case of stored "1" can be found using the principle of charge sharing as discussed in Section II to be

$$V_{BL1} = \frac{C_s V_{DD} + C_{BL} V_{thn}}{C_{BL} + C_s} \quad . \tag{11}$$

Substitution of this value for V_{BL1} into Eq. (10) results in

$$i_{11} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_1 \left[\frac{C_s V_{DD} + C_{BL} V_{thn}}{C_{BL} + C_s} - V_{thn}\right]^2$$

$$i_{11} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_1 \left[\frac{C_s V_{DD} + C_{BL} V_{thn} - C_{BL} V_{thn} - C_s V_{thn}}{C_{BL} + C_s}\right]^2$$

$$\therefore i_{11} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_1 \left[\frac{C_s (V_{DD} - V_{thn})}{C_{BL} + C_s}\right]^2 \tag{12}$$

So, the reference current will be chosen to be

$$i_2 = \frac{i_{11} + i_{10}}{2} = \frac{i_{11}}{2} \tag{13}$$

$$\therefore \frac{1}{2} k_n' \left(\frac{W}{L}\right)_2 \left[V_{Bopt} - V_{thn}\right]^2 = \frac{1}{4} k_n' \left(\frac{W}{L}\right)_1 \left[\frac{C_s (V_{DD} - V_{thn})}{C_{BL} + C_s}\right]^2$$

After simple mathematical manipulations, we can obtain

$$V_{Bopt} = V_{thn} + \sqrt{\frac{1}{2} \frac{(W/L)_1}{(W/L)_2}} \left[\frac{C_s (V_{DD} - V_{thn})}{C_{BL} + C_s}\right]. \tag{14}$$

For the 0.13 µm CMOS technology which is adopted in the simulation in this thesis, V_{DD} = 1.2 V and V_{thn} = 0.4 V. Considering C_s and C_{BL} to be equal to 10 fF and 250 fF, respectively and assuming that $(W/L)_1 = (W/L)_2$, we obtain upon substitution into Eq. (14),

$$V_{Bopt} = 0.4217 \text{ V}.$$

If the same parameters that are used in computing V_{Bopt} were used in computing V_{BL0} and V_{BL1}, we will get V_{BL0} = 0.384 V and V_{BL1} = 0.43 V. It is obvious that V_{Bopt} is not equal to the arithmetic average of V_{BL0} and V_{BL1}. This is an expected result since the reference current, i_2, is equal to the arithmetic average of the two currents generated through M_1 in case of stored "1" and stored "0" and these two currents are not linearly related to the corresponding gate voltages. Instead, there is a square-law dependence.

Finally, it should be noted that the speed of this scheme is more sensitive to the change in C_s than the conventional scheme as increasing C_s causes the current, i_1, to increase significantly due to the square-law dependence.

V. IMPACT OF TECHNOLOGY SCALING

1. Reduction of the V_{DD}/V_{thn} Ratio

Due to the need to reduce the dynamic power consumption and enhance the reliability of short-channel devices, the power-supply voltage, V_{DD}, reduces at a rate that is faster than that of V_{thn} from one technology generation to the next [8]. So, the ratio V_{DD}/V_{thn} decreases. Since C_{BL} is precharged to V_{thn} instead of $V_{DD}/2$, the percentage of the precharging time interval relative to the total access time is expected to increase. However, it remains below the precharging time interval of the conventional scheme in which C_{BL} is initially precharged to $V_{DD}/2$ as soon as V_{thn} remains below $V_{DD}/2$. The precharging time interval, however, of the conventional scheme remains the same as V_{DD} and the precharge level decreases by the same ratio from one technology generation to the next. If the V_{DD}/V_{thn} ratio reaches 2, then $V_{DD}/2$ will be equal to V_{thn} and the precharging time delays of the conventional and proposed readout schemes will be the same. Also, the need arises in this case to adjust the threshold voltage of the precharging PMOS transistor in the conventional scheme.

To investigate the impact of the reduction of the V_{DD}/V_{thn} ratio on the ratio between the two sense margins in case of "0" and "1" readings, SM_0 and SM_1, respectively, refer to Eqs. 9 and 6 for V_{BL1} and V_{BL0}. They will be repeated here for convenience.

$$V_{BL1} = \frac{C_s V_{DD} + C_{BL} V_{thn}}{C_s + C_{BL}} \tag{15}$$

$$V_{BL0} = \frac{C_{BL} V_{thn}}{(C_{BL} + C_s)}. \tag{16}$$

So, the sense margins in case of "1" and "0" readings will be

$$SM_1 = \Delta V_{BL1} = V_{BL1} - V_{thn} = \frac{C_s (V_{DD} - V_{thn})}{C_s + C_{BL}} \tag{17}$$

and

$$SM_0 = \Delta V_{BL0} = V_{thn} - V_{BL0} = \frac{C_s V_{thn}}{C_s + C_{BL}}, \tag{18}$$

respectively. The ratio between SM_1 and SM_0 is thus

$$\frac{SM_1}{SM_0} = \frac{C_s (V_{DD} - V_{thn})}{C_s V_{thn}} = \frac{V_{DD}}{V_{thn}} - 1. \tag{19}$$

So, with technology scaling, the ratio between SM_1 and SM_0 decreases until we arrive at the case $V_{DD} = 2V_{thn}$ at which the two sense margins are equal. In fact, this case corresponds to precharging the bitline to $V_{DD}/2$ as in the conventional scheme. Refer to Fig. 5 for illustrating the impact of technology scaling on SM_1 and SM_0.

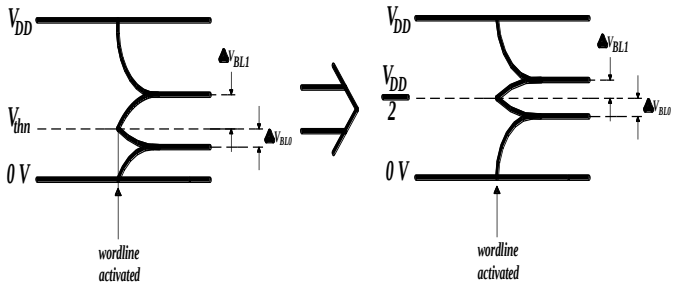


Fig. 5 The effect of the reduction of the V_{DD}/V_{thn} ratio on the sense margins of "1" and "0" readings, SM_1 and SM_0, in the proposed method. Note the equalization of the sense margins, SM_1 and SM_0, with technology scaling.

2. Velocity Saturation and Mobility Degradation

Due to the velocity saturation, the drain current will no longer be related to the gate-to-source voltage through a square law. However, it will be related to V_{GS} through the following relationship [9]:

$$i_D = K\left[V_{GS} - V_{thn}\right]^{\alpha} \tag{20}$$

where K is a parameter that depends on the CMOS technology and the device dimensions and is equal to 2 in long-channel MOSFETs with channel lengths longer than typically 1µm. If we proceed with the analysis of Section IV concerning the determination of V_{Bopt}, the following two currents will be obtained in response to V_{BL0} and V_{BL1};

$$i_{11} = K\left[V_{BL1} - V_{thn}\right]^{\alpha} \tag{21}$$

and

$$i_{10} = 0. \tag{22}$$

If the two transistors, M_1 and M_2, have different sizes, then the drain current can be related to the device dimensions through

$$i_{11} = K_1\left(\frac{W}{L}\right)_1\left[V_{BL1} - V_{thn}\right]^{\alpha} \tag{23}$$

where K_1 is a parameter that depends on the CMOS technology. So,

$$i_{11} = K_1\left(\frac{W}{L}\right)_1\left[\frac{C_s V_{DD} + C_{BL} V_{thn}}{C_{BL} + C_s} - V_{thn}\right]^{\alpha}$$

$$i_{11} = K_1\left(\frac{W}{L}\right)_1\left[\frac{C_s V_{DD} + C_{BL} V_{thn} - C_{BL} V_{thn} - C_s V_{thn}}{C_{BL} + C_s}\right]^{\alpha}$$

$$\therefore i_{11} = K_1\left(\frac{W}{L}\right)_1\left[\frac{C_s\left(V_{DD} - V_{thn}\right)}{C_{BL} + C_s}\right]^{\alpha}. \tag{24}$$

So, the reference current will be

$$i_2 = \frac{i_{11} + i_{10}}{2} = \frac{i_{11}}{2}$$

$$\therefore K_1\left(\frac{W}{L}\right)_2\left[V_{Bopt} - V_{thn}\right]^{\alpha} = \frac{1}{2}K_1\left(\frac{W}{L}\right)_1\left[\frac{C_s\left(V_{DD} - V_{thn}\right)}{C_{BL} + C_s}\right]^{\alpha}$$

$$\therefore V_{Bopt} = V_{thn} + \left(\frac{1}{2}\frac{(W/L)_1}{(W/L)_2}\right)^{\alpha}\left[\frac{C_s\left(V_{DD} - V_{thn}\right)}{C_{BL} + C_s}\right] \tag{25}$$

α is typically 1.3 in short-channel devices. Substituting this value for α in Eq. (25) and assuming the same values for C_s and C_{BL} as that substituted in Eq. (14) along with the assumption of $(W/L)_1 = (W/L)_2$ results in

$$V_{Bopt} = 0.424 \text{ V},$$

which is far from the arithmetic average of V_{BL1} and V_{BL0} than the value obtained in the analysis of Section IV assuming long-channel devices.

VI. SIMULATION RESULTS

The proposed reading scheme is simulated for the 0.13 µm CMOS technology with V_{DD} =1.2 V using Multisim 11. The simulation results for this scheme are shown in Figs. 6 and 7 for stored "1" and stored "0", respectively. Shown in these figures are the voltages across the cell capacitor, V_{Cs}, across the bitline parasitic capacitance, V_{BL}, and the voltages at the *out* and $\overline{out}$ nodes with the biasing voltage source, V_B, put equal to 0.42 V. Also, shown in Fig. 8 are the simulation results for stored "0" when the transistor, M_5, is not connected. Note that the voltage at node *out* will not be perfectly 0 V. The access time is approximately 18 ns compared to 20 ns for the conventional scheme. The, the power-delay products in case of reading "1" (the worst case from the point of view of PDP) are 388.5 fJ and 188 fJ for the conventional and proposed schemes, respectively.

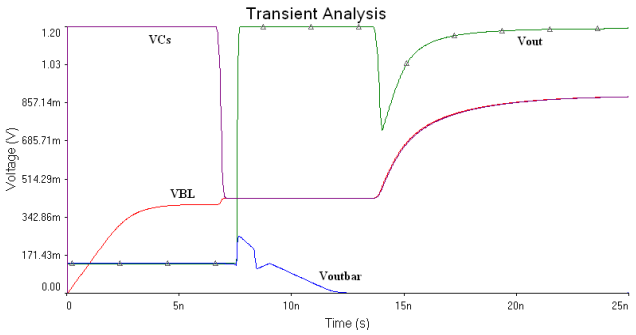


Fig. 6 The simulation results showing the voltages across the cell capacitor, the bitline parasitic capacitance, at the *out* and $\overline{out}$ nodes for stored "1".

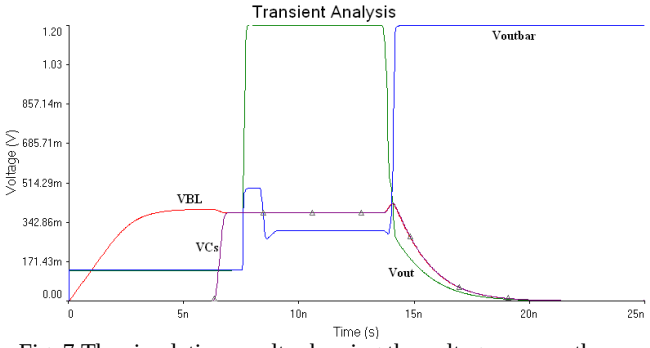


Fig. 7 The simulation results showing the voltages across the cell capacitor, the bitline parasitic capacitance, at the *out* and $\overline{out}$ nodes for stored "0".

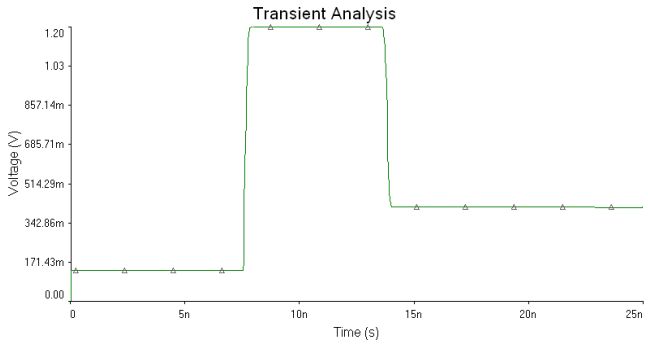


Fig. 8 The simulation results showing the voltage at the node, *out*, for stored "0" when the transistor, M_5, is eliminated which is an erroneous output data.

VII. CONCLUSIONS

There is no doubt that, dynamic RAMs play a significant role in all computing and control devices. The conventional reading process of one-transistor one-capacitor dynamic RAMs requires the use of a sense amplifier that compares between the bitline voltage and the dummy bitline voltage, then amplifying the voltage difference between them. However, this takes a relatively long time. In this paper, a novel reading technique was proposed. This technique depends on converting the voltage change generated on the bitline due to charge sharing between C_s and C_{BL} to a current change and using a current comparator instead of the sense amplifier in order to speed-up the operation. The access time is approximately 18 ns compared to 20 ns for the conventional scheme. The, the power-delay products in case of reading "1" (the worst case from the point of view of PDP) are 388.5 fJ and 188 fJ for the conventional and proposed schemes, respectively.

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