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Analysis of Thyristor Controlled Series Capacitor Application in Fault Current Limiter Mode

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Abstract:

The present paper describes and analyzes the mechanism and extent by which the Thyristor Controlled Series Capacitor (TCSC) may be applied to limit fault currents through developing high inductive impedance under fault conditions. The transition to and from normal operating conditions and fault current limiting mode of TCSC is analyzed beside its original function as a flexible ac transmission system device under PSCAD/EMTDC and MATLAB environments. The fault current limiting performance of TCSC is compared against that of a static synchronous series compensator (SSSC) applied to the same system under study.

Key words: FCL, TCSC and SSSC

ملخص: تقدم الورقة البحثية وصفاً وتحليلاً لأسلوب وحدود إستخدام إحدى نبائط خطوط النقل المرنة "مكثف التوالى المتحكم بالثيرستور" للحد من قيمة تيار القصر بولسطة توفير معاوقة حثية عالية فى حالات القصر. وقد تم تحليل حالات الإنتقال المختلفة من ظروف التشغيل المعتادة ووظائف نبيطة خطوط النقل المرنة وإلى وضع الحد من تيار القصر وبالعكس. وقد تم مقارنة أداء مكثف التوالى المتحكم بالثيرستور بأداء معوض التوالى المتزامن الساكن فى حالة الحد من قيمة تيار القصر.

I. Introduction

In order to meet load demands in complex interconnected power systems while satisfying both stability and reliability criteria, existing transmission lines should be efficiently utilized through the use of power-electronics based power-system controllers known as Flexible AC Transmission Systems (FACTS). On the other side, fault current limiters [1,2] are required for overcoming expansion associated increased short circuit levels. Thyristor controlled series compensator, (TCSC), a FACTS device that combines conventional series capacitor with thyristor controlled reactor (TCR) to allow continuous control of its reactance, is already used for power flow control, transient / dynamic compensation, sub-synchronous resonance mitigation [3]. The function of TCSC may also be extended to limit fault currents by adjusting their impedance dynamically to a large inductive value. The main objective of this paper is to demonstrate in details the design, implementation and application boundaries of thyristor controlled series capacitor in fault current limiting mode.

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The usual and extended modes of operation of TCSC in normal and abnormal power system conditions have been simulated under PSCAD/EMTDC environment [4]. The model is further validated under MATLAB environment [5]. A comparative study to the performance of SSSC [6] in fault current limiting mode is conducted to illustrate the importance of TCSC application as a fault current limiter.

II. TCSC BASIC MODES OF OPERATION

The simplified circuit of a single module TCSC shown in Fig. 1 comprises a resonant circuit; a thyristor controlled reactor in parallel with a capacitor.

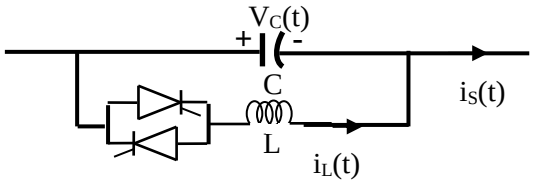


Figure 1 TCSC simplified circuit

There are three basic modes of operation, namely: thyristor blocked mode (TB), thyristor switched reactor (TSR) or thyristor fully conducting, and thyristor operating in phase controlled mode (TPC). In TB mode, firing pulses are inhibited and the TCSC behaves as a single series capacitor

bank with all transmission line current passing through the capacitor. In TSR, the thyristor valve(s) is continuously fired, so most of the line current flows through the TCR and consequently the TCSC develops inductive impedance. This mode provides the means of limiting the line current by increasing the line impedance by a value that depends on the design of the TCSC. The criterion for such a design can be found in [7]. The TSR mode is thus suitable with minor design modifications for limiting fault current in power systems to a certain extent. In TPC mode, thyristor switches operate with phase control of the firing signal. Consequently partial conduction is established and the fundamental current passing through the bi-directional thyristor valve is effectively controlled. Depending on the magnitude of this current, the TCSC may present either a capacitive or inductive net reactance. A small current circulating in the reactor results in a net capacitive reactance which is greater than that of the capacitor alone. On the contrary, TCSC operation with a high level of thyristor conduction results in a reversed circulating current and a net inductive reactance greater than that of the reactor alone [8,9]. In case the steady state resonance region is avoided, the control mode is known as vernier control. The fundamental operational feature of all FCL is their ability to switch rapidly from a normal low-impedance conducting state to a high-impedance current-limiting state in case of faults. FCL must discriminate between three classes of events, short-term disturbances, such as lightning strikes, low-level faults, which are within the rating of existing breakers; and high level faults, which require current limiting action.

III. Sizing of TCSC components

To illustrate the extended performance of TCSC, the radial system used in [3] was adopted as shown in Fig. 2.

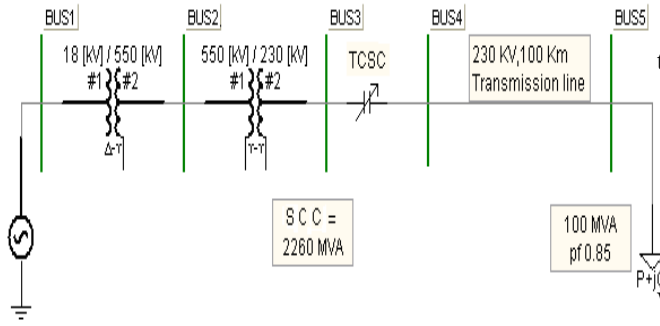


Figure 2 Radial test system [3]

It comprises an equivalent source (generator, 18/550 kV step-up transformer, autotransformer 550/230 kV), and a 230 kV, 100 km transmission line that feeds a 100 MVA, 0.85 power factor load. The short circuit capacity at bus 3 (point-of-common coupling of a sensitive load) is around 2,260 MVA.

The inductive reactance of the transmission line was found to equal 0.458 Ω/km per phase. Based on design criteria [7], typical values of both of the capacitive and inductive VARs of the TCSC are selected to be 2.097 and 0.43 MVAR respectively.

IV. Analysis of TCSC

The analysis of TCSC operation in the vernier-control mode is performed based on the simplified TCSC circuit shown in Fig. 1. Transmission-line current is assumed to be the independent-input variable modeled as an external current source; $i_S(t)$. It is further assumed that the line current is sinusoidal, as derived from actual measurements demonstrating that very few harmonics exist in the line current [10,11]. The firing angle "**α**" is generated using a reference signal that can be in phase with the capacitor voltage. Relations of capacitor and thyristor valve currents according to switching status "u" are expressed by the following equations [12]:

$$C\frac{dV_C(t)}{dt} = i_S(t) - i_L(t).u$$

$$L\frac{di_L(t)}{dt} = V_C(t).u$$

Where $i_L(t)$ is the instantaneous current passing through the inductance "L", and $V_C(t)$ is the instantaneous value of the voltage across the capacitor "C".

According to the instants of switching per cycle; $\frac{\alpha}{\omega}$ and $\frac{\beta}{\omega}$, where β = π-α is the angle of advance, the steady state thyristor current $i_T(t)$ is given by:

$$i_T(t) = \frac{k^2}{k^2-2} I_m \left[\cos\omega t - \frac{\cos\beta}{\cos k\beta} \cos\omega_r t \right]; \qquad -\beta \le \omega \le \beta$$

Where $\omega_r = \frac{1}{\sqrt{LC}}$ and $k = \frac{\omega_r}{\omega} = \sqrt{\frac{x_C}{x_L}}$ as x_C is the nominal reactance of the fixed capacitor.

The capacitor's voltage is given by:

$$V_C(t) = \frac{I_m x_C}{k^2-1} \left(-\sin\omega t + k\frac{\cos\beta}{\cos k\beta} \sin\omega_r t \right); \qquad -\beta \le \omega t \le \beta$$

The equivalent reactance of TCSC; X_T is given by

$$X_T = x_C - \frac{x_C^2}{(x_C - x_L)\pi}\left[2\beta + \sin 2\beta + \frac{4(k\tan k\beta - \tan\beta)\cos^2\beta}{k^2 - 1}\right]$$

The variation of TCSC per unit reactance as a function of firing angle α is illustrated in Fig. 3.

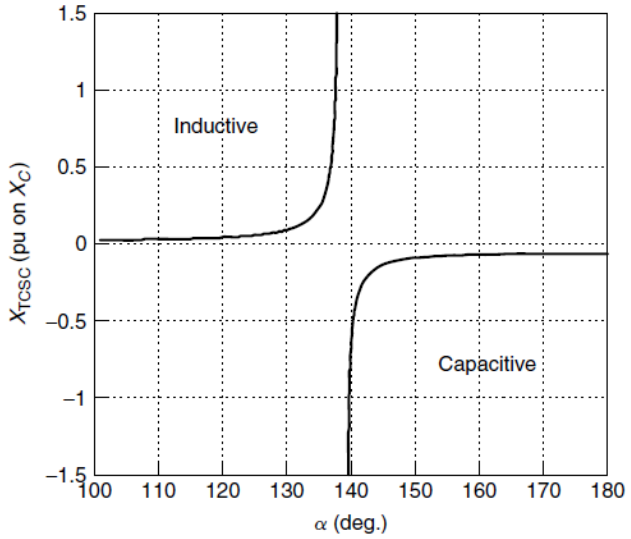


Figure 3 Reactance of TCSC versus firing angle 'α' [12]

Parallel resonance is thus created between X_L and X_C at the fundamental frequency corresponding to the values of firing angle α_{res} given by

$$\alpha_{res} = \pi - (2m-1)\frac{\pi\omega}{2\omega_r}; \qquad m = 1,2$$

The different resonances can be reduced to one by a proper choice of "k" in the range 90°<α <180°. At the resonant point, the TCSC exhibits very large impedance and results in a significant voltage drop.

During TCSC operation in its normal modes, this resonant region is avoided by installing limits on the firing angle. For the values of parameters adopted in the present paper, the typical value of the firing angle resulting in resonance is found to equal 145°.

V. TCSC as a Fault current limiter

Single line to ground short circuits is applied along line **4-5.** The fault location was varied in increments of **10 km** in order to evaluate the provided current limit extent. The TCSC may be used for limiting fault current by adjusting its impedance dynamically to a large inductive value that depends upon the TCSC design. Decision of operation in the FCL mode is dependent on the result of comparing the line current with a simulated fault current signal, the phase and magnitude of which are adjusted to represent the largest value the controller should allow without activating FCL mode.

Phase locked loop (PLL) is applied to provide a reference phase signal synchronized with the ac system voltage. Such signal is further used as a basic carrier wave for deriving valve firing pulses to ensure that transients and distortion in system voltage do not impair TCSC control system performance.

In pre fault condition, the TCSC is operating either in capacitive vernier mode or in by pass mode based on the power system's conditions. At fault conditions, the control system senses and discriminates between classes of faults to avoid activating fault current limiting mode for lower level faults that can be handled by existing breakers. During the FCL mode, each phase of the TCSC is separately controlled according to the different fault types. The firing angle 'α' should be set between 90° and 141°. Normal FCL operation in inductive mode where high inductive impedance is introduced in series to the transmission line increases the total impedance seen by the fault and results in decreasing fault current level. To illustrate the necessity of modifying the TCSC for extending operation in FCL mode, different types of faults at different line locations are applied.

Fig. 4 shows the operation of single and multiple modules of TCSC at different current limiting depth. At the verge of the FCL mode (at 90° delay for the used values) for a single line to ground fault at 0.1 sec at a distance of 80 km from bus 4, the available fault current limiting action in cases with a single module is found to be in the order of 10%, which is deemed unsatisfactory.

If the firing angle 'α' is set close to but not venturing through resonance region; the full extent of the inductive mode is attained, which results in a further reduction of fault current levels. Nevertheless, such achievement comes on behalf of increased harmonics. Further appreciable fault current limiting action without risky need to approach resonance region may be attained by adopting independently operated multiple modules TCSC, where smooth variation of reactance is reachable.

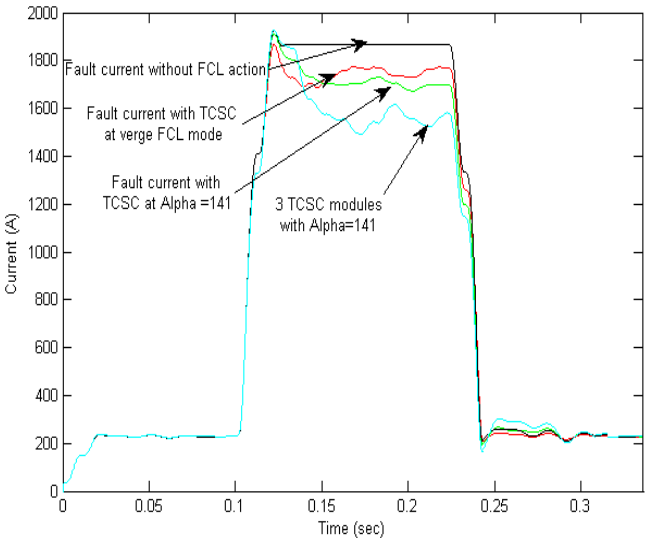


Figure 4 TCSC modules responses for fault at 80Km

Fig. 5 and Fig. 6 show the currents flowing in the inductor and capacitor respectively during FCL mode. The currents wave shapes are in accordance with the expected high harmonic content.

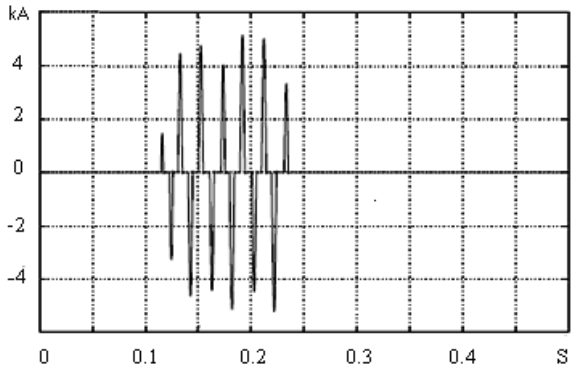


Figure 5 Inductor current versus time in FCL mode.

The TCSC capacitor itself partially acts as a filter with respect to the rest of the system. Furthermore, high harmonics produced during fault current limiting mode are of very low rate of occurrence, and fault duration is limited as well. In which case, the outcomes of this mode are in accordance with standards regarding short duration harmonics [1].

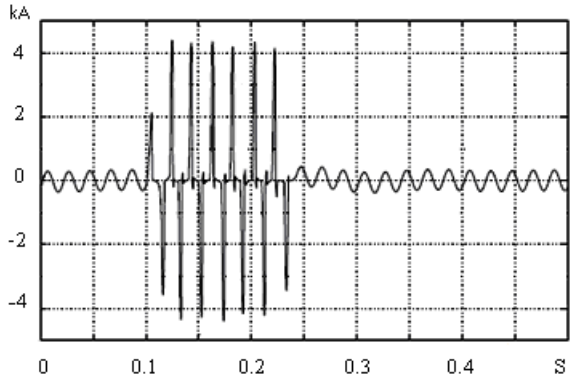


Figure 6 Capacitor current versus time in FCL mode

A metal oxide varistor (MOV) [13, 14], modeled as a nonlinear resistor, is connected across the series capacitor to prevent the occurrence of high over-voltages. Fig. 7 illustrates the basic MOV protective characteristics.

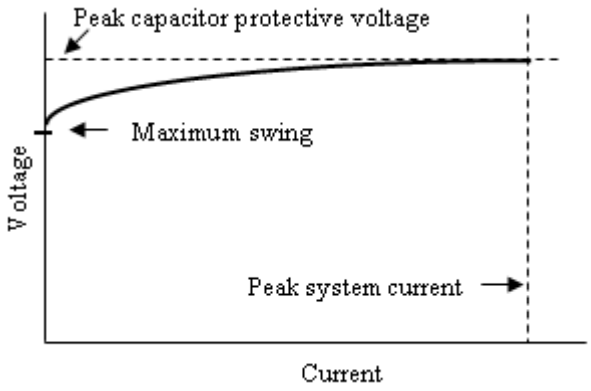


Figure 7 MOV protection characteristics [13]

By limiting the voltage across the capacitor, the MOV allows the capacitor to remain in the circuit during fault conditions and helps improve the transient stability. Both of the capacitor's voltage and MOV current are traced during TCSC compensating and FCL modes. The effect of MOV on capacitor voltage is accordingly analyzed. During steady state TCSC operating modes other than fault current limiting mode, the MOV doesn't have significant effect, as the current passing through the MOV is minimal.

Fig. 8 and Fig.9 shows the capacitor's voltage and MOV current versus time in thyristor blocked mode and fault current limiting mode respectively.

The resulting capacitor voltage shows that the MOV prevents over-voltages on capacitor by acting as a non linear resistance. Furthermore, stresses across the capacitor are readily decreased within and during transitions between operating modes. The resistance decreases with the increase in the voltage across the capacitor above certain level, which justifies the flow of high current through the MOV. During fault conditions, the current passing through the MOV is limited by the virtual rise of inductive reactance's value.

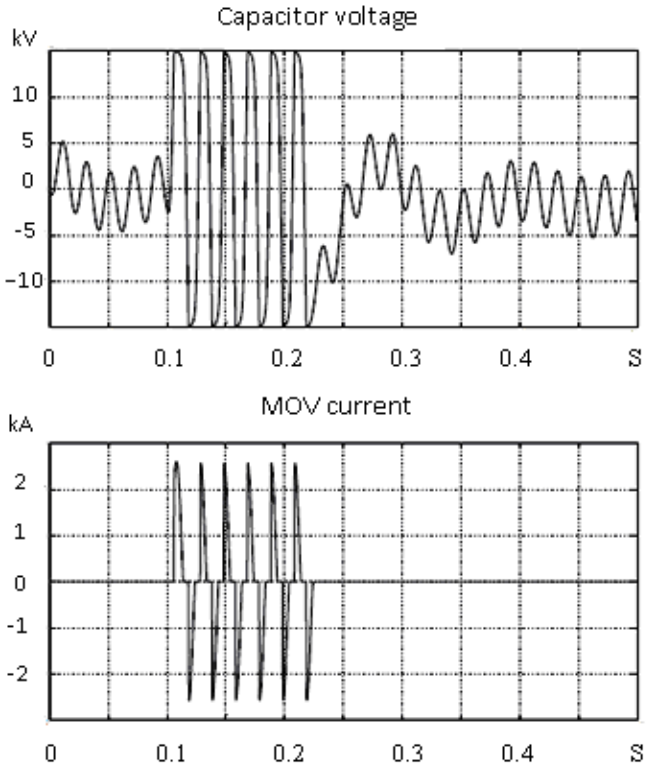


Figure 8 Capacitor voltage and MOV current versus time during thyristor blocked mode

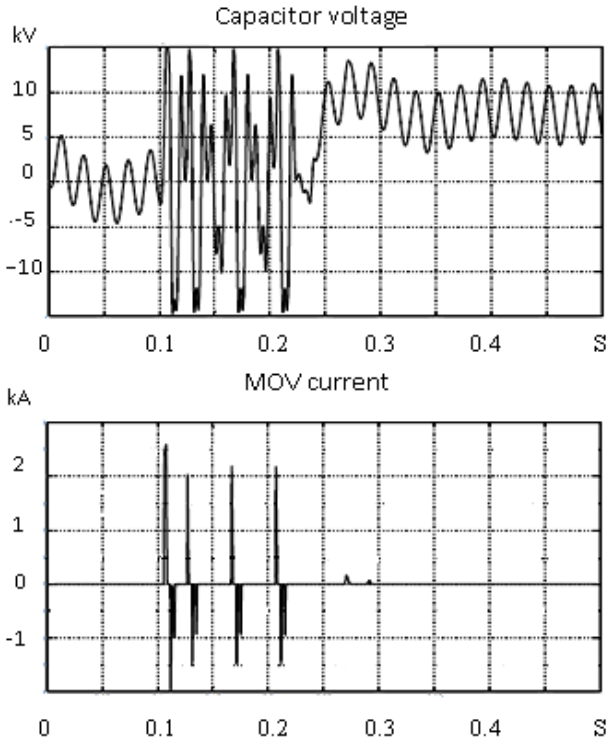


Figure 9 Capacitor voltage and MOV current versus time during FCL mode

VI. SSSC as a Fault Current Limiter

To illustrate the adequacy of applying the TCSC in FCL mode, another series FACTS devices already probed in such mode [15,16,17] should be considered. The Static Synchronous Series Compensatore, SSSC, composed of phase shifting transformer, a synchronous voltage source (SVS) and dc storage capacitor, is shown in Fig.10.

The SVS can produce a set of almost sinusoidal voltages at the desired fundamental frequency with controllable amplitude and phase angles. Accordingly, when connected in series with the transmission line, the injected voltage in quadrature with the line current emulates inductive or capacitive reactance in series with the line, and reactive power is either generated or absorbed. The SSSC is controlled to compensate reactance of transmission line to enhance steady state stability of power system.

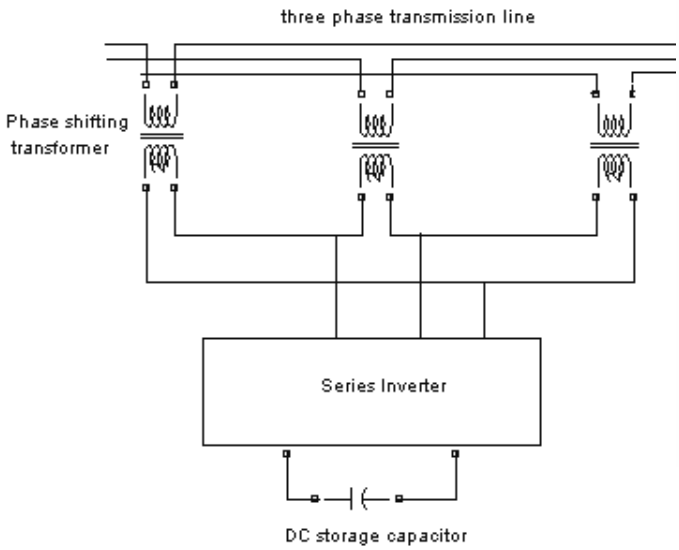
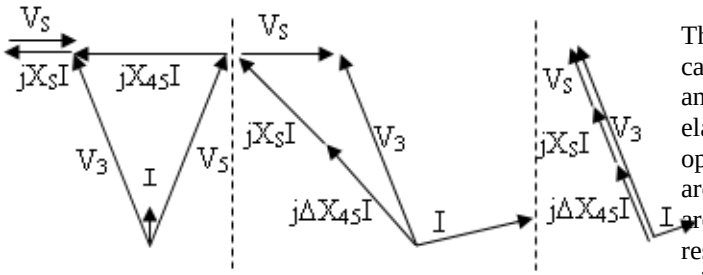


Figure 10 Static Synchronous Series Compensatore

Inserting SSSC instead of TCSC in the present test system, and controlling the SSSC to act as a pure virtual inductor causes operation in its FCL mode. Voltage and current vectors for pre-fault, fault onset and current limiting SSSC conditions are shown in Fig.11. At the time of short circuit, if voltage 'V_S' injected by the SSSC is maintained to be equal to its value before instant of short circuit, the vectors of voltage and current will be as shown in Fig. 9b. This injected voltage is insignificant compared with the voltage across the leakage reactance of SSSC. Avoiding the existence of a resistive component in the virtual impedance is necessary as it causes the SSSC to absorb real power during fault compensation and consequently charge the dc capacitor bank leading to a damaging condition with large fault current flow. As shown in Fig. 12 and Fig. 13, applying the same fault/location patterns with SSSC, it is found that the fault current limiting action of SSSC slightly surpasses that of TCSC.



(a) Pre fault **(b) Fault onset mode** **(c) FCL**

Figure 11 Voltages and currents of SSSC

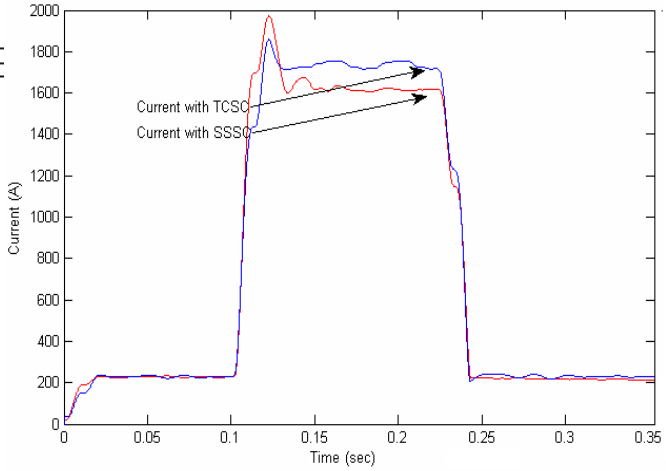


Figure 12 SSSC and TCSC responses for fault at 80Km

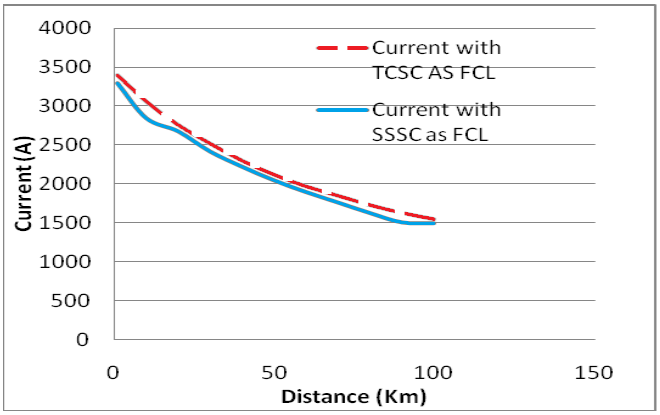


Figure 13 Fault currents for faults at different locations along the transmission line with TCSC and SSSC

VI. CONCLUSIONS

The performance of a traditional thyristor controlled series capacitor with additional fault current limiting function is analyzed and its principle of operation is thoroughly elaborated. Transitions between different modes of operation have been simulated and the associated responses are traced. The same test system and operating conditions are used with a static synchronous series compensator. The results proved that the TCSC fault current limiting action without the least component sizing modification is not so far from that of an SSSC. Taking higher SSSC cost into account, the TCSC may be assumed an equal choice for FCL operation compared to SSSC. Considering the short duration of fault current limiter operation, together with the low occurrence of faults in the first place, the effect of harmonics associated with TCSC fault current limiting mode is assumed to be tolerable. Furthermore, as the SSSC already requires harmonic filters, the limited need for

harmonic mitigation with TCSC in FCL mode either through filters or modulation control doesn't negatively affect the comparison.

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