

Design of low quiescent current LDO voltage regulator for portable electronic devices

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Abstract

Low dropout linear voltage regulators are analog circuit blocks that play an important role in power delivery process and prevent a system from fluctuations in the supply rails. There is a high demand on using LDO regulator in system-on-chip (SOC) applications, given their inherently noisy environment. This work presents a design of low dropout voltage regulator (LDO) to satisfy desired parameters. Basic design parameters of the proposed LDO CMOS circuit are introduced. The proposed circuit is designed to achieve a low quiescent current and dropout voltage as well as large PSRR value as possible, while maintaining the stability is paramount. Simulation results of the proposed circuit using 180 nm process CMOS technology and its corner analysis are presented. The simulation of the proposed LDO design achieves low quiescent current in the range of microamperes.

I. INTRODUCTION

Nowadays, there is an increase demand in the industry for a power management System-on-Chip (SoC) for battery-powered applications^[1-3]. LDO regulators over a constant and stable output voltage independent of the load impedance, temperature and even the time required for battery discharges. One of the advantages of LDO is it can operate at lower supply voltages with a rather low dropout voltage, and provide multiple voltage levels. LDOs are also capable of minimizing current consumption down to microamperes, which is crucial for current consumption of the sub-blocks in sleep mode^[4].

This paper presents an LDO voltage regulator designed in 180 nm process with GPDK180 process design kit. It produces a 1.5 V output voltage for all load conditions. The load current ranges from 10 μ A to 1 mA with 10% error. A 1 μ F output capacitor is added on the output for the regulator stability. The output capacitor equivalent series resistance (ESR) ranges from 10 m Ω to 300 m Ω .

In the next sections, a design of LDO voltage regulator is presented. It works in a temperature ranges from -50°C to 100°C , which is in between industrial, and military temperature grades. The input voltage ranges from 1.7V to 2 V with quiescent current lower than 10 μ A.

II. LDO Small Signal Model

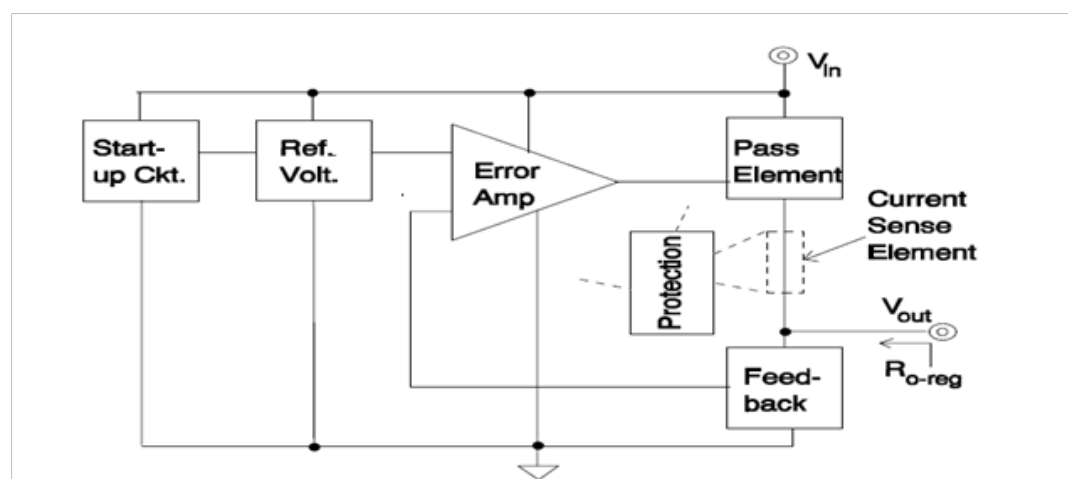


Fig. 1: LDO circuit block diagram^[5]

Figure 1 shows a series low-drop-out regulator circuit that provides a stable DC voltage. The LDO circuit has a low drop-out voltage which is defined as the value of the input/output differential voltage where the control loop stops regulating^[5].

A series low-drop-out regulator is a circuit that provides a well-specified and stable dc voltage whose input to output voltage difference is low. The drop-out voltage is defined as the value of the input/output differential voltage where the control loop stops regulating^[6].

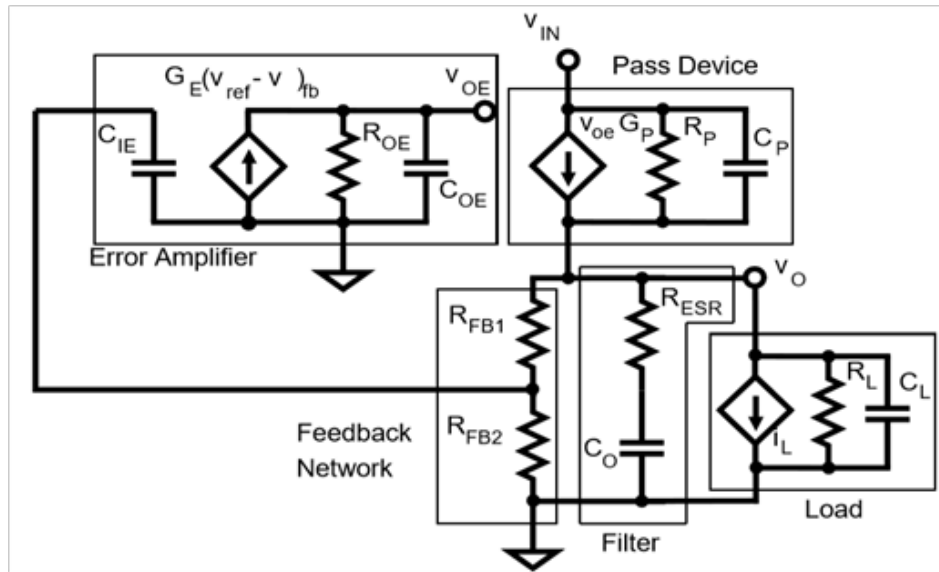


Fig. 2: LDO Equivalent circuit model

III. The proposed circuit Design Methodology

Traditionally, square-law is used in hand analysis to obtain initial design point however, short channel and weak inversion devices do not obey the square law. As a result, square law is seldom used in nowadays designs. The popular approach nowadays is using gm/ID design methodology. Perform DC sweeps for both PMOS and NMOS to generate design charts vs gm/ID. The range of gm/ID values does not differ much from one device to another and from one technology to another. gm/ID can be a though as a normalized measure for the device inversion level.

III.1. LDO circuit Design specifications

To start designing LDO, it is important to first look at the specifications that were given. The parameters of the aimed low dropout voltage regulator design are:

- Output voltage 1.5V
- Input voltage from 1.7V to 2V
- Input reference voltage 1.2V
- Load current from 10uA to 1mA with 10% error
- Fastest change in load current 1usec
- Output capacitor of 1uf with 20% error
- Temperature in range -50°C to 100°C
- Maximum quiescent current 10 uA
- Biasing current of 100nA with 20% error and temperature coefficient of 3mV/K

From these specifications, the circuit is expected to be simple, because the current consumption has to be minimal.

The best way to start designing an LDO regulator is from the output, so the start with designing the pass device and feedback resistor divider.

III.2. Feedback Voltage Divider

The ratio of the feedback factor β_{FB} which states what the division of the output voltage will be^[1]. The reference voltage is 1.2V and the output voltage is 1.5V so the feedback factor is:

$$\beta_{FB} = \frac{V_{FB}}{V_O} = \frac{1.2}{1.5} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} = 0.8 \quad (1)$$

The ratio between the resistors is known, but it is important also to define absolute values for the sake of current consumption and stability.

III.3. Pass Element Design

From the input voltage, which ranges from 1.7 V to 2 V and output voltage specification, which is 1.5V. Therefore, the maximum dropout voltage is 200 mV. There are two choices of pass devices to choose from, NMOS or PMOS. The PMOS has substantially lower demand on the minimum input voltage, because only its saturation voltage gives the minimum voltage needed to stay in saturation $V_{DS,sat}$. To use NMOS, it would be possible, but because of input voltage specification, a charge pump would be needed, to raise the gate voltage of the NMOS pass element

to sufficient level for it to be under proper bias conditions. That would furthermore complicate our circuit and because of this tight specification on low quiescent current, it would be inefficient in terms of power consumption. The PMOS is ultimately the best choice for our application because of its low dropout voltage.

As a result, PMOS device is chosen to be used as a pass element. However, it needs to take into account the

$$I_D = \frac{1}{2} \mu C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 \Rightarrow \frac{W}{L} = I_D \frac{2}{\mu C_{ox}} \cdot (V_{GS} - V_{TH})^2 \text{ [A]} \quad (2)$$

However, this value could be changed drastically under the effect of process corners and temperature. As a result, to be sure that the pass device does not go into triode region, the pass device should be scaled to a larger W/L according to the worst corner in simulation. However, for a larger gate area, a larger the capacitance we get which slows the response of the system and deteriorates its stability.

III.4. Buffer Amplifier design

Since the pass device gate area is large, it introduces a large parasitic capacitance C_{ip} at its gate. In proposed design, the capacitance is not large to impose a slew-rate constraint. However it poses a problem for the system stability. In order to produce sufficient loop gain A_{LG} , a large resistance R_{OE} has to be placed at the output of the error amplifier A_E . The resistance R_{OE} together with capacitance C_{ip} produces a low-frequency pole p_{OE} which will threaten the system stability. Thus, a buffer amplifier A_B is utilized. The amplifier A_B should have a small input capacitance, a small output impedance, and a large enough voltage swing across its output. Therefore, it can be able to both shut the pass device off and drive it fully at maximum load current. Although, a PMOS source follower has been chosen, that may hinder the dropout voltage of the PMOS pass device. That is because of how low its source-gate voltage can fall in respect to V_{IN} [7].

$$V_{DO} \propto \frac{1}{V_{SG,PASS}} = \frac{1}{V_{IN} - V_{O,BUF}} = \frac{1}{V_{IN} - (V_{SG,PASS} + V_{OE})} \text{ [V]} \quad (3)$$

Where V_{DO} is drop out voltage, $V_{SG,PASS}$ is pass transistor source-gate voltage, V_{IN} is input voltage, $V_{O,BUF}$ is buffer output voltage, $V_{SG,PASS}$ is buffer source-gate voltage and V_{OE} is error amplifier output voltage.

maximum load current that will be flowing through it. Specification states 1mA maximum load current with up to 10% possible variation and that gives us a total of 1.1mA maximum load current. The pass transistor should stay in the saturation region under all load conditions, so square-law equation will be utilized for drain current to calculate the minimum W/L ratio of the pass device. Neglecting channel length modulation the equation will be

III.5. Design of Error Amplifier

To choose the right topology for the error amplifier, all the previous constraints and parameters should be taken in consideration as in the case of pass device and buffer. The goal should be low quiescent current, proper bias under all load current and input voltage conditions. In addition, high enough gain to provide sufficient accuracy and PSR at the output, but not excessively high so that the system remains stable [8]. Systematic and random input-referred offset should be low as well. Moreover, the architecture of the error amplifier itself should be considered, so it can drive the buffer properly.

III.6. Differential Pair circuit

The reference voltage V_{ref} may be a limiting factor when selecting the differential amplifier topology. According to the PMOS differential pair [9], the minimal headroom needed above V_{ref} is

$$V_{IN,min} = V_{ref} + V_{SD,sat} + V_{SG} = 2 \cdot V_{SD,sat} + V_{THP} + V_{ref} \text{ [V]} \quad (4)$$

Where $V_{IN,min}$ the minimum is input voltage, $V_{SD,sat}$ is the saturation voltage of PMOS, V_{THP} is its threshold voltage, and V_{SG} is its source-gate voltage. For the NMOS differential pair, the situation changes. The V_{ref} defines the headroom for the input pair and the biasing transistor M_T . The reference voltage has to be large enough to bias both M_T and input pair.

$$V_{ref,min} = V_{GS} + V_{DS,sat} = 2 \cdot V_{DS,sat} + V_{THN} \text{ [V]} \quad (5)$$

Since the minimal input voltage is 1.7 V and V_{ref} is 1.2 V, the headroom of 0.5 V is not enough for PMOS differential pair. So here, the choice is straightforward, NMOS differential pair.

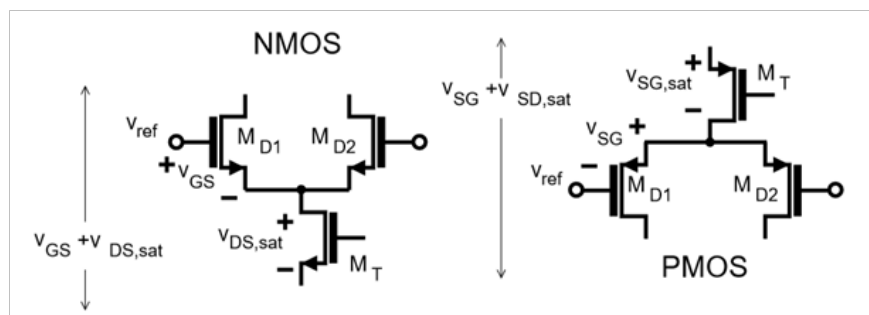


Fig. 3: Dynamic ranges of PMOS and NMOS differential pair [10]

III.7. Error Amplifier Topology

A symmetrical OTA (operational transconductance amplifier) has been chosen as a final topology. The schematic is in figure 4. Compared to simple OTA with differential pair, it has two more branches. Therefore, it has larger quiescent current, but the main advantage of this topology is its large output swing. Only the saturation voltage of the two transistors limits the minimum and maximum voltage at its output. Therefore, the minimum output voltage is the saturation voltage of NMOS.

$$V_{OE,min} = V_{DS,sat} \text{ [V]} \quad (6)$$

And the maximum is the saturation voltage of PMOS at the output stage.

$$V_{OE,max} = V_{IN} - V_{SD,sat} \text{ [V]} \quad (7)$$

This ensures that the error amplifier can drive the buffer and thus the pass transistor properly over specified

load current conditions. The GBW of the OTA is large enough compared to the output dominant pole, so that is not a limiting factor. In terms of PSR the circuit is not completely symmetrical and the derivation of it is not so straight forward as for simple OTA with only one load current mirror. The PSR at the output of the symmetrical OTA depends on the summing of the NMOS a PMOS type mirrors PSR contributions. Also every node, except the output node of the OTA is gate-drain connected, which means that impedance at those nodes is low, because the impedance looking into the gate is $1/g_m$. In small signal model, this reduces the resistance at internal nodes to roughly $1/g_m$.

IV. The Simulation Results

This section will take closer look at the operation of the proposed LDO, how specified variation of parameters influence stability and bias conditions. The final design schematic is presented in figure 5, all bulks of NMOS transistors are connected to ground, and all bulks of PMOS are connected to supply.

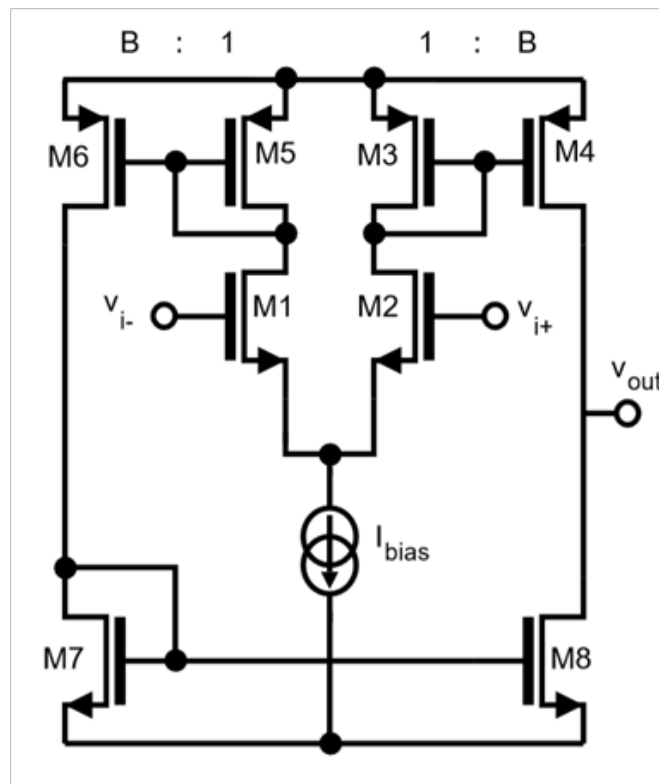


Fig. 4: Symmetrical OTA schematic

First, it is important to assure that the circuit is properly biased; assuring that every transistor is in saturation region is of paramount importance. Since the specification says that quiescent current has to be under 10uA, it's possible to predict that the W/L ratios of the error amplifier and the buffer won't be too large, because there won't be any excessive currents flowing. Next, it is important to strive for putting the current mirrors into the strong inversion region for better matching. However, since there are going

to be small currents, it may be hard to achieve that, since increasing length of the transistors to push them into strong inversion also increases output resistance at the nodes and sacrificing stability for the sake of matching, which is not optimal. Therefore, the target is to obtain as small g_m/I_D ratio as possible, to the extent of not compromising stability. Voltage V_{ref} is 1.2 V and that is high enough for the differential pair M1-M2 and the biasing transistor M4 to stay in saturation. Since the differential pair is for the sake of

gain in weak inversion, $V_{DS,sat}$ of M1, M2 is low and thus it does not hinder the V_{DS} voltage headroom for upper current mirrors comprising of transistors M5-M6 and M7-M8. The main problem with saturation is with the transistor M10 at the output of the error amplifier. When the load current rises, the V_{SG} of the pass transistor needs to be increased via the feedback, to push more current through the pass transistor. Thus, the voltage at gate and at the buffer output V_{BUF} decreases and the output of the error amplifier V_{OE} also decreases, because it is only level shifted voltage from the

buffer output. This may lead to transistor M10 falling into triode region, which would significantly reduce the gain of the error amplifier and thus overall accuracy and ability of the circuit to regulate properly. To ensure that the transistor M10 stays in saturation, it is important to look at the worst corner, which will cause the highest voltage level shift of the buffer and design the buffer W/L ratio accordingly, so the M10 stays in saturation under all conditions. The W/L ratio of M_{PASS} is given by the maximum load current as stated earlier.

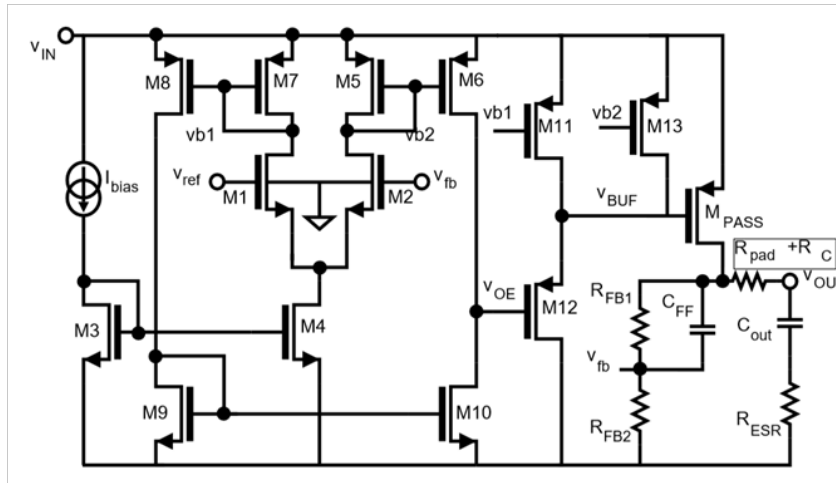


Fig. 5: Final schematic of the proposed LDO

If it has assured that the circuit under proper bias conditions, then it is important to ensure that it is stable under all load conditions. In order to study the circuit stability requirements were outlined and now the exact poles and zeros of the final circuit will be explained. The output pole p_o is defined primarily by the resistance of the pass device R_p and the output capacitor C_o .

$$p_o = \frac{1}{2\pi C_o R_p} \text{ [Hz]} \quad (8)$$

The resistance of the pass device R_p relies on the load current. The larger the current I_{DS} , the smaller the output resistance. From this an assumption could be made, that the output pole p_o will be shifting with load current changes as

shown in Figure 6. Since mainly the output pole defines the unity-gain bandwidth f_{0db} , the bandwidth is also dependent on the load current. Under smaller load, the R_p is large and f_{0db} is at very low frequency, the system is responding slowly to the changes of the input voltage and load current, but is unconditionally stable, because the rest of the poles lie high above the f_{0db} . The other poles that need to be taken into account are the pole at the output of the error amplifier and at the output of the buffer. The error amplifier pole will be at low frequencies due to the high output resistance of the error amplifier. The pole is defined by its output resistance and the capacitance at its output

$$p_{AE} = \frac{1}{2\pi R_{OE} C_{OE}} \text{ [Hz]} \quad (9)$$

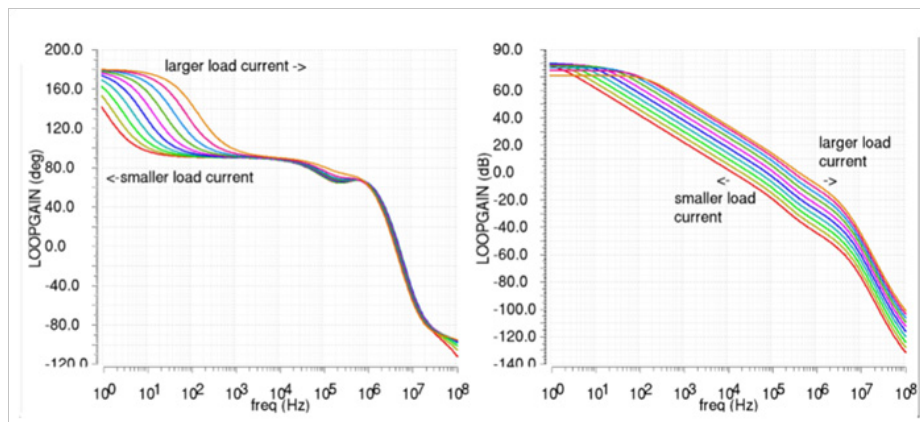


Fig. 6: The change of Load current with frequency

Where R_{OE} incorporates parallel combination of output resistances of transistors M6 and M10. C_{OE} is the sum of parasitic capacitance present at the node. The pole at the output of the buffer is defined similarly to the previous pole, but the buffer output resistance is much lower, due to the source of the Transistor M12 being connected to the node. This introduces resistance $1/g_m$ to the parallel combination of the output resistances. Since it is significantly smaller compared to the drain resistances of transistors M11 and M13, the output pole can be ultimately defined as:

$$P_{ABUF} = \frac{1}{2\pi \frac{1}{g_{m,12}} C_{O,BUF}} \text{ [Hz]} \quad (10)$$

Where capacitance at the output of the buffer $C_{O,BUF}$ is mainly defined by the parasitic capacitance presented at the gate of the PMOS pass device. The buffer output pole will be past the unity-gain bandwidth f_{0dB} . To push these poles to higher frequencies the biasing current of the error amplifiers should be increased. This reduces the output resistance at all nodes and also increase the g_m of M12. Here a trade-off between stability, quiescent current and gain is presented, because loop gain A_{LG} is partly defined by the gain of the error amplifier A_{OE} . Since out specification states that the quiescent current must be under 10uA the aim is for lowest value possible and it is important to choose different way in stabilizing the system. In this case more convenient way is to insert in phase zeros, which to an extent cancel the effects of the poles and allow keeping phase from shifting by more than 135° . One such zero is implicitly present because of the output capacitor equivalent series resistance (ESR).

$$Z_{ESR} = \frac{1}{2\pi C_O R_{ESR}} \text{ [Hz]} \quad (11)$$

This zero can be utilized, but its effect on the stability can vary substantially with temperature and fabrication corners, that must be taken into account.

Also, at the minimum specified ESR, the zero will be at very high frequency and will not save almost any phase. But since the maximum load current is 1.1 mA, if a small resistance R_{pad} is put to the path of the load current, it can push the Z_{ESR} to lower frequencies, and lose only small portion of output voltage. This also simulates the resistance of the pad and, which decided to be between 200–500 mΩ. This way secures, that the circuit is stable for specified range of ESR. Since the error amplifier pole p_{AE} will be below $f_{0dB,min}$ and Z_{ESR} will be around f_{0dB} the phase margin would be deteriorated by buffer output pole p_{ABUF} and also by the parasitic poles at high frequencies, because their combined effect can have impact on the phase margin and especially gain margin. It is important to introduce other zero which can be added by shunting the feedback resistor R_{FB1} with feed-forward capacitor C_{FF} . Thus

$$Z_{FF} = \frac{1}{2\pi R_{FB1} C_{FF}} \text{ [Hz]} \quad (12)$$

For the sake of current consumption, it is convenient for us to make the resistors R_{FB1} and R_{FB2} as large as possible, but not too large, to properly drive the capacitance at the gate of transistor M2. This allows us to make capacitance C_{FF} relatively small so it does not consume vast area. The best way to address the stability issue is to put the Z_{FF} near the p_{AE} and Z_{ESR} near the $f_{0dB,min}$, since the minimum specified ESR is so small, it is more convenient for the Z_{ESR} to be at higher frequency than Z_{FF} . The final design phase and open loop gain response is in the next figure. The first pole is clearly the dominant output pole. Next there is sort of smooth transition and then Z_{FF} is at about the same frequency as p_{AE} which is past 100kHz. The next transition is in between 1 MHz and 10 MHz where the effect of the p_{ABUF} and other parasitic is introduced and is to some extent compensated by the Z_{ESR} .

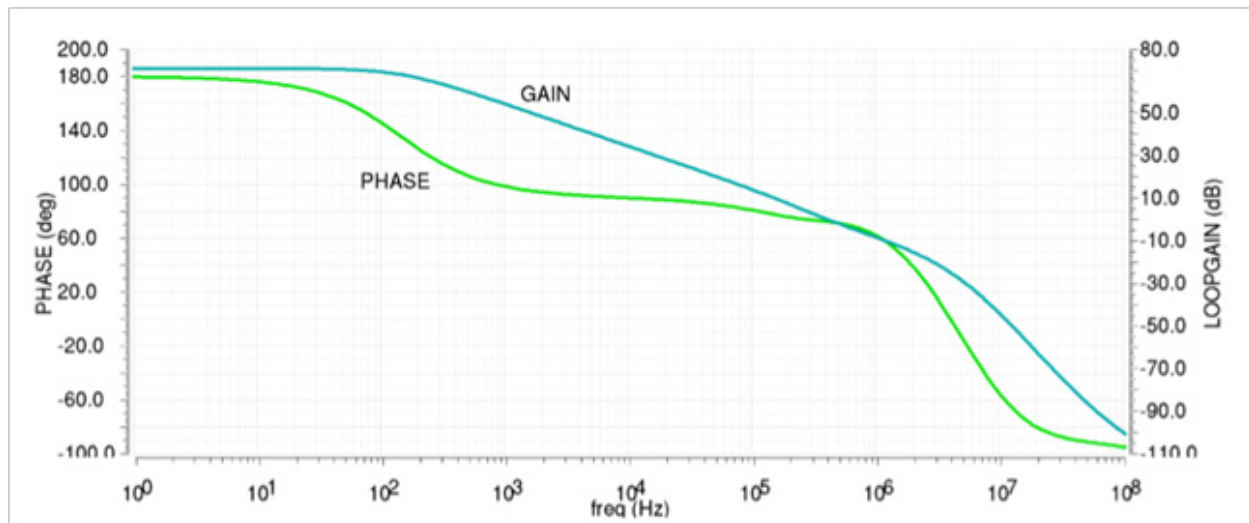


Fig. 7: The phase and open-loop gain response of the proposed circuit

From Figure 7, which assure that the circuit is stable at the nominal corner, it is important to check the variation of the output due to the random offset. The problem is that the GPDK180 does not have mismatch modeled correctly. So to predict the mismatch to at least some extent, the schematic was fully imported into GPDK090 technology. From the simulation the three-sigma variation of the output voltage was under 5 mV, but since the process constants which define the mismatch of the GPDK180 model are not known, it is only a crude approximation. The results from Monte Carlo simulation are in the following figure 8. The gate area of the devices was enlarged so that the threshold voltage mismatch (which was the highest) was minimized, based on the Pelgrom model^[10].

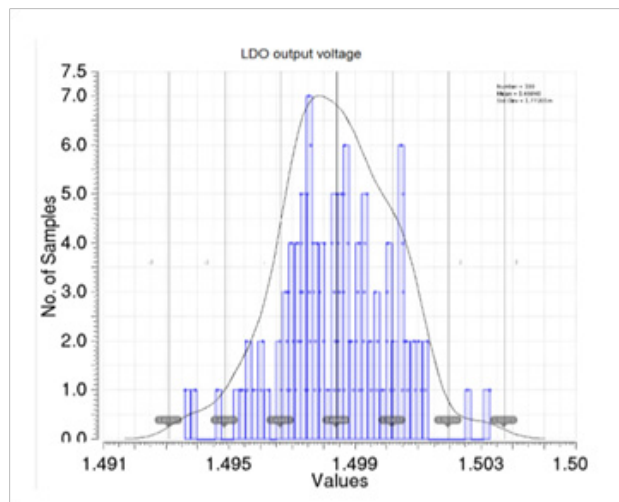


Fig. 8: Monte Carlo simulation of the proposed circuit

Table 1: Final sizes of the circuit devices

Device	W/L [um]
M1, M2	8/10
M3	20/10
M4	10*1/20
M5, M6	3/3
M7, M8	3/3
M9, M10	2/5
M11, M13	3/3
M12	10/1
M _{pass}	10*(20/2)

Table 2: Final sizes of the circuit passive components

component	W [um]	L [um]	value
R _{FB1}	0.6	340.85	200 kΩ
R _{FB2}	0.6	1363.4	800 kΩ
R _C	0.3	15	0.5 Ω
C _{FF}	62.5	20	7 pF
Total Area 2277 um ²			

V. DC Results

This section focuses on steady state parameters of the LDO. It represents values at which the system settles after the transient response fades away.

V.1 Dropout Voltage

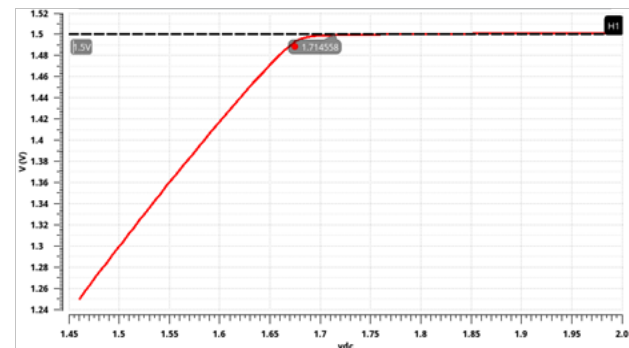


Fig. 9: Input voltage sweep - dropout and regulation region

The dropout voltage was measured as the input voltage at which the output voltage starts to drop from its nominal value of 1.5 V. It was measured under maximum load current of 1.1 mA and in nominal corner. Figure 9 shows how the regulator ceases to regulate when input voltage falls below 1.57 V that is when the pass transistor starts to operate in triode region and the system loses gain^[1, 4, 11, 12]. Thus, the feedback loop cannot keep output value as precise as before.

V.2. Line Regulation

The line regulation shows how the output behaves under slow change of the input supply. In the Figure 10, the line regulation for nominal and worst corner is presented. The worst corner, as expected, is for the lowest bias current and largest output capacitor, that translates into lower gain, which is proportional to the line regulation^[1, 4, 11, 12].

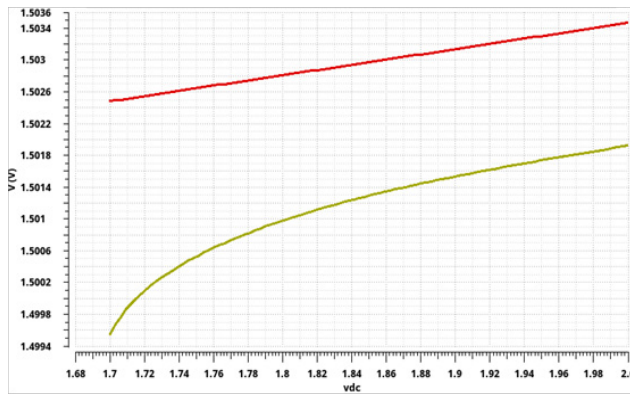


Fig. 10: Line regulation for the proposed circuit

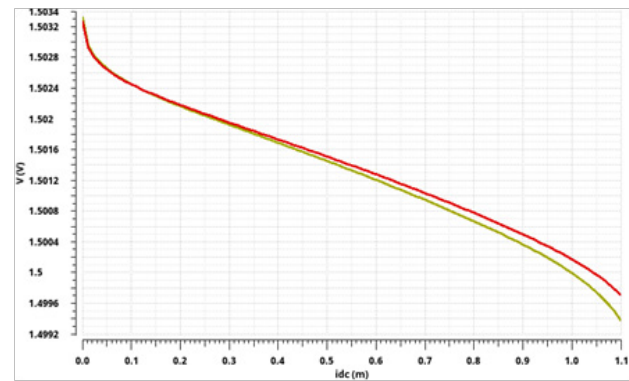


Fig. 11: Load regulation for LDO regulator

V.3. Load Regulation

Another steady state parameter is load regulation. Since the loop gain is finite, the regulator cannot completely cancel the effect of changing load current^[6, 13]. The load regulation is in Figure 11.

V.4. Temperature Variation

It is useful to plot how the output changes with temperature as shown in figure 12, because the ambient temperature is could vary significantly^[14-16], depending on the application where the LDO would be used.

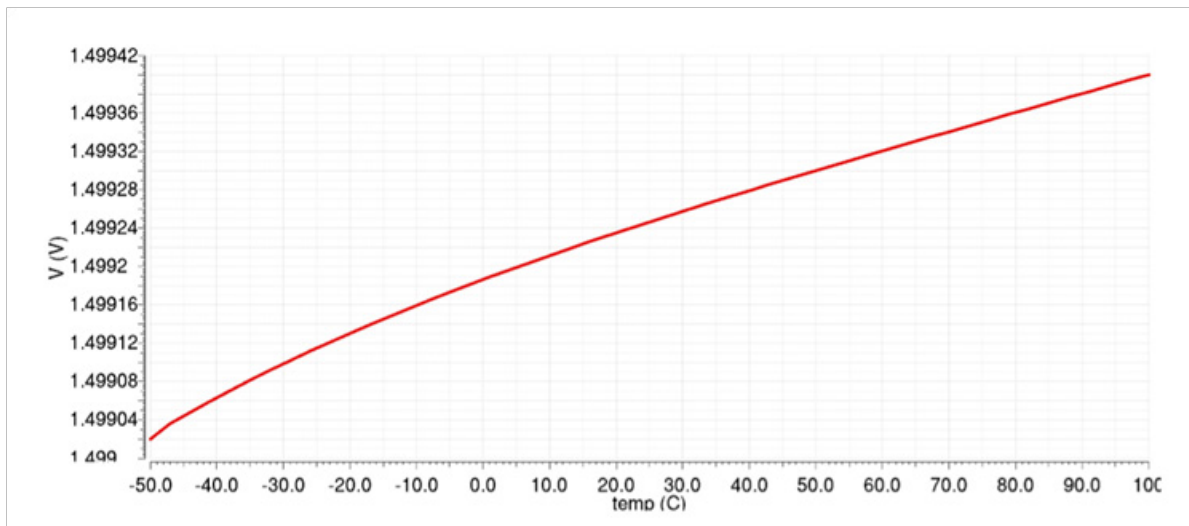


Fig. 12: Output voltage variation with temperature

VI. AC Parameters

It is important to measure the open loop parameters as open-loop gain and phase to define phase margin and gain margin^[12, 16]. In addition, the unity gain bandwidth f_{0dB} defines how fast can the circuit react to changes at the output or input. Open loop parameters like phase margin also defines how the circuit behaves under step response

inputs and such. However, the most important parameter is stability, which is defined by phase and gain margin. at phase margin is aimed to be at least 45° in the worst corner. In Figure 13, the same shifting of the dominant pole introduced earlier, plus the shift of the zeros and other poles due to the change of bias conditions. The most obvious deviation is when the load current is minimal (9uA), then the dominant pole is at the lowest frequency.

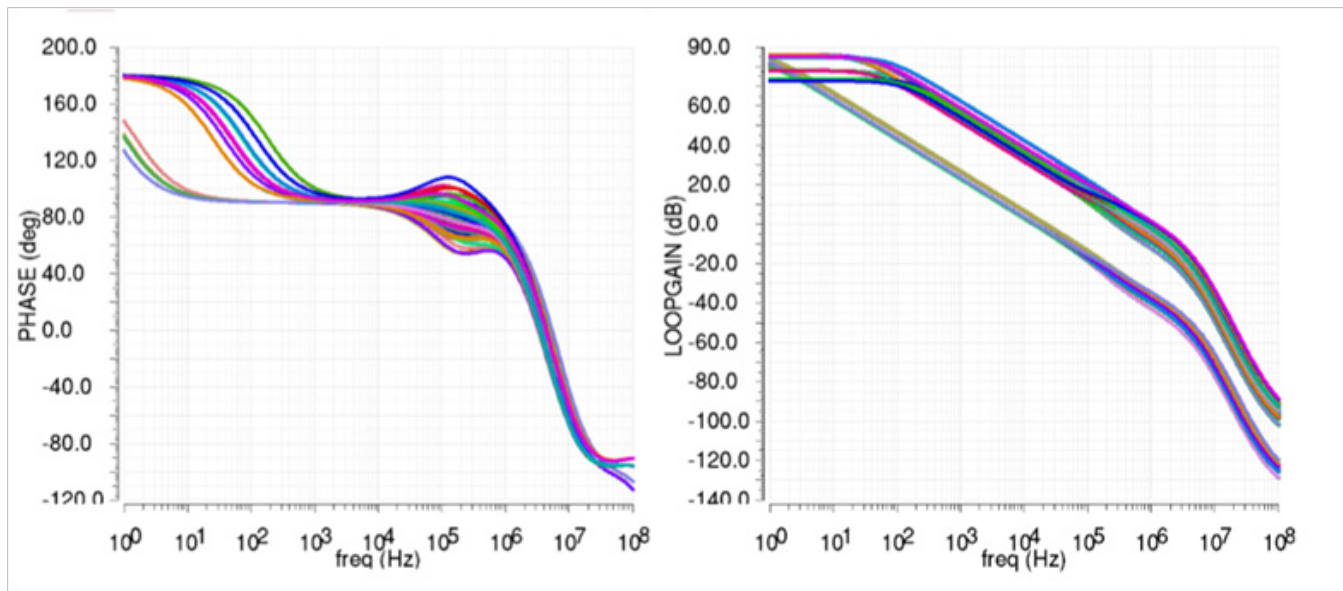


Fig. 13: LDO regulator open loop gain and phase

The gain bandwidth f_{0dB} shifts a lot; it is therefore useful to plot its behavior. In Figure 14 with load current, the f_{0dB} rises, and phase margin accordingly to it falls. the minimum phase margin is not at the maximum output current, but around 250 uA, this needs to be taken into account later during the overall corner simulation. Next important parameter from AC domain is Power Supply Ripple Rejection or PSR (shortly Power Supply Rejection) [5, 17, 18]. It defines how well can the regulator suppress changing input voltage over wide frequency range. It is important to note, that in our design, the PSR at the very

output of the LDO is affected by the RC filter, which is formed from the output capacitor and the resistance of the pad. It starts to filter high frequency supply signals just below the unity gain bandwidth. Normally, it would drop in the magnitude of PSR around unity gain bandwidth, as it is in figure 15, but since the RC filter start to filter the signal, the unity gain bandwidth effect is compensated and the PSR is even better after that. Since the PSR was not the scope of this work, it can be settled with the 50 dB value, which is satisfying.

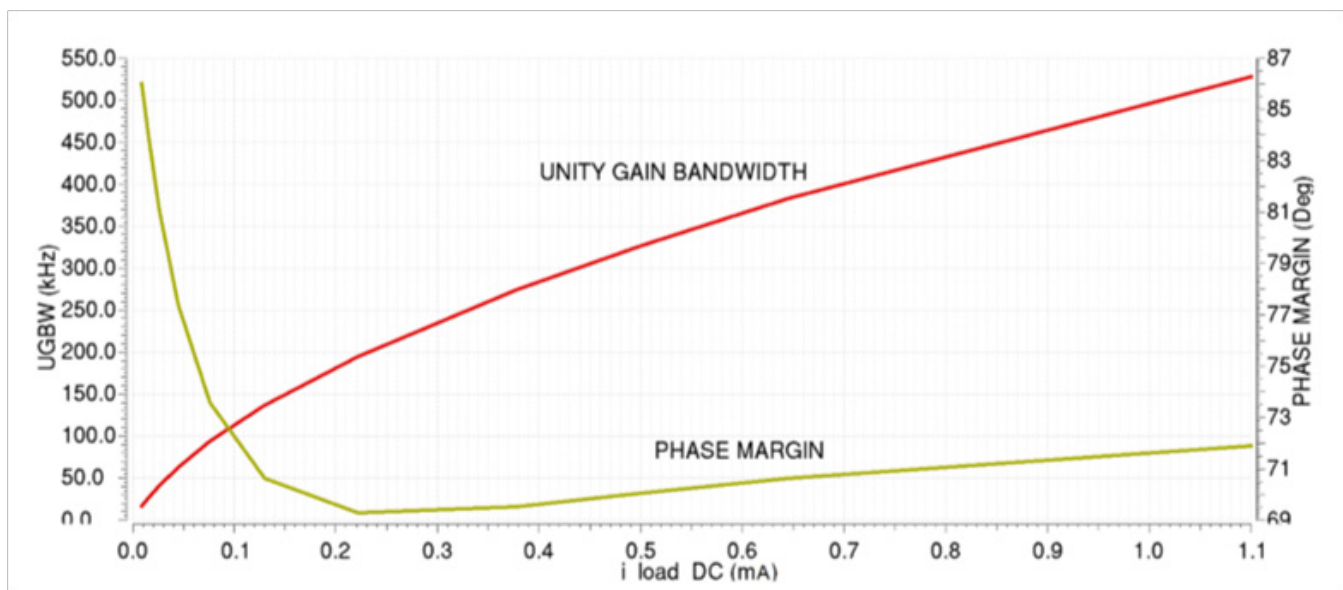


Fig. 14: Unity gain bandwidth and Phase margin vs. load current

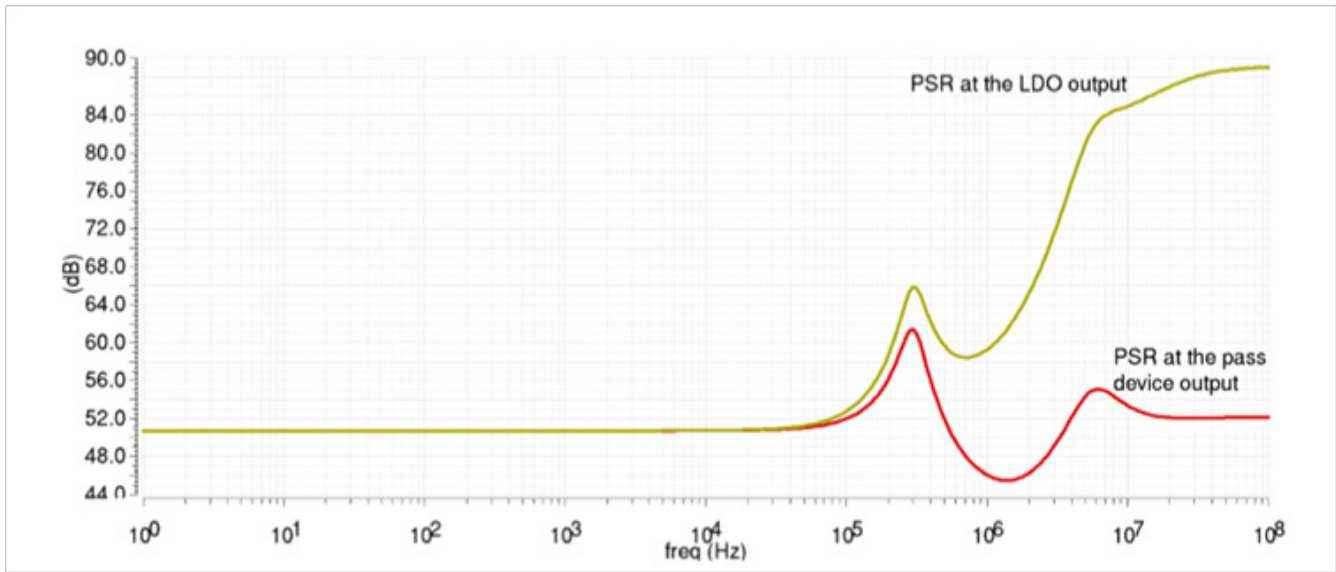


Fig. 15: Power supply ripple rejection(PSR) of the LDO regulator

VII. Transient Analysis

The open loop AC responses and DC response of the system are simulated which gives satisfying results; they are mostly helpful approximations of the circuit behavior. The transient response tests how the circuit behaves in real time with varying large signal transients. The important parameters of LDO regulator in transient domain are Load and Line Transient responses.

VII.1 Load Transient

In figure 16 shows the load transient response with frequency of 5 kHz so the signal has enough time to settle. Since the system has huge phase margin at low load current, the transition from maximum load current to minimum load current is slow, smooth and without any overshoots. On the other hand, the transition from minimum load current to maximum load current, where phase margin is around 70° is fast and with small overshoot.

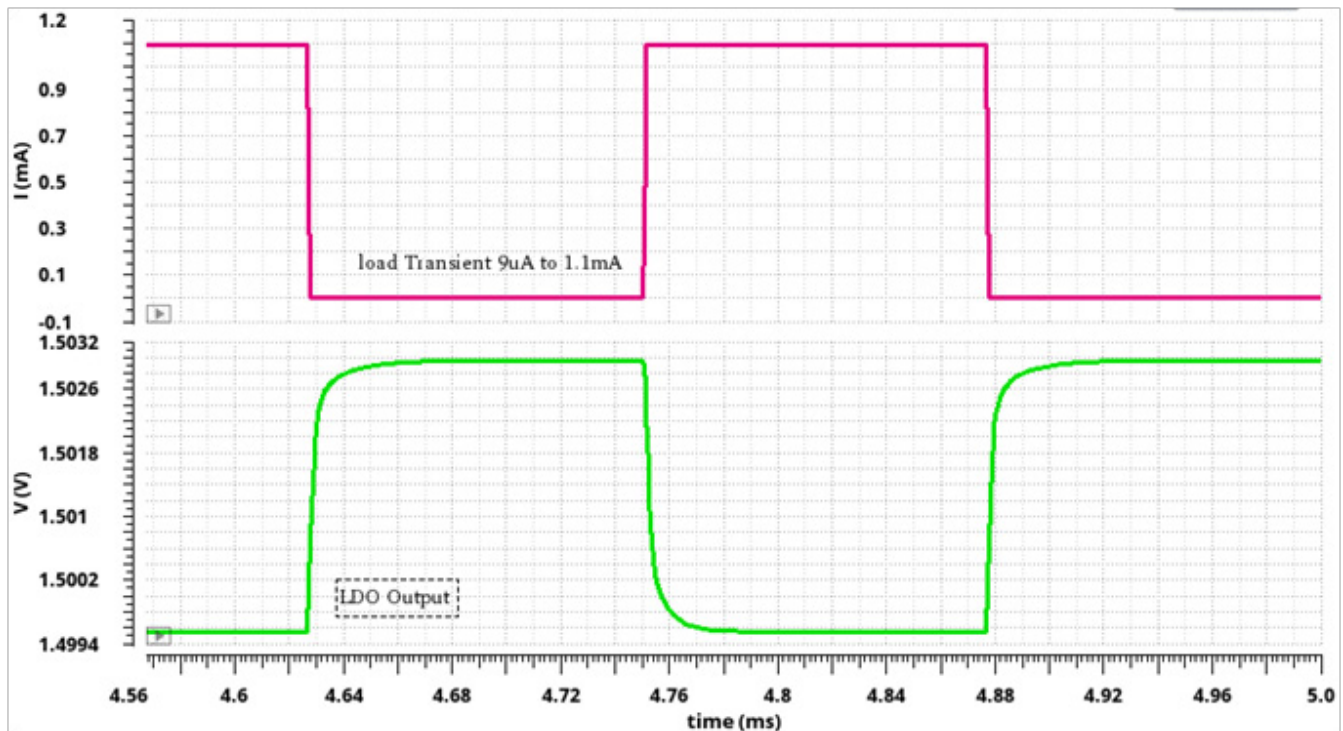


Fig. 16: The load transient from 9uA to 1.1mA at low frequency of 5 kHz

The ESR of the output capacitor mainly causes this effect. The larger the current step and ESR is, the larger the overshoot^[19-22]. The capacitor is trying to source the current to the load, before the regulator starts to regulate and the ESR is in the way of the

current from capacitor. As a result, there is a voltage drop on it. Since ESR in suggested application is not very large and load current is small, these overshoots tend to be in the range of millivolts, which is optimal.

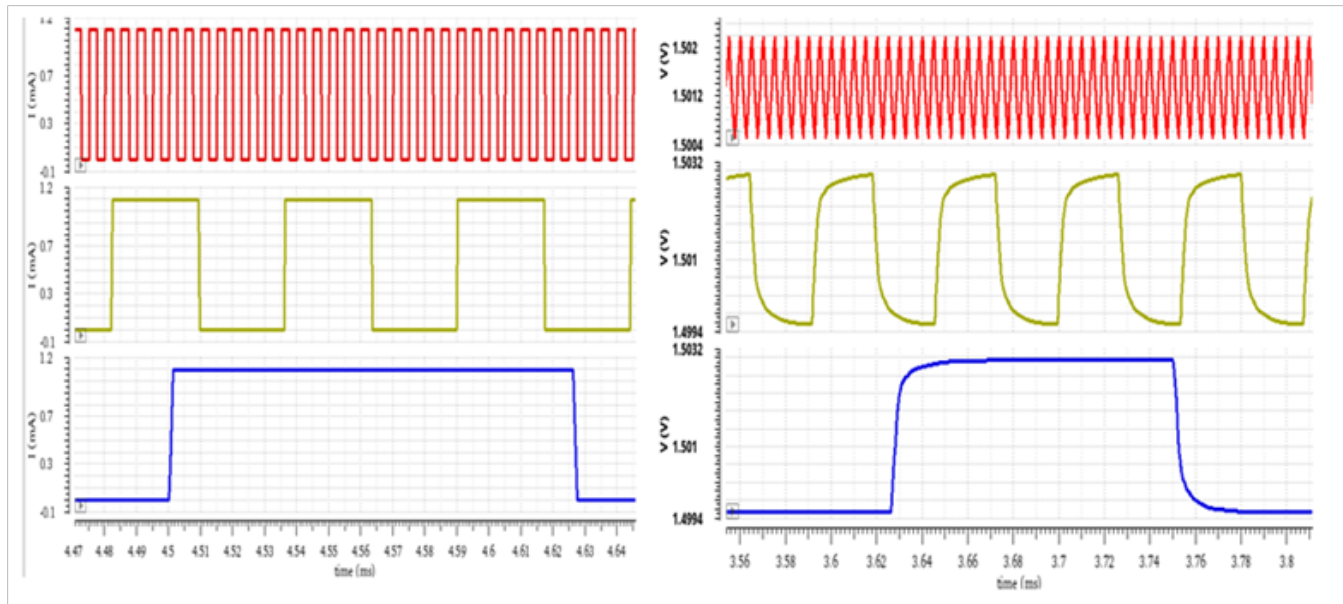


Fig. 17: The load transient from 9uA to 1.1mA for 5kHz, 18.5kHz and 200kHz

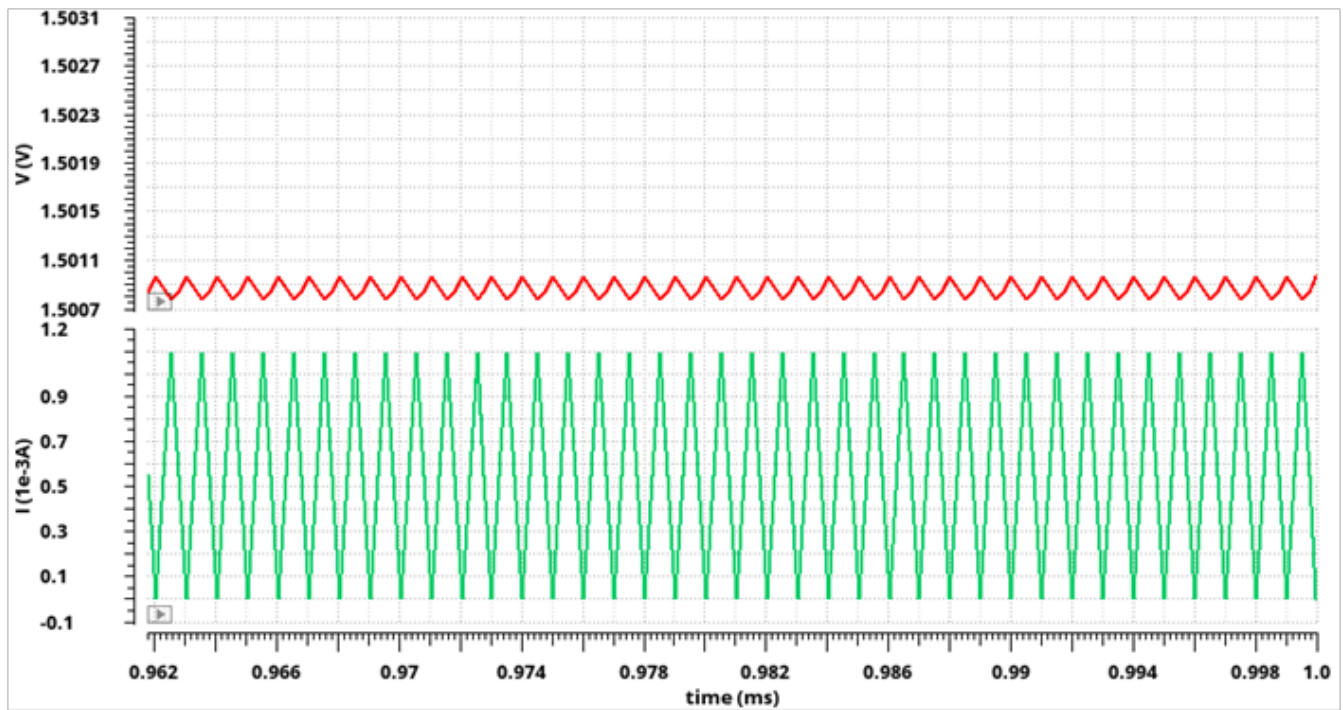


Fig. 18: The load transient from 9uA to 1.1mA at 1MHz

From Figure 17, the output instability and the ripples as result of the decrease of the system gain. The system cannot respond fast enough to the changes of the output. The system bandwidth changes, then the regulator does not have time to react. As a result, it oscillates between high and low load states, as shown in figure 18.

VII.2. Line Transient

The line transient behaves quite differently from the load

transient. The difference between the steady state voltages of the line transient is much lower, because it corresponds with the power supply rejection and line regulation. In addition, the overshoots are in opposite directions to the overshoots of the load transient. There is large difference between line transient for small and large load current^[4, 16, 23]. Figures 19 and 20 show the response at maximum load current and the comparison with small load current.

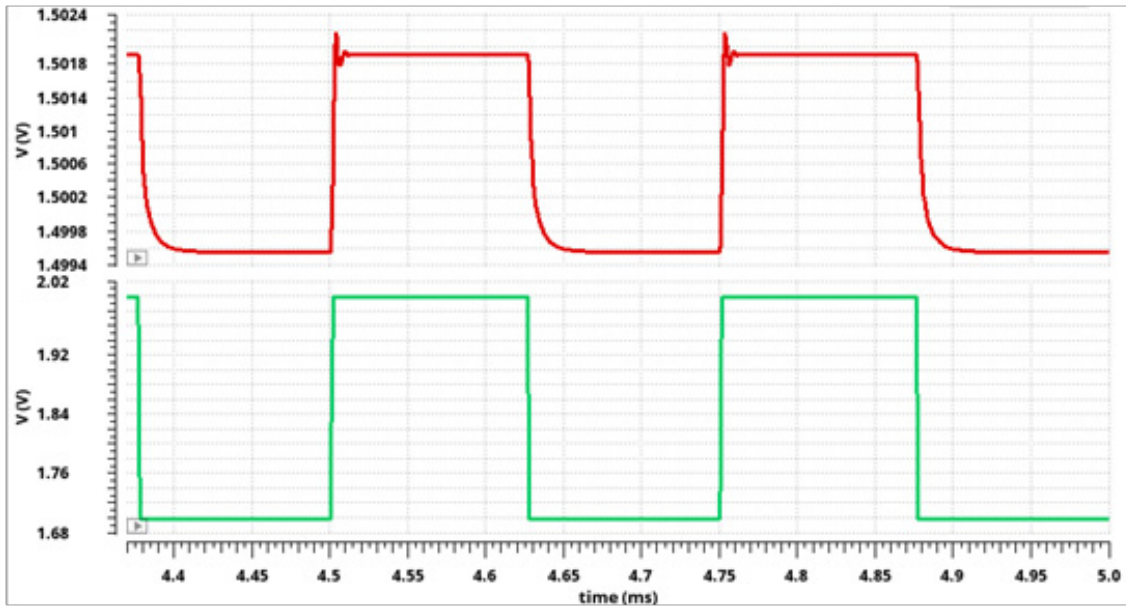


Fig. 19: Line transient from 1.7v to 2V for load current of 1.1mA at 5 kHz frequency

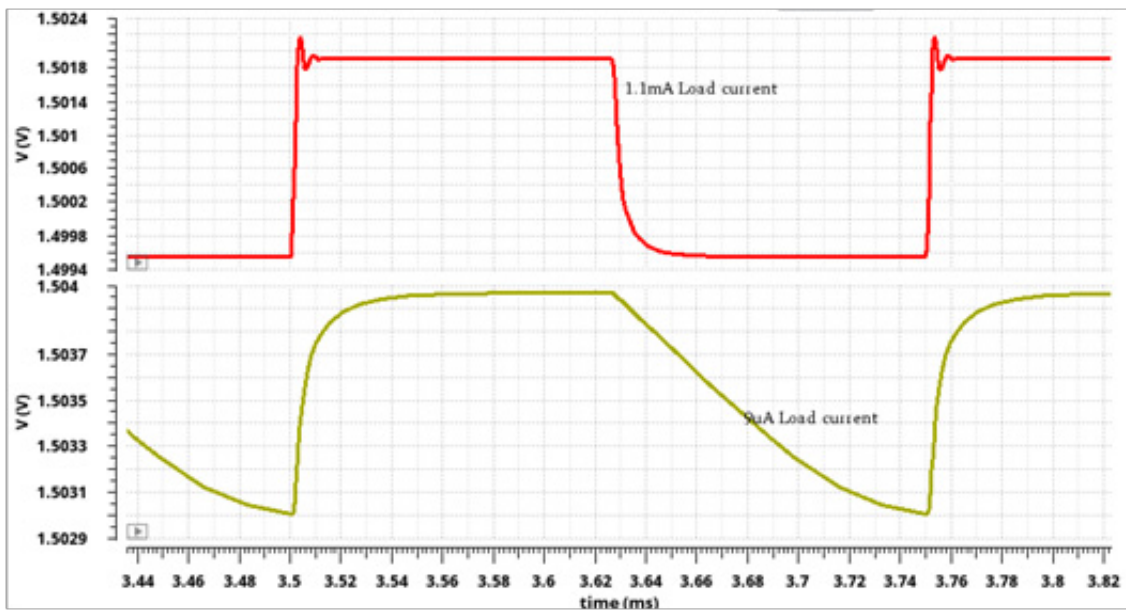


Fig. 20: Line transient from 1.7v to 2V for load current of 1.1mA and 9uA at 5kHz frequency

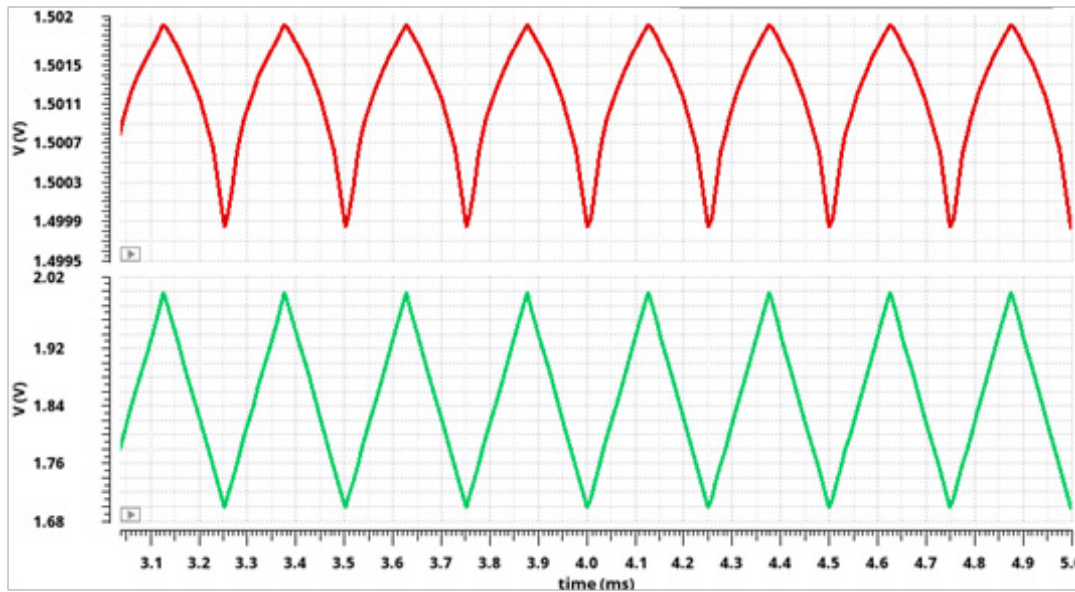


Fig. 21: Line transient from 1.7 V to 2 V for load current of 1.1 mA at 1 MHz frequency

Clearly when the voltage rises, the response is fast, because the capacitor is charged by the current from the supply. When the voltage drops, the output capacitor holds its value for quite a long time, because it is discharged only by a small load current of about 15 μ A.

Line transient at higher frequencies of the system has similar effect as in the case of high frequency load transient

as shown in Figure 21.

VII.3. Power Supply Ripple Rejection

To measure the PSR, the transient ripple signal will be superimposed on the V_{IN} supply line and the ratio of the output ripple to the input ripple should give us roughly the same PSR that is received from AC analysis.

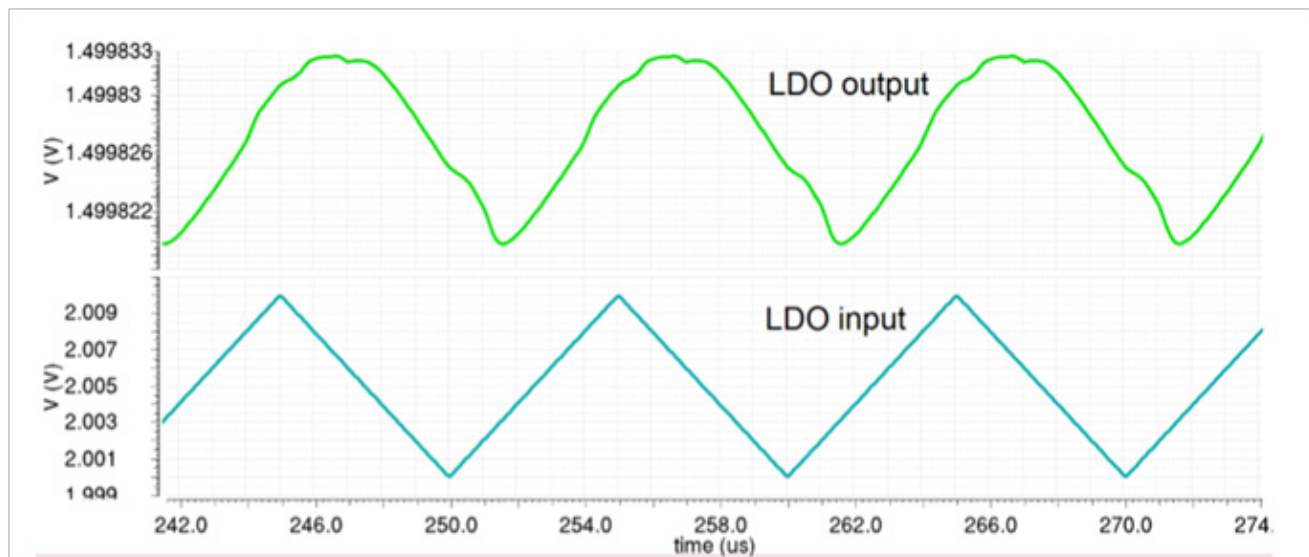


Fig. 22: Transient response to power supply ripple of 10 mV

Figure 22 shows the output versus input voltage. When 10 mV ripples is superimposed to the supply line, the output changes in the range of

microvolts. The total PSR given by the total change of the input voltage to the total change of the output voltage.

$$PSR = \frac{\Delta v_{in}}{\Delta v_{out}} \quad (13)$$

This gives us about 50 dB PSR depending on the frequency and the simulation corner.

VIII. Corner Analysis

The last step in the proposed circuit verification is called corner analysis. The process parameters like, oxide thickness, carrier mobility, width, and length of the gate vary and different dies are fabricated with different

absolute parameters. Especially passive components like resistors and capacitors may differ up to 20% in absolute value, but ratio of resistor-to-resistor is much more precise in the same die, the error is about 0.1%. These changes in the absolute resistance will affect the quiescent current and the position of the compensation zeros. The parameter corners and their ranges^[24], which should be taken into account, is shown in table 3.

Table 3: Parameter corners and their ranges^[24].

Corner parameter	Range
input voltage (V_{in})	1.7 V to 2 V
load current (I_{load})	9 uA to 1.1 mA
bias current (I_{bias})	80 nA to 120 nA
temperature (Temp)	-50°C to 100°C
output capacitor value	0.8 uF to 1.2 uF
output capacitor ESR	0.01 Ω to 0.3 Ω
pad resistance (R_{pad})	0.2 Ω to 0.5 Ω

It is possible to predict the behavior of some parameters in different corners, but for example phase and gain margin are hard to predict. So this simulation is vital to verify, that the circuit is stable under all conditions. By analyzing corner analysis table, the parameters behave as it is predicted earlier. Quiescent current is largest for fast

resistor corner, where the total resistance of the feedback divider is smallest. Unity gain bandwidth is low when the load current is low. It is possible to predict the behavior, but without analyzing all corners. It wouldn't be assured, that for example some transistor does not fall out of saturation region at some process corner.

Table 4: Corner analysis for process, parameters and temperature corners for DC and AC parameters

Parameter	Corner Analysis									
	Nom.	WC	Proc.	V_{in}	I_{load}	I_{bias}	Temp	C_out	R_ESR	R_pad
$V_{out,min}$ [V]	1.499	1.498	SSF	Min	Max	Max	Max	Min	Min	Max
$V_{out,max}$ [V]	1.499	1.502	FFS	Max	Min	Min	Max	Min	Min	Min
$V_{drop,max}$ [mV]	15.6	89.64	SSF	-	Max	Max	Min	Min	Min	Min
I_q [uA]	4.62	6.43	FFF	Max	Max	Max	Max	Min	Min	Min
$M10_{hdr}$ [mV]	355.5m	106.6	SSF	Min	Max	Min	Min	Min	Min	Min
DC gain [dB]	76.1	67	SSF	Min	Max	Max	Min	Max	Max	Max
UGBW [MHz]	0.571	0.012	SFS	Max	Min	Min	Max	Max	Min	Min
PM [deg.]	65.1	48.6	SSF	Max	Max	Min	Min	Min	Min	Min
GM [dB]	21.39	13.54	FSS	Max	Max	Max	Max	Min	Max	Max
$PSR_{UGBW/10}$	54.2	43.21	SSF	Min	Max	Max	Min	Min	Min	Min
PSR_{UGBW} [dB]	57.8	51.08	FFS	Min	Max	Min	Min	Min	Max	Min
$PSR_{UGBW*10}$	82	57.9	FFS	Min	Max	Max	Min	Min	Max	Max



Transient analysis parameter corners were measured for low frequency signal of 5kHz, so that the output has enough time to settle. The transient load and

line responses can properly be measured. It is assumed that the output will not be changed frequently, especially load current.

Table 5: Corner analysis for process, parameters and temperature corners for line transient analysis

Line transient corners								
Settling time for high to low line transient								
Nom.	WC	Proc.	I _{load}	I _{bias}	Temp	C _{out}	R _{ESR}	R _{pad}
3.7 us	78.91 us	SFS	min	min	max	max	min	max
Settling time for low to high line transient								
Nom.	WC	Proc.	I _{load}	I _{bias}	Temp	C _{out}	R _{ESR}	R _{pad}
3.7 us	33.1 us	FFS	min	min	max	max	max	max
Percent overshoot for high to low line transient								
Nom.	WC	Proc.	I _{load}	I _{bias}	Temp	C _{out}	R _{ESR}	R _{pad}
0	12.7%	SFF	220 uA	min	min	min	min	min
Percent overshoot for low to high line transient								
Nom.	WC	Proc.	I _{load}	I _{bias}	Temp	C _{out}	R _{ESR}	R _{pad}
0	6.25%	FFS	220 uA	min	min	min	min	min

Table 6: Corner analysis for process, parameters and temperature corners for load transient analysis

Load transient corners								
Settling time for high to low load transient								
Nom.	WC	Proc.	V _{in}	I _{bias}	Temp	C _{out}	R _{ESR}	R _{pad}
2.6 us	16.2 us	FFS	max	max	max	max	max	max
Settling time for low to high load transient								
Nom.	WC	Proc.	V _{in}	I _{bias}	Temp	C _{out}	R _{ESR}	R _{pad}
2.5 us	5.5 us	FSS	min	max	max	max	max	max
Percent overshoot for high to low load transient								
Nom.	WC	Proc.	V _{in}	I _{bias}	Temp	C _{out}	R _{ESR}	R _{pad}
0	1.3%	SFF	max	min	min	min	min	min
Percent overshoot for low to high load transient								
Nom.	WC	Proc.	V _{in}	I _{bias}	Temp	C _{out}	R _{ESR}	R _{pad}
6.7 %	36.6%	SFS	max	min	min	min	min	min

IX. CONCLUSION

In this work, design of an LDO regulator in GPDK180 technology, to meet specified parameters, is presented. There were several parameters that were taken into account during the design. The main focus was on the quiescent

current, which was specified to be under 10 uA. First, the typical parameters of the LDO regulators are discussed, how are they interpreted and how to measure them. After that the GPDK180 technology parameters were analyzed, to obtain better understanding of how the devices that used

behave under different conditions. The stability under all load conditions has been discussed. Since the pass device is a high capacity load, an operational transconductance amplifier was utilized as the error amplifier.

Symmetrical OTA topology has been chosen for its wide output swing, because the voltage at its output will be varying significantly with changing load conditions.

Table 7: Comparison of specified and accomplished parameters

Parameter	Specification	Nominal results
Iload,max	< 1.1 mA	1.1 mA
Iq	< 10 uA	4.62 uA
Vout	1.5 V	1.499 V
Vdrop	<0.2 V	15.6 mV
UGBW	-	571 kHz
PM	> 45° at WC	48.6° at WC
GM	-	13.54 at WC
PSRDC	-	54.2 dB
PSR1 MHz	-	62.5 dB
Area on chip	-	2730 um ²
Efficiency	-	82%

The circuit was stabilized with PMOS source follower buffer amplifier and by utilizing phase saving zeros. Parameters of the designed LDO voltage regulators were measured using Spectre simulator in Cadence design environment. From table 7 it is clear that the specifications^[24] have been met. Designed LDO regulator is stable under all process and parameter corners, which is essential.

The small output current is offset with small quiescent current and very low dropout voltage. The efficiency depends on the input voltage and ranges from 75% to 88% depending on the input voltage. The final design meets the specification but there is wide room for improvement. Biasing techniques in respect to load current could be implemented to achieve stability at larger output currents while keeping the efficiency of the circuit relatively constant.

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