ALL OPTICAL OVSF CODE GENERATOR REALIZATION USING OPTICAL FLIP FLOP AND OPTICAL HARDLIMITTERS

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ABSTRACT

The orthogonal variables spreading factor (OVSF) provides variables data rates to flexible support many applications with different bandwidth. This paper presents an optical OVSF code generator using all optical gates and a set of all optical flip-flops based on two coupled polarization switches (PSWs). The optical OVSF code generator helps to use the OVSF code technique in optical communications. The general objective is to make the OVSF code tree suitable to support a lot of users in the optical communication links. The overall design and the results are discussed through the realization and the computing numerical simulation to confirm its operation and feasibility. The proposed scheme has been theoretically demonstrated for a spreading factor of 4 and 8.

Keywords: Optical Flip Flops, Optical Gates, Bragg Grating, OVSF, SOA.

1. Introduction

The Modern Code Division Multiple Access (CDMA) uses the OVSF technology codes to provide multiuser access. It has a lot of uses in different applications mainly with digital communications and test pattern generations.

In the OVSF, a single code using one transceiver can support higher and variable data rates with less complexity than the multi-code orthogonal constant spreading factor (OCSF) [1]. The OVSF techniques of code placement and allocation in CDMA guarantee the orthogonally between all users in different communication channels.

The emergence of increasingly high speed and the number of users in optical communication systems demands the OVSF codes technique in the optical communication links. The performing of signal processing operations entirely within the optical domain would exploit the speed and parallelism inherent to optics [2].

The overall optical design of linear feedback shift register (LFSR) of pseudorandom binary sequence (PRBS) generator of CDMA using the hardlimiter and a set of series all

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optical D flip flops has been demonstrated by Tanay and Tamer et al. (2013) [3]. Zoirios et al. (2011) [4] have demonstrated an all optical pseudorandom generators using the Terahertz optical asymmetric Demultiplexer (TOAD).

In this paper, the basic operation and design of all-optical OVSF code generator of the modern CDMA used in Universal Mobile Telecommunication System (UMTS) standard are proposed. The overall optical design in the optical communication system eliminates the conversion from optical to electrical and vice versa and reduces the latency due to this conversion [3].

An overview of the OVSF codes and its code placement methods are presented in Section 2. The digital electronic circuit of OVSF code is represented in Section 3. The building construction and operation of optical devices such as all optical gates and all optical flip flops are proposed in Section 4. Finally, the overall optical design of OVSF code generator and the results output from this generator are displayed in Section 5.

2. OVSF codes in the modern CDMA

The CDMA system allows multiple users to transmit at the same time in the same frequency band [3]. The CDMA suffers from the high blocking probability because the number of orthogonal codes is limited. There are two steps applied to users in a CDMA system. The first step is transforming every bit into a code sequence, where the code sequence has a length called the spreading factor (SF). The second step is called the scrambling process, where the scrambling codes are used to separate the signal from different sources [5, 6]. The OVSF in CDMA achieves a flexible support of mixed and variable data rates at the same bandwidth, where the OVSF codes are used as the channelization codes [7].

The OVSF codes can be represented and defined by the code tree shown in Figure 1. Each OVSF code can be presented by a channelization code $C_{SF,N}$, where *SF* is the spreading factor in the range $[4\text{-}512]=[2^2\text{-}2^9]$ and *N* is the branch identification number of user, $1 < N < (SF\text{-}1)$. The number of codes at each level is equal to the value of SF. All codes in the same layer are orthogonal, while codes in different layers are orthogonal if they do not have an ancestor-descendant relationship such as $C_{4,2}$ and $C_{2,2}$. Leaf codes have the minimum data rate, which is denoted by 1R and the data rate is doubled whenever we go one level up the tree [8].
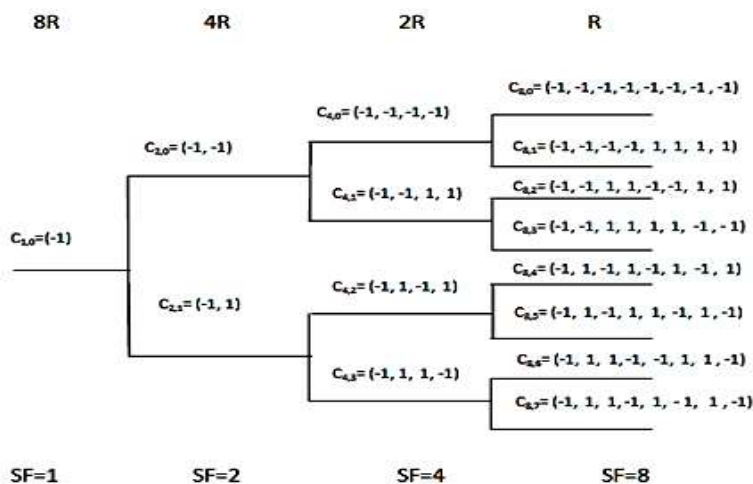

Fig. 1. Tree of OVSF codes till spreading factor SF=8

There are many techniques used for code placement, where the code placement techniue is allocation policy for a new user requesting for a code of rate kR. There are two possible prbabilties that occur at no free codes exists, the first one is rejecting this call (i.e. Code Blocking) and the second is to relocate the existing codes used for a new user [8]. The OVSF code placement has been investigated as follows. Chao et al. [8] proposed a simple algorithm based on single and multi- codes placement and replacement schemes, but it possibly incurs many fragmented codes which produce a code blocking problem. The proposed strategies in Chao [8] and Chen et al. [10] algorithms are based on three strategies of Random, Leftmost and Crowded –first. The OVSF code placement is assigned for IMT-2000 for multi-rate with less complexity by Cheng and Lin [9]. Recently, Chen and Lung [6] proposed un-sequence property of linear-code chains to design a new code placement and replacement mechanism by identifying a linear-code chains (LCCs) and nonlinear-code trees (NCTs) in the Rotated OVSF code tree. The logic circuit of OVSF code tree generator was designed by Dong [11] and Boris [12].

3. The digital logic circuit of OVSF codes generator

This section represents the electrical logic circuit of OVSF codes generator. Boris et al. [12] proposed a logic circuit for OVSF code generator. The hardware of the OVSF codes generator consists of a set of logic gates and T flip flops. The chip sequence is specified in binary number set $\{-1, +1\}$ for digital logic operating in the set $\{0, 1\}$. The OVSF codes generator is shown in Figure 2 [12]. This generator consists of 9 bits OVSF code ID register (n_8 - n_0), this ID register represent the identification number of user N, supposing the channelization code $C_{8,6}$ is required

$N=6=n_3n_2n_1n_0=0110$
$SF=8$

Also, the OVSF generator contains a set of AND gates, XOR gates, and 8 bits binary ripple counter as shown in Figure 2. That code generator is capable of producing codes with a spreading factor over range SF=4 to 512 [12]. The logical expression of OVSF code can be expressed as:

$$OVSF\ Code = (n_0 \cap b_8) \oplus (n_1 \cap b_7) \oplus (n_2 \cap b_6) \oplus (n_3 \cap b_5) \oplus (n_4 \cap b_4) \oplus$$
$$(n_5 \cap b_3) \oplus (n_6 \cap b_2) \oplus (n_7 \cap b_1) \oplus (n_8 \cap b_0) \quad (1)$$

$\oplus$ and $\cap$ indicates the XOR and AND operation, respectively.

The design counter is counting incrementally from 0 to $SF - 1$, where b_8 is always the most significant bit (MSB), and the least significant bit (LSB) is specified by the variable spreading factor SF. The MSB of ID code number N is always enabled by the LSB of the counter [12]. In this case, a regular binary ripple counter is required to count between 0 and $SF - 1$. Based on the logic circuit of OVSF code generator, the code generated for all channelization codes in the level of SF=8 for binary counting $b_8b_7b_6$ is depicted in Table 1. The logic circuit of binary ripple counter is depicted in Figure 3 [12]. The counter consists of a series T flip flops of 9 bits. The LSB counting is controlled by SF register as depicted in Table 2.

The MSB of counter is always n_8, and the LSB is controlled by SF register code. The stored value in SF register represents the information describing the spreading factor and the code ID required to generating the code.
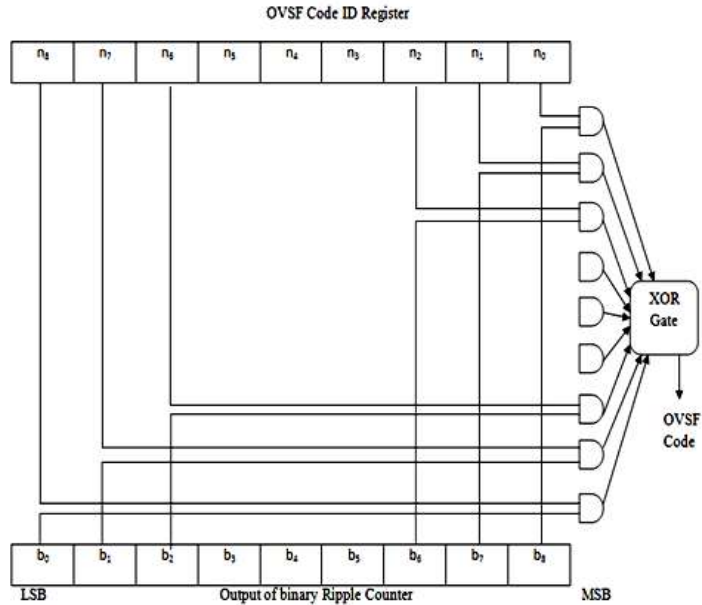
Fig. 2. The logic circuit of OVSF codes generator [12].

Table1.

Generation of channelization code for *SF*=8

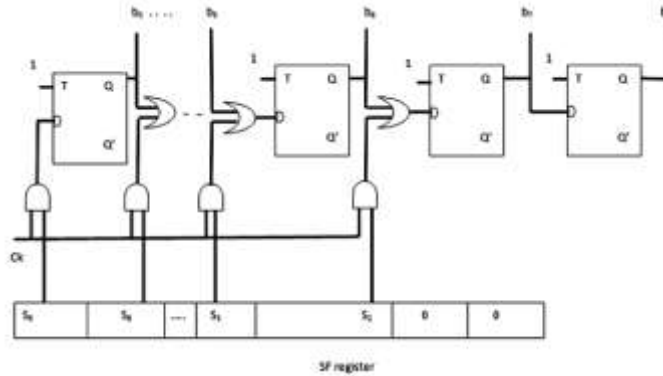| Counter Code O/P $b_8 b_7 b_6$	000	001	010	011	100	101	110	111
Logic Operation OVSF Code	n_3	$n_3 \oplus n_2$	$n_3 \oplus n_1$	$n_3 \oplus n_2 \oplus n_1$	$n_3 \oplus n_0$	$n_3 \oplus n_2 \oplus n_0$	$n_3 \oplus n_1 \oplus n_0$	$n_3 \oplus n_2 \oplus n_1 \oplus n_0$
$C_{8,0}$ ($n_3 n_2 n_1 n_0$=0000)	0	0	0	0	0	0	0	0
$C_{8,1}$ ($n_3 n_2 n_1 n_0$=0001)	0	0	0	0	1	1	1	1
$C_{8,2}$ ($n_3 n_2 n_1 n_0$=0010)	0	0	1	1	0	0	1	1
$C_{8,3}$ ($n_3 n_2 n_1 n_0$=0011)	0	0	1	1	1	1	0	0
$C_{8,4}$ ($n_3 n_2 n_1 n_0$=0100)	0	1	0	1	0	1	0	1
$C_{8,5}$ ($n_3 n_2 n_1 n_0$=0101)	0	1	0	1	1	0	1	0
$C_{8,6}$ ($n_3 n_2 n_1 n_0$=0110)	0	1	1	0	0	1	1	0
$C_{8,7}$ ($n_3 n_2 n_1 n_0$=0111)	0	1	1	0	1	0	0	1

Fig. 3. The logic circuit of 9 bits ripple counter with variable location of the LSB [12]

Table 2.

The contents of *SF* register for different spreading factors

SF	SF Register $S_9S_8S_7S_6S_5S_4S_3S_2S_1S_0$	Counter Range
1	0000000000	0
2	0000000000	0
4	0000000100	0-4
8	0000001000	0-8
16	0000010000	0-16
32	0000100000	0-32
64	0001000000	0-64
128	0010000000	0-128
256	0100000000	0-256
512	1000000000	0-512

4. All optical hardware components

This section represents the optical components used in the realization of the proposed optical OVSF generator.

4.1. All optical AND, OR and XOR gates

Figure 4 [3, 13] illustrates an all-optical XOR and AND gates using the Bragg grating as a hardlimiter. Inputs A and B get combined into a single beam. The transmitted intensity is defined as O1 output and the reflected value as output O2. We bias the hardlimiter at a limiting value a = 2. If one of the inputs is 0 and the other 1, the output at O1 is 0 and at O2 is 1. If both inputs A and B have the value of 1, then 2 is transmitted and 0 reflected. If both A and B inputs have the value of 0, then 0 is transmitted and a 0 is reflected. Thus, O1 yields the result of an AND operation and O2 the result of a digital XOR. The intensity value 2 output of O1 (AND) must be normalized to yield a digital output [13, 14].
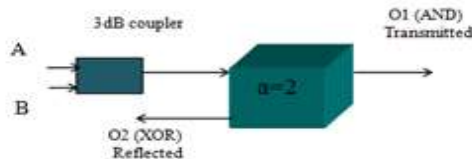

Fig. 4. All optical XOR and AND gates [3, 13].

Figure 5 [13] illustrates the use of the Bragg grating as a hardlimiter in the construction of OR gate. Inputs A and B are first combined into a single beam. The transmitted intensity is defined as the O1 output and the reflected value as the O2. We bias the hardlimiter at a limiting value a=1. If one of the inputs is 0 and the other 1, the output at O1 is 1 and at O2 is 0. If both inputs A and B have the value of 1, a 1 is transmitted and 1 reflected. Thus, O1 yields the result of an OR operation.
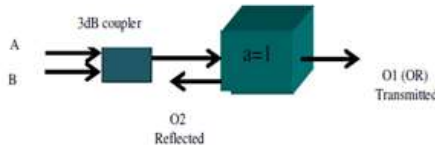

Fig. 5. All Optical OR gate [13].

4.2. All optical JK flip flop

The structure of the all-optical J-K flip-flop memory is depicted in Figure 6. It is consists of all optical flip flop based on two coupled polarization switches [2, 14] and a set of all optical logic gates based on the hardlimiters that are added to convert it into JK flip flop [15]. The first PSW1 outputs light that is injected into the second PSW2. Hence, the light that PSW1 outputs acts as a saturating control signal for SOA2 that can suppress PSW2 and the light that PSW2 outputs can act as a saturating control signal for the SOA1 to suppress PSW1. The optical pulses are injected into PSW1 via Port I of PBS (polarization beam splitter) to set the flip-flop in State1. The optical pulses are injected into PSW2 via Port II of PBS to reset the flip-flop in State 2 [14]. The hardlimiters shown in Figure 5 are biased at a limiting value a=3 to obtain optical AND gates with three inputs [15]. The output Q is applied to the AND gate with K terminal and clock pulse CK inputs. The flip-flop is cleared during a clock pulse if Q was previously 1. Similarly, output Q' is applied to AND gate with J terminal and clock (CK) inputs, and the flip-flop is set with a clock pulse if Q' was previously 1. Inputs J and K behave like inputs S and R to set and clear the flip flop [14]. The T flip flop can be obtained from a J-K type if both inputs are tied together [16]. The truth table of J-K flip flops is depicted in Table 3. The logical expression of the inputs Set (S) and Reset (R) can be expressed as:

$$S = Q'_n \cap J \cap Ck \tag{2}$$

$$R = Q_n \cap K \cap Ck \tag{3}$$
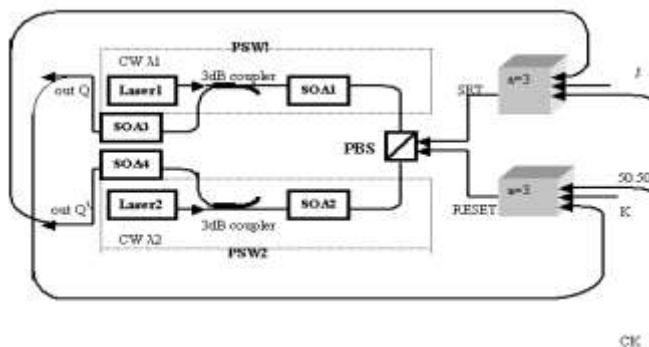
Fig. 6. All optical J-K flip flop based on two coupled polarization switches and optical gates.

Table 3.
The truth table of JK flip flop

J	K	Q_{n+1}	Q'_{n+1}
0	0	Q_n	Q'_n
0	1	0	1
1	0	1	0
1	1	Q'_n	Q_n

5. All optical implementation of OVSF code generator

This section introduces the design of overall optical implementation, experimental results, and the simulation analysis of the OVSF generator. The design of generator is based on the logic design depicted in Figure 2 and 3 by using the proposed optical components in Section 4. The performance and accuracy of the design of the optical circuit is evaluated through experimental and numerical simulation to confirm its feasibility in terms of the choice of the critical parameters.
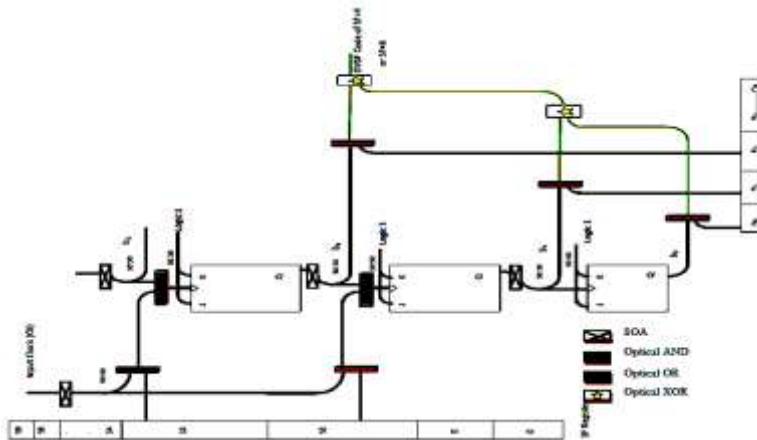
Fig. 7. The overall all optical OVSF code generator including the ripple counter of T flip flops, SF register, and optical gates

Figure 7 shows a section of the circuit diagram of all-optical OVSF code generator, it consists of a cascaded all-optical JK flip flops, and a set of optical hardlimiter AND gates, OR gates, and XOR gates which is equivalent to modulo 2 adder. The two inputs J and K of each flip flop are tied together to obtain a T flip flop, and this common input is set by logic input 1.

SOA's (semiconductor optical amplifier) are used to compensate the losses of the cascaded connections between flip flops and optical couplers of 50:50 by adjusting the SOA current injection from 40 mA to 60 mA for different SOAs [17]. This injected current is used to control on the gain of SOA.

In order to calibrate and validate the model, experimental results were used. The theoretical parameters were heuristically refined until the best agreement between simulation and experiment, and the values are presented in Table 4, for a central wavelength of 1550 nm.

Table 4.

The theoretical parameters of SOA

Parameter	Definition	Value
w	Cavity width	1.35 μm
d	Cavity height	0.21 μm
l	Cavity length	670 μm
a	Transversal section gain	1.29×10^{-16} cm^2
N_{tr}	Transparency carrier dens.	2.1×10^{18} cm^{-3}
α	Attenuation	2100/m
R	Facet reflection	0.0001
β	Line-width enhancement factor	5
n_{ef}	Effective refractive index	3.414
$α_{ins}$	Total insertion loss	6.3dB
E_{sat}	Saturation energy	1.25 pJ
Γ	Confinement factor	0.39

The outputs of SF register are applied to optical ANDs with the external clock to control the counting of optical counter according to Table 2. The optical counter consists of a series of optical T flip flops based on two coupled polarization switches which are presented in Section 4.2. The output of counter is optically AND with the identification code N. The outputs of all optical ANDs are applied to XOR gates according to Eq.(1) to finally obtain the OVSF code.

The OVSF code is numerically simulated using Beam Prop method V.7 and Optowave simulation program V.2. The wavelengths of each flip-flop are 1550 nm for $λ_1$ and 1552 nm for $λ_2$. There is an external light input at wavelength of 1600 nm ($λ_3$) which is injected as a clock pulse (CK). The optical clock pulses are injected approximately at every 0.1 ns with clock speed of 9-10 GHz with duration equal to 0.05 ns.

Figure 8 shows the result backed by the simulation results of optical OVSF generator $C_{8,6}$ at SF=8, where the identification number is $N=6=n_3n_2n_1n_0=0110$ and the SF register code is adjusted at 0000001000. At *SF*=8, the counter is counting incrementally from 0 to 8, where b_8 is always the MSB, and the LSB is b_6 as shown in Figure 8. The logic expression of OVSF code at this case can be expressed as:
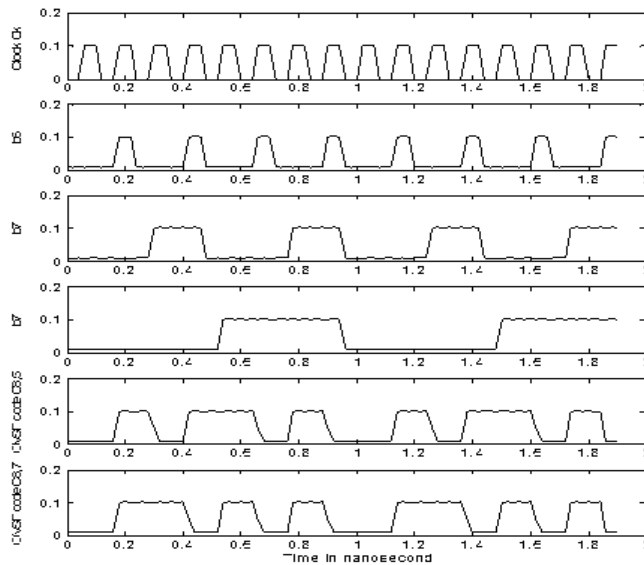
$$OVSF\ Code = (n_0 \cap b_8) \oplus (n_1 \cap b_7) \oplus (n_2 \cap b_6) \qquad (4)$$

The outputs of OVSF code generator of $C_{8,5}$ and $C_{8,7}$ for N=5 and N=7 respectively are depicted together in Figure 9.
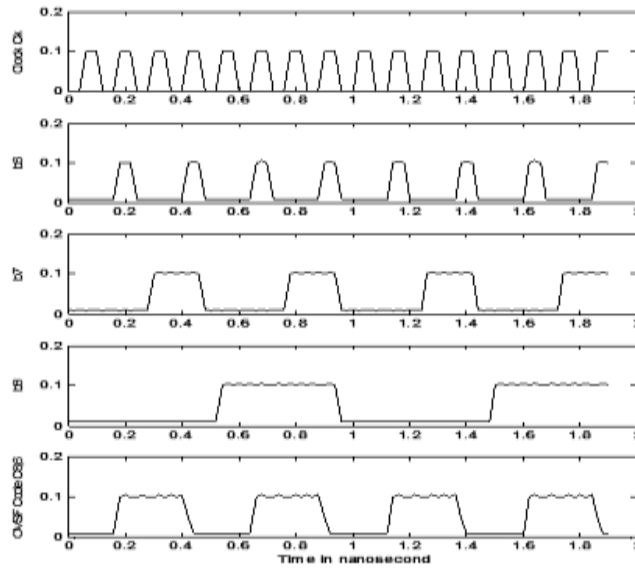
Fig. 8. The numerical simulation output code $C_{8,6}$ at N=0110 with *SF*=8 and counter range b_8 b_7 b_6 (0-8).

Fig. 9. The numerical simulation output codes $C_{8,5}$ and $C_{8,7}$ at N=0101 and N=0111 respectively.

6. Conclusion

In this paper, we have proposed and described all-optical schemes for OVSF code generator of spreading factor range *SF*=4-512. The generator consists of a series of optical T flip flops based on two coupled polarization switches, and a set of optical logic gates. Numerical simulation results confirming the described method are given. The theoretical model is developed and the results obtained experimentally backed by the numerically simulation result will be useful in the future for using the OVSF code tree techniques in all-optical computing and optical information processing to supports a lot of users in the optical communication links.

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الملخص العربى

معامل الأنتشار متعامد التغير (OVSF) يقوم بتقديم معدلات متغيرة للبيانات ويدعم العديد من التطبيقات المختلفة مع العديد من النطاقات الترددية المختلفة.حيث تقدم هذه الورقة مولد رمزي بصري ل OVSF باستخدام البوابات الضوئية ومجموعة من التأرجحات الضوئية القائمة على اثنين من مفاتيح الاستقطاب (PSWs). و يساعد المولد الرمزي OVSF الضوئي على استخدام تقنية كود OVSF في مجال الاتصالات البصرية. وتناقش الورقة التصميم العام للمولد والنتائج من خلال المحاكاة العددية باستخدام الحاسب الألي لتأكيد جدوى التصميم من خلال عاملي الانتشار 4 و 8 .