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WIDEBAND ANALOG VLSI IMPLEMENTATION OF ARTIFICIAL NEURAL NETWORKS

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This paper presents an analog VLSL circuit for implementation of Artificial Neural Networks (ANNs). The building blocks of the proposed circuit include Differential voltage current controlled source (DVCCS), Super MOSFET and Differential voltage controlled voltage source (DVCVS) which are used to multiply incoming analog signals with variable weights, and current in / current out sigmoid function circuit. The proposed circuit can be easily implemented in a 0.34 μ m CMOS VLSI process. Simulations are presented to confirm the validity of the proposed circuit.

KEYWORDS: *ANNs, Analog VLSI, DVCCS, Super MOS and DVCVS.*

NOMENCLATURE

I_{IN}	input current to the neuron	V_{GS}	gate to source voltage
X_i	input signal	V_T	MOSFET threshold voltage
W_i	synaptic weight	$U(t)$	current step function for system causality
I_{bias}	bias current		
Yi	action potential	G_n	DVCCS transconductance
$F(Y)$	activation function	I_{DVCCS}	output current of the DVCCS
I_{sat}	MOSFET saturation current	I_{out}	neuron output current
μ	electron mobility	K	current mirror gain
C_{ox}	oxide gate capacitance	Z_n	input voltage of the of the sigmoid function
ω/L	channel width/length		

I- INTRODUCTION

Artificial Neural Networks (ANNs) originally inspired by the computational capabilities of the human brain, refer to a variety of computing architectures that consist of massively parallel inter connections of simple processing elements. Analog VLSI (very large scale Integration) of artificial neural networks with computational intelligence has received much attention lately [1], [2]. The advantages of using analog VLSI as technology medium for special purpose neural network implementations include the inherent parallelism of the summing operations, the compact size, and low power consumption [3], [4]. The drawbacks attributed to analog VLSI, in general, are the limited available dynamic range and the channel length modulation effect through the early voltage [5].

On the other hand, Operational amplifiers (op-amps), as voltage amplifiers are not generally adequate in VLSI for ANNs, due to a considerable chip area and design expertise required.

The basic idea of the neuron is placed upon combining the incoming signals from other neurons which called synaptic weights and Bias is usually added to shift values along the input axis, then activation function which may be sigmoid function limits the amplitude of the output. The proposed analog VLSI-ANN cell consists of synaptic weights, implemented by transconductance amplifier, summation of the weighted signals, activation functions are realized by amplifier nonlinearities and capacitors are used for smoothing the transition from an initial state to a desisted equilibrium.

In this paper we primarily focus on the three major building blocks needed for a neuron. Differential voltage current controlled source (DVCCS) for making synaptic weights and the Differential voltage controlled voltage source (DVCVS) by directing DVCCS output current into a resistor. However, one of the best ways to do this is to attach the gates of a CMOS pair on to the output of the DVCCS. Since the CMOS pair allows no current at its inputs, the DVCCS can of course no longer act as a current source but its output voltage is determined by other factors (especially, the channel length modulation effect through the Early voltage). Therefore, the third building block is a Super MOSFET, where the effect of the channel length modulation parameter is drastically reduced. Because of each neuron output needs to be sent to each of the other neuron, the output current needs to be repeated many times, this being accomplished by the bidirectional current mirrors. Super MOSFET can also be used in perfect matched current mirror [6], [7].

The paper is divided up into several sections. Section II presents the genetic description model. Analog VLSI neuron is presented in section III, simulation results are discussed in section IV, and finally conclusions are presented in section V.

II- GENETIC DESCRIPTION MODEL

The main function of the neuron (node) is combing incoming signals from other neurons, then an activation function which may be a sigmoid function limits the amplitude of the output. Fig 1 shows the basic concept of the neuron (node).

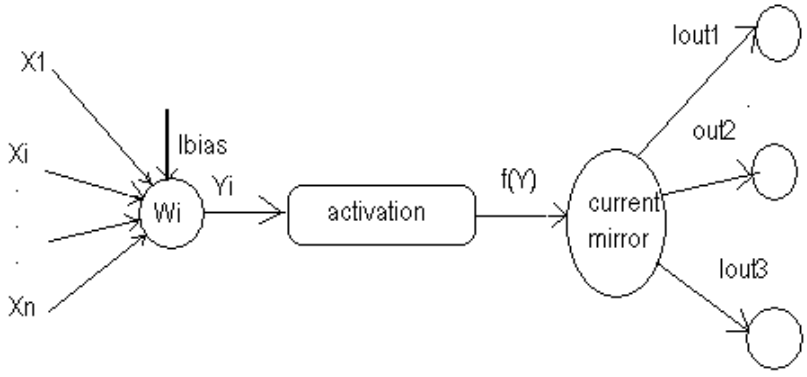


Fig.1. The basic concept of the neuron (node)

The genetic model of the neuron where the main function is combining the input signals from other neurons, by summing weights:

$$Y_i = \sum_{i=1}^{n} X_i W_i \quad \text{.....(1)}$$

A bias current is usually added to shift values along the input axis:

$$Y_i = I_{bais} + \sum_{i=1}^{n} X_i W_i \quad \text{.....(2)}$$

The activation function that limits the amplitude of the output is given by:

$$f(Y) = \frac{1}{1+e^{-Y}} \quad \text{.....(3)}$$

If the short channel MOSFET is operating in the saturation region, we have a quadratic behavior, that is :

$$I_{sat} = (\mu C_{ox} \varpi / L)(V_{GS} - V_T)^2 \; U(t) \text{.....(4)}$$

The output current from the neuron after limiting the amplitude from the sigmoid function and the gains from the current mirrors becomes:

$$I_{out} = KI_{DVCCS} \quad \text{.....(5)}$$

Fig. 2 represents the analog VLSI neuron, whose output is themselves feed back via cross ban connections. Straight for ward analysis leads to [4], [5]:

$$C_n \frac{dZ_n}{dt} + G_n Z_n = \sum_{n=1}^{n=N} X_i w_i + I_{bias} \quad \text{.....(6)}$$

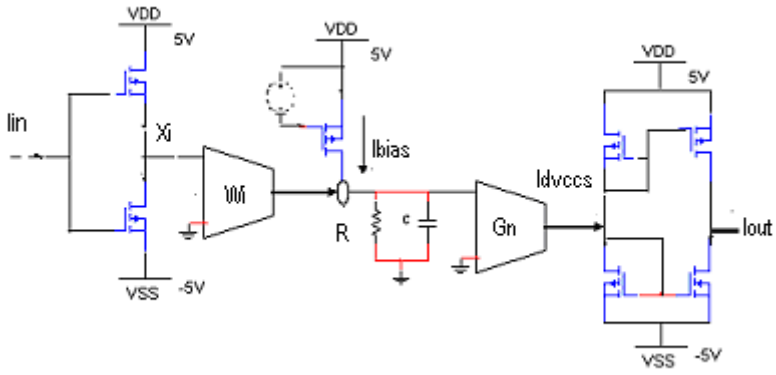


Fig. 2 circuit diagram of the analog VLSI-neuron

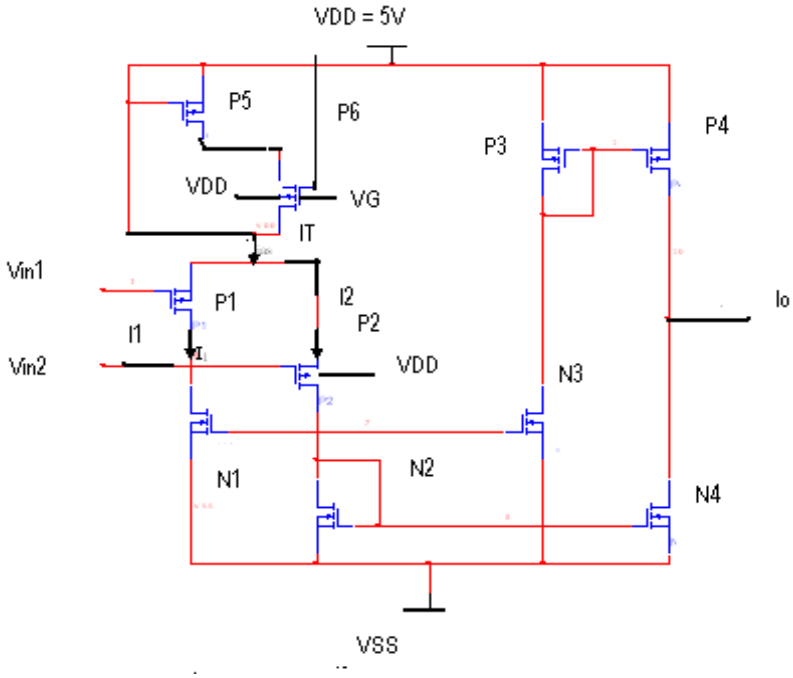
III. ANALOG VLSI – NEURON

III. A. Differential Voltage Current Controlled Source (DVCCS)

The transconductance amplifier is a device that generates at its output a current that is a function of the difference between two input voltages V_1 and V_2 as shown in Fig.3. The

differential pair at an input stage are used as a current source, under normal circumstance, its drain voltage is large enough that the drain current is saturated at a value set by the gate voltage V_g. The three current mirrors are used to generate an output current that is proportional to the difference between the two differential drain currents.

All transistors operate in the saturation mode for the specified output current level. We notice that the transconductance G is proportional to the bias current, a fact that will become apparant when the amplifier is used to produce a voltage type output [7].



F:g.3. Wideband tronsconductance amplifier

III.B Differential Voltage Controlled Voltage Source (DVCVs)

In some instances it is necessary to convert the output current of a DVCCS into a voltage giving a Differential voltage controlled voltage source (DVCV) as when output voltage for an activation function is desired. Such can be accomplished by directing DVCCS output current into a resistor, or generated by by other DVCCS or an MOS transistor. However, one of the best ways to do this is to attach the gates of a CMOS pair that allows no current at its input, the DVCCS can of course no longer act as a current source but its output voltage is defer mined by other factors, specially, the channel length modulation effect through the Early voltage .

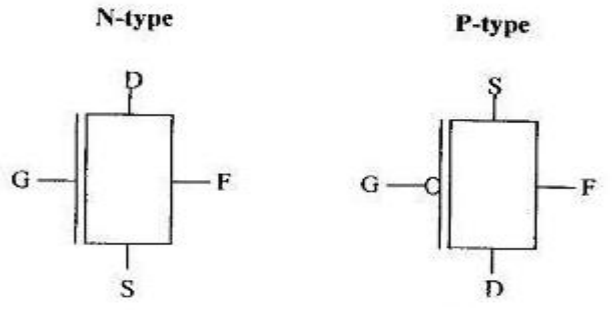
These drawbacks are eliminated using the Super MOSFET [8], which is self biasing and easier to design. Moreover, the Super MOS has high gain-boosting techniques and needs a single power supply. On the other hand, the influence of the channel length modulation parameter on the drain current and the output conductance of the small signal model is drastically reduced.This means that the Super MOS also be

can used in a perfect matched current mirror. This ensures a low saturation voltage of the Super MOS. On the other hand, the effect of the early voltage is usually negligible in digital circuits but can be significant in analog circuits. The single MOS transistor exhibits an Early voltage of approximately less than 5V [9].Also, a super MOS whose threshold voltage is mask programmable through changing the dimensions of a single transistor has the following relation [9]:

$$V_T = K_1 - \frac{K_2}{\sqrt{W_3}} \quad \text{.....(10)}$$

Where V_T is the threshold voltage of the super MOS and W_3 is the width of N_3 MOSFET K_1 and K_2 are material constants.

4(a)



4(b)

Fig. 4 (a) N Type super MOS. (b) super MOS symbols

A CMOS pair that consists of Super NMOS and Super PMOS is designed. Because each neuron output current (which can be positive or negative) needs to be sent to each other neurons, it needs to be repeated many times, this being accomplished by the bidirectional perfect matched current mirror. These simply reproduce many copies of the neuron output current irrespective of what loads is presented to it. The perfect matched current mirror uses super MOS could be easily achieved especially it has very high output impedance. The circuit diagram of the proposed analog VLSI neuron is shown in Fig. 5.

IV. SIMULATION RESULTS

TO confirm the validity of equation (1), the proposed analog VLSI neuron of Fig. 5 was simulated using HSPICE. In the simulation V_{DD} was set at 5 volts, the scaling factor of the current mirror was chosen to be 0.1. The maximum allowable output current was ± 100 μA, I_{out} was also Limited to approximately + 10 μA , Fig. 6 shows the simulation results of the input weight voltage against the full supply range.

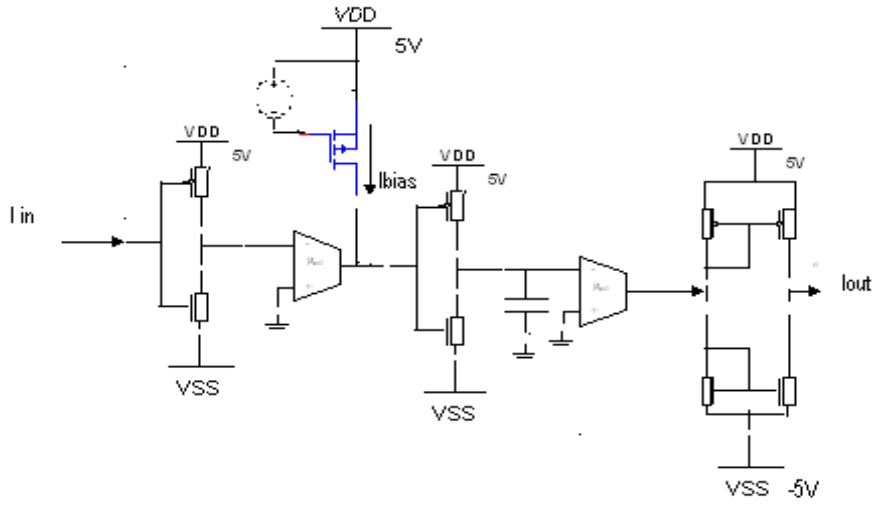


Fig.5. Circuit diagram of the proposed analog VLSI neuron

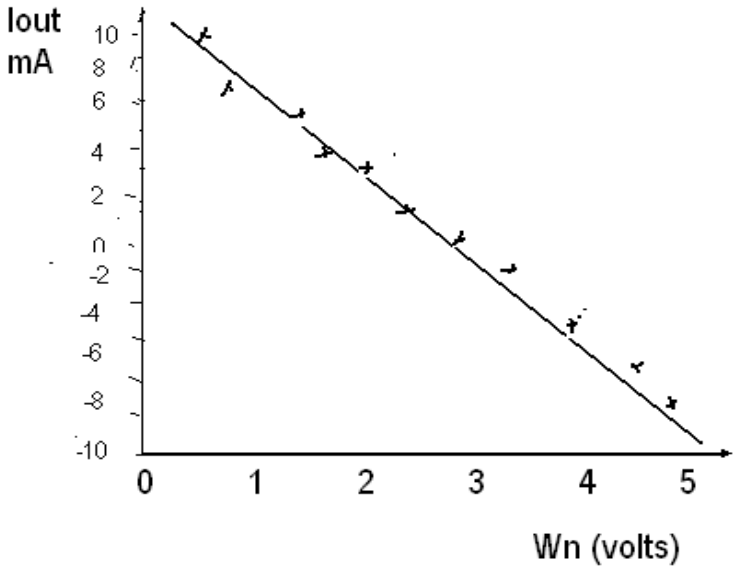


Fig 6. HSPICE simulation result of output current against the input weight voltage

It can be clearly seen that the curve is Linear and symmetrical about the differential voltage current controlled source. The values of threshold voltage and transconductance parameters can vary wildly due to processing spread. AC analysis is carried out to get the circuit gain and bandwidth which is inherently high in current mode operation. Analysis is carried out by considering the parasitic capacitances of all MOSFET. Junction areas and perimeters are estimated according to the layout design rules for 0.34 μm CMOS technology. Figure 7 shows the activation function of the neuron circuit obtained using HSPICE simulation.

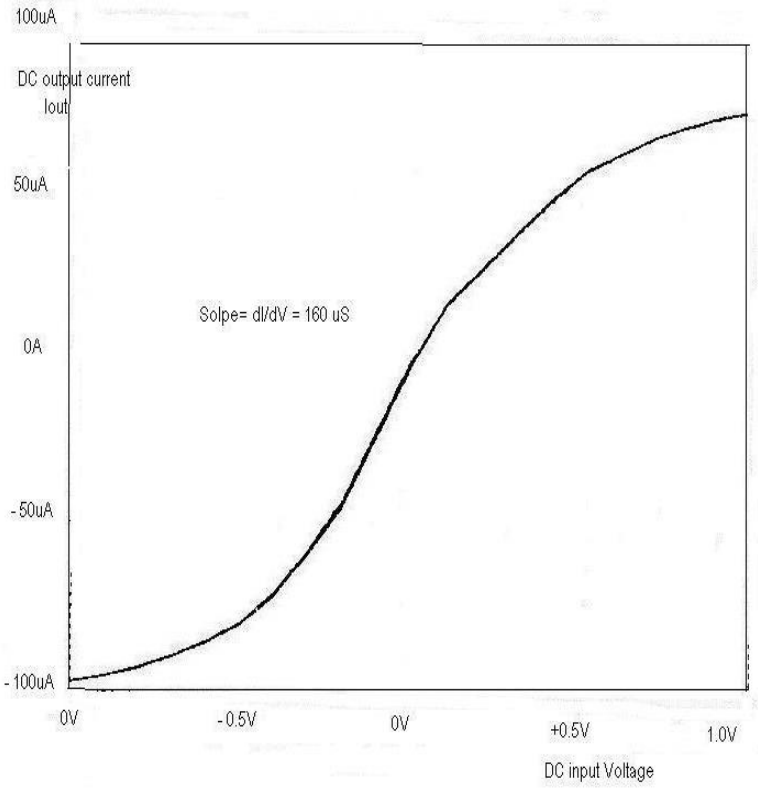


Fig. 7 Activation function of the neuron circuit

V. CONCLUSIONS

Analog VLSI Circuits suitable for implementation of artificial neural networks have been presented and analyzed. The circuits have been primarily designed for neural networks that communicate with analog signals. All the circuits are confirmed by HSPICE. Simulation using 0.35μm CMOS technology. The proposed DVCCS circuit has many advantages over the simple Transconductance. The obtained band width reaches 400 MHz which is suitable for wide band operation neural networks. The output driving current capability is sufficiently high for driving large capacitive loads. The Super MOS whose threshold voltage is mask programmable through changing the dimensions of a single MOS [9]. Therefore, programmable and modular artificial neural networks can be built using the proposed circuits.

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REFERENCES

[1]. Mohamed .Alazab " Modeling and Simulation of a new VLSI analog circuit for Artificial Neural Networks Applications , Proceeding of the 1-th ASAT conference, pp 300-309, 29-31May007,Cairo,Egypt.

[2] Kazuokiguchi, etal," Neuro- Fuzzy control of A Robtic Exoskeleton with EMG signals ", IEEE Transactions on fuzzy systems, vo1.12. No.4, pp 310-319, august 2004.

[3] Valle M., " Analog VLSI implementation of Artificial Neural Networks with supervised on-chip learning" , Analog Integrated circuits and signal processing, Vol. 33, No. 3 December 2002 " pp.263-287(25).

[4] Silvio P. , etal Analog VLSI Neural Networks: Impale mutation Issues and Examples in Optimization and super uised learning", IEEE Transaction on industrial electronics, vol.59,No. 6, pp611-618, December 2002.

[5] Robert w. Newcomb and Jason D.Lohn" Analog VLSI for neural networks", handbook of Brain theory and neural networks, M Arbib Ed , Brad ford books, MIT press, 1995.

[6] Iwata, A. Moreie, etal, " Merget Analog – Digital circuits using Pulse Modulation for Intelligent SOC applications. IEICE transaction Fundamentals, E84-A, 486-496 (2001)

[7] Gert Cauwenberghs, " Ananalog VLSI Recurrent Neural Learning a continuous – time trajectory", IEEE transactrons on neural networks, vol, No. 2, pp 401-409, March 2000

[8] Mohamed . Alazab," Design and simulation of awide band CMOS transcenductance Amplifier", 16th National Radio science conference, NRSC, 99 (URSI seuies), pp121-129, Ain Shams Univ. Cairo , Egypt, Feb.23-25-,1999

[9] Mohamed . Alazab, H F. Ragaei " Mask Programmable VT with super MOSFET" , Sci. Bull . Fac .Eng. Ain Shams Univ. , Cairo, Egypt. Vo1.32,No3, pp 45-55, Sep30 1997

تصميم الخلايا العصبية بتكنولوجيا الدوائر متناهية الصغر

يقدم هذا البحث نموذج لخلية الدوائر المتكاملة متناهية الصغر وتستخدم في تطبيقات الخلايا العصبية الصناعية, وتمت محاكاة الدوائر وتحديد خواصها بدقة مقبولة إلى جانب الاستخدامات المتعددة في مجالات الإنسان الالى والدوائر التماثلية.