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Comparative Analysis between Two Different Control PWM Techniques Based on a Reduced-Component Multilevel Inverter

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Abstract This paper focuses on the implementation of two pulse width modulation (PWM) techniques on a reduced-component multilevel inverter which reduced the number of power switches along with the voltage sources used. The reduced components multilevel inverter has two circuits; level circuit and polarity circuit. The level circuit is used for producing voltage levels, whereas polarity is a conventional H-bridge used for reversing output voltage levels. The reduction in harmonics is primarily dedicated by the switching technique used to control the power switches. In this paper, two PWM techniques were applied to the presented inverter to investigate the change in the switching signal period on ripple contents and total harmonic distortion (THD) with a closed-loop voltage control system. In the closed-loop system, a conventional PI controller is used to regulate the load voltage to achieve an output voltage near to sinusoidal. MATLAB/SIMULINK has been used to analyze the overall performance of the multilevel inverter based on seven-level operation under both PWM techniques. The simulation results show that the first PWM technique, which has a low switching time for the power switches, has an influence on the THD and the ripple content by about a 6 percent reduction compared with the second technique.

Keywords: PWM; Seven-level Inverter; Single phase; THD; Voltage Control.

1 Introduction

Power electronics development has drawn much of the researcher's attention for its high performance and power capability [1]. This development has made it possible to create pulse width modulation (PWM) inverters that can control voltage and frequency. As a result, the use of power electronics has increased significantly in more industrial applications such as renewable energy systems [2], [3], uninterruptable power supplies (UPS) [4], flexible AC transmission systems (FACTS) [5], motor drives [6], etc., to improve the performance of these applications.

The three-level H-bridge PWM inverter circuit is the first circuit of dc-ac converter topologies [7]. As a result of the need for low total harmonic distortion (THD) and high efficiency, a demand for high voltage rating multilevel inverter (MLI) has grown. Another significant benefit for MLI is the absence of high-rated step-up transformers for high voltage applications.

The stepped output voltage from MLI presents a voltage shape very similar to the sinusoidal waveform; consequently, THD, dv/dt stress, and output filter size are reduced [8]. Mainly, the three most popular MLI topologies are diode-clamped MLI, flying capacitor MLI, and cascaded H-bridge MLI [8]–[10]. All these common topologies suffer from a high number of switching devices and result in high switching losses, low efficiency, and high overall topology costs for higher rated applications.

The most challenging issue is how to achieve low THD output voltage, low filter circuit, low cost and high efficiency. In this case, a reduction in the number of switching devices components is considered to be the solution to this problem. Recently, several topologies have been recommended as a replacement for the familiar topologies of MLI. Each topology has shown its effective solution to one or more of the aforementioned problems related to the common traditional MLI topologies.

The key element for the use of MLI is the harmonic content which is determined by the proper switching for each switch forming the topology used. This paper

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introduces two PWM techniques based on different control and generation of different voltage levels in order to demonstrate how this affects them.

This paper is structured as follows: Section 2 addresses the construction of a reduced-component multilevel inverter used in the study of the two PWM techniques and the operation of seven-level topology. The switching scheme of the two PWM techniques is demonstrated in Sections 3. The voltage regulation scheme is set out in Section 4. Section 5 discloses the validity of the proposed inverter using MATLAB/SIMULINK. This work is concluded in Section 6.

2 A Reduced-Component Multilevel Inverter

2.1 Circuit Configuration

The illustration of a reduced-component multilevel inverter is shown in Fig. 1 as set out in [11], [12]. It has two circuits; the level circuit and the polarity circuit. The level circuit comprises of "*n*" cells with each cell, from the 2nd to nth cells, having one voltage source and one IGBT switch without an antiparallel diode, but, the 1st cell has one source and one switch along with its antiparallel diode is used for the output of the first level, in contrast, the IGBT switch is used for the freewheeling path in case of inductive loads. This circuit is responsible for producing various voltage levels for the inverter terminal. On the other hand, the polarity circuit is called a traditional three-level H-bridge circuit whose key functions are to control the polarity of the voltage levels and to produce the zero voltage level.

2.2 Operational Principle of Seven-level

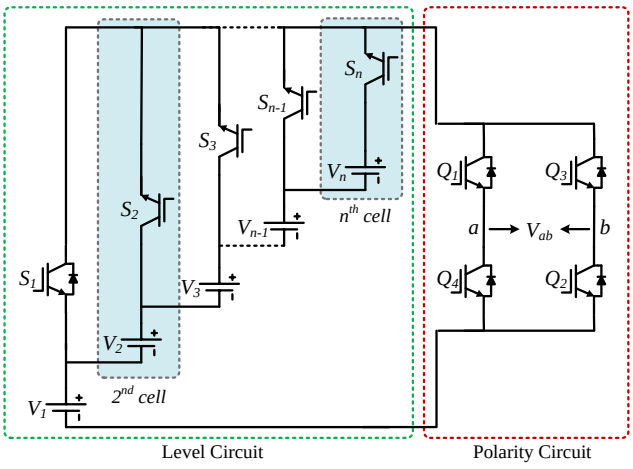


Fig. 1 Circuit configuration of the reduced-component inverter

For seven-level topology, the inverter has three cells including three symmetrical voltage sources i.e., $V_1 = V_2 = V_3 = V_{dc}$ and seven IGBT switches that control output voltage levels. The seven output levels are $+V_{dc}$, $+2V_{dc}$, $+3V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$, and $-3V_{dc}$. The output voltage from the inverter has nine states depending on the switches in the ON state as listed in Table 1. Besides, to understand the turning ON and OFF of each switch, Fig. 2 summarizes the current direction of the seven-level generation.

Table 1 Switching combination of seven-level inverter

State	Inverter output voltage (V_{ab})	Direction of load output current (I_{out})	Switches in ON state
a.	$3V_{dc}$	Positive	S_3, Q_1, Q_2
b.	$2V_{dc}$	Positive	S_2, Q_1, Q_2
c.	V_{dc}	Positive	D_{S1}, Q_1, Q_2
d.	V_{dc}	Negative	S_1, D_{Q1}, D_{Q2}
e.	0	Positive	Q_1, D_{Q3}
f.	$-V_{dc}$	Negative	D_{S1}, Q_3, Q_4
g.	$-V_{dc}$	Positive	S_1, D_{Q3}, D_{Q4}
h.	$-2V_{dc}$	Negative	S_2, Q_3, Q_4
i.	$-3V_{dc}$	Negative	S_3, Q_3, Q_4

3 Switching PWM Algorithm

The ON and OFF modes of each switch and the switching frequency (F_{SW}) are the key contributors to harmonic content of the produced output voltage. In the following subsections, two PWM techniques will be shown to present the effect of the switching method on THD. The switching pattern used to produce a seven-level output voltage is created by comparing a rectified sinusoidal reference signal (V_{ref}) has a frequency of the required output voltage with triangle carrier signals. The numbers of carrier (N_{car}) are determined by the following equation:

$$N_{car} = (N_l - 1)/2 \quad (1)$$

Where; N_l is the number of voltage levels required. In this case, for seven-level voltage, three carrier signals are needed for each PWM Technique.

3.1 PWM Tech-I

The first PWM technique would have three carrier signals (i.e. V_{car1}, V_{car2}, and V_{car3}). All of these carriers have the same F_{SW} value, the same peak value but different in offset voltage as indicated in Fig. 3. The intersection points between V_{car1}, V_{car2}, and V_{car3} with a V_{ref} decide the output voltage levels.

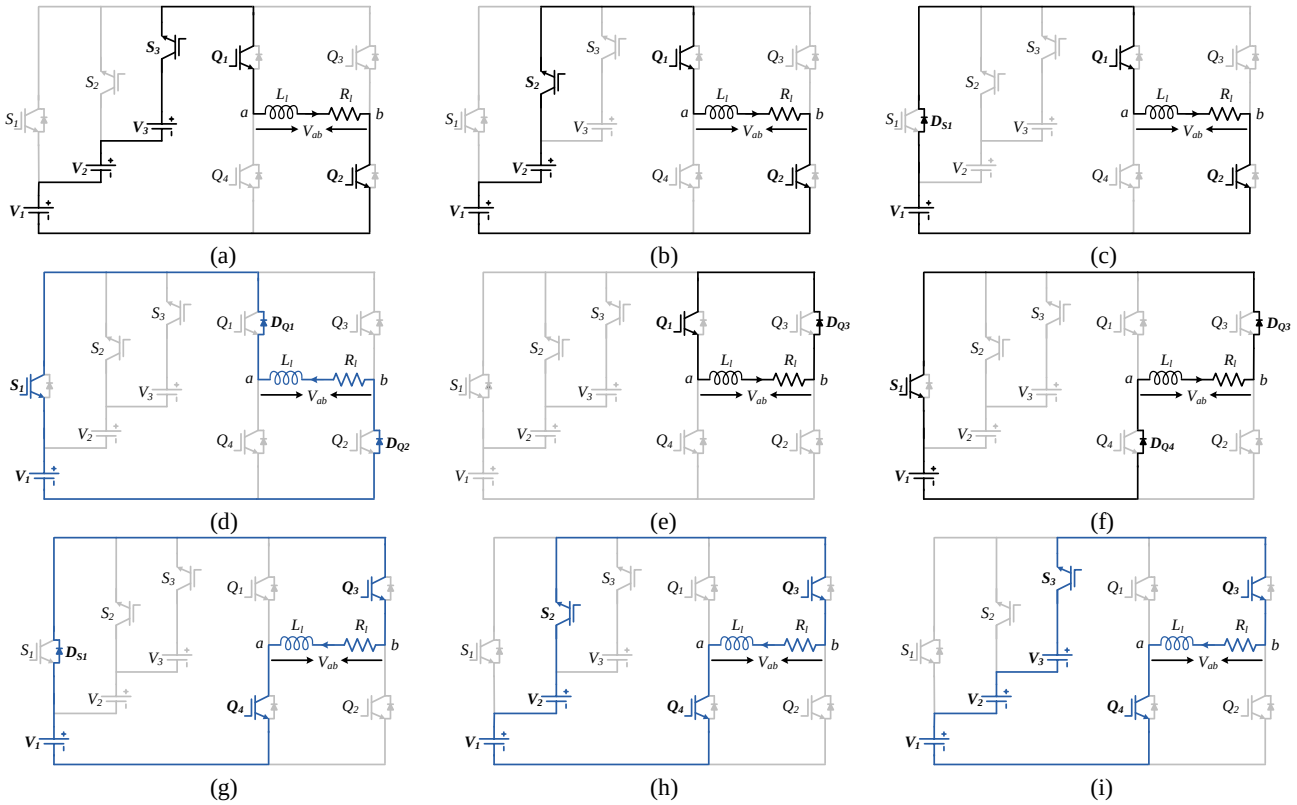


Fig. 2 Current path for generating the seven levels.

The modulation index (*MI*), which will present the number of levels at the terminals of the inverter, can be calculated as follow:

$$MI = A_m /(3 * A_c) \quad (2)$$

Where, A_m is the amplitude of V_{ref} and A_c is the peak-to-peak value of a carrier signal.

When V_{ref} intersects V_{car1}, the C_A control signal is produced and the first output voltage levels, $\pm V_{dc}$, are generated. The second levels, $\pm 2V_{dc}$, of the output voltage are created by intersecting V_{ref} with V_{car2}. Also, the C_B control signal is produced. The last output voltages, $\pm 3V_{dc}$, are generated when the intersection between V_{ref} and V_{car3} occurs and the C_C control signal is generated. The gating signal for each IGBT switch is produced by the proper switching combination. The positive half-cycle of V_{ref} is responsible for generating positive levels while the rectified half-cycle of V_{ref} is responsible for generating the negative levels.

In one cycle, the H-bridge lower leg switches (Q_2 and Q_4) are switched at fundamental frequency, while the H-bridge upper leg switches (Q_1 and Q_3), S_1, S_2 and S_3 are switched at the F_{SW}.

3.2 PWM Tech-II

In this PWM technique, the three carriers have the same F_{SW}, but the peak with no voltage offset is calculated by the following equation:

$$Car_p = Car_n / 2 \quad (3)$$

Where; Car_p is the carrier's peak value and Car_n is the carrier's number. In this case, V_{car1} is the first carrier (Car_n = 1) and the peak value based on Eq. 2 equals to 0.5, V_{car2} is the second carrier (Car_n = 2) and has a peak value equal to 1.0, and finally V_{car3}, the third carrier (Car_n =3), has a peak value of 1.5, as shown in Fig. 4. *MI* here is calculated as following:

$$MI = (2 * A_m) / 3 \quad (4)$$

The generation of each level is the same as that of PWM Tech-I by intersecting V_{car1}, V_{car2}, and V_{car3} with V_{ref} in the same way, and the gating signal for the switches is obtained by an appropriate switching combination.

4 Voltage Control Scheme

The voltage control scheme is a closed-loop voltage regulation for the output voltage. It consists of two parts; the power and control circuit as shown in Fig. 5. The

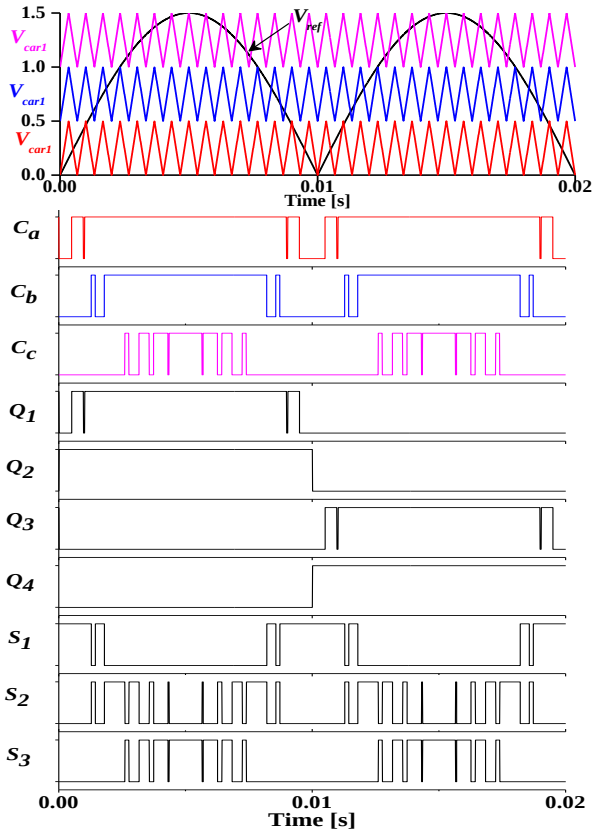


Fig. 3 Switching pattern of PWM Tech-I.

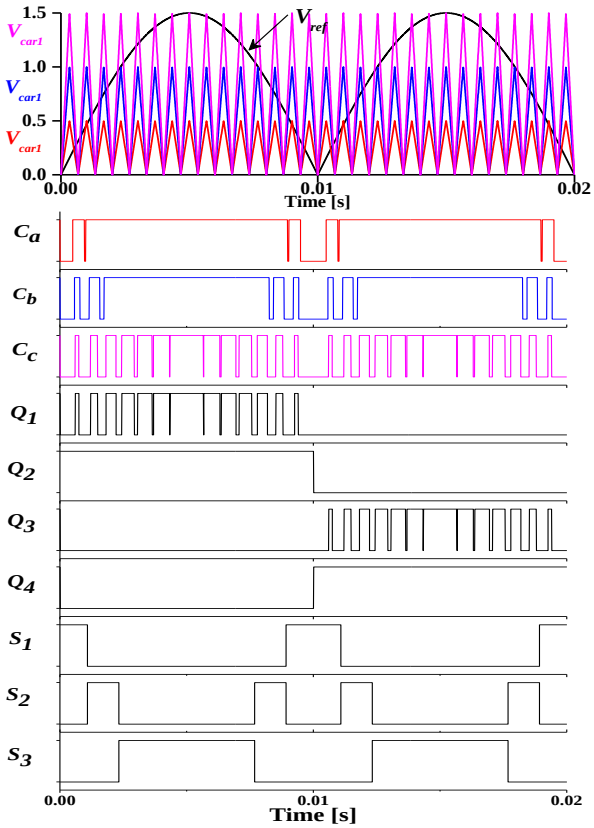


Fig. 4 Switching pattern of PWM Tech-II.

circuit is the seven-level inverter with a simple filter and resistive load, while the control circuit is mainly based on a feedback system using a PI controller. The LC filter is based on the reduction of the ripple found in both the output voltage and the inverter current.

The main function of the PI controller is to control the load voltage (V_L) to be as sinusoidal as the reference voltage (V_R). Therefore an error signal is created by comparing the load voltage with the reference voltage. The error is applied to the PI controller that generates the modulated signal (U) and that signal is applied to one of the two PWM techniques as a reference signal to show the switching states required to generate the inverter levels.

5 Simulation Results

The MATLAB/SIMULINK is designed to present the validity of the reduced-component multilevel inverter during operation with two separate PWM control techniques when connected to the resistive load. The parameters used in the Simulink are listed in Table 2. The results are shown in different *MI* values for generating different voltage levels. The inverter output voltage can be three, five or seven levels, depending on the *MI*. The different *MI* values demonstrate the effectiveness of each PWM technique in controlling the load voltage with respect to the reference value. There are three levels at *MI* below 0.33. *MI* is set from 0.33 to 0.67 for five levels. Seven levels are synthesized to *MI* greater than 0.67. The V_R peak used for the closed-loop feedback system is set to 10 V, 40 V and 70 V in order to obtain different *MI* values (*i.e.* 0.11, 0.44, and 0.77).

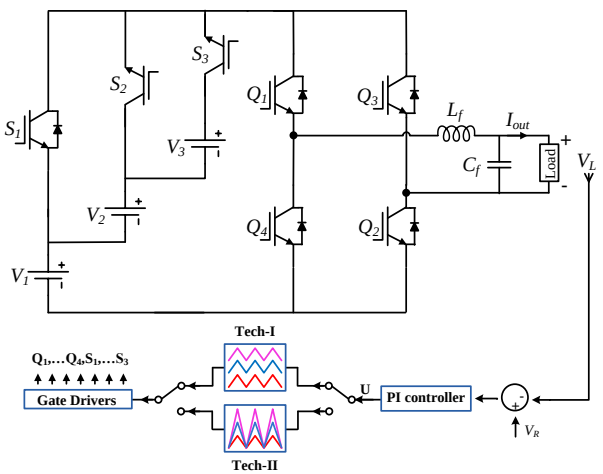


Fig. 5 The closed-loop voltage control scheme.

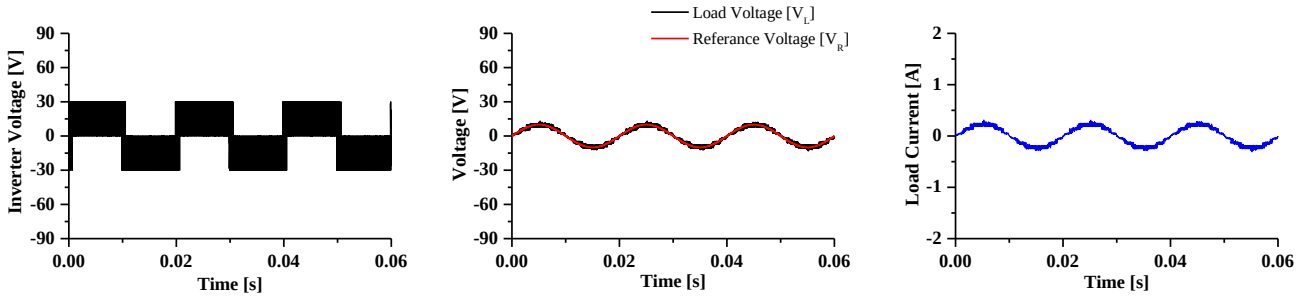
Table 2 Simulation Parameters

Specification	Symbol	Value	Unit
DC power supplies	V_1=V_2=V_3	30	V
Switching frequency	F_{SW}	10	kHz
Fundamental frequency	F_f	50	Hz
Sampling time	T_s	5	µs
Filter	L_f	1	mH
	$C_{\_f}$	3	µF
Load	R_l	42	Ω
PI controller gains	K_p	0.005	A/V
	K_i	10000	A/V.S

5.1 Simulation Results Using PWM Tech-I

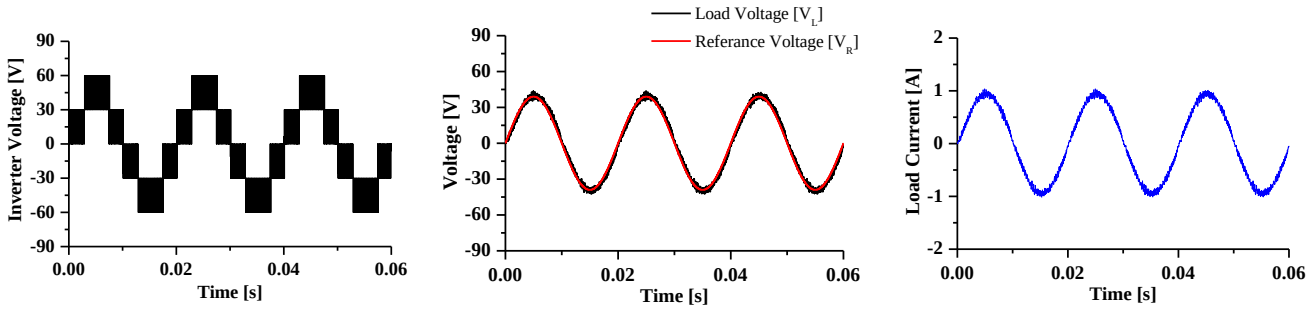
The simulation results for the closed-loop voltage control system for a seven-level inverter with resistive load under PWM Tech-I are shown in Fig. 6, Fig. 7, and Fig. 8.

Fig. 6 presents the results at *MI* < 0.33. The inverter output voltage consists of three levels in the terminal as shown in Fig. 6(a). In Fig. 6(b), reference and load output voltages (V_R, V_L) are presented. As can be seen, the output voltage effectively tracks the reference voltage. Finally, Fig. 6(c) shows the current of the load which is in phase with the load output voltage. Fig. 7 demonstrates the results for *MI* between 0.33 and 0.67. As can be seen in Fig. 7(a), the inverter terminal compromise five levels in addition, V_R and V_L appear identical in Fig. 7(b). Similarity Fig. 8(a) presents seven levels at the terminals of the inverter at MI greater than 0.67. In the same way, Fig. 8(b) and (c) show the reference and load voltages and the load current, respectively.



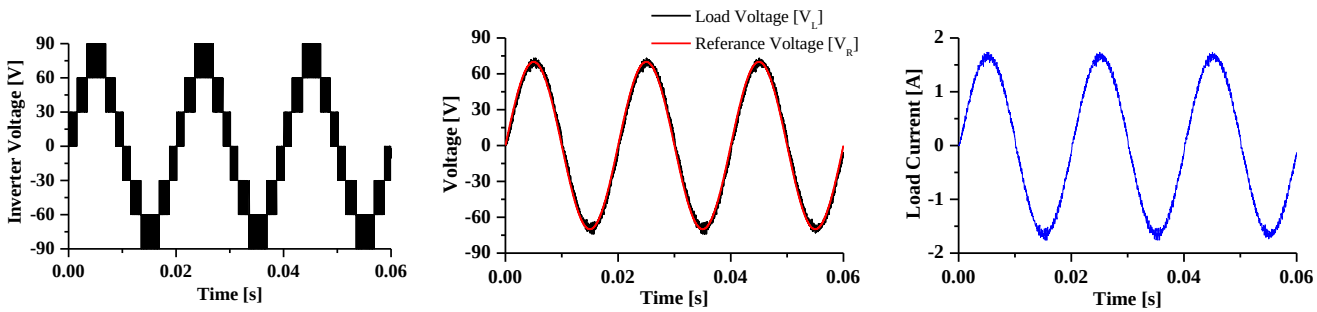
(a) (b) (c)

Fig. 6 Simulation results of the single-phase seven-level inverter using PWM Tech-I at *MI* = 0.11.



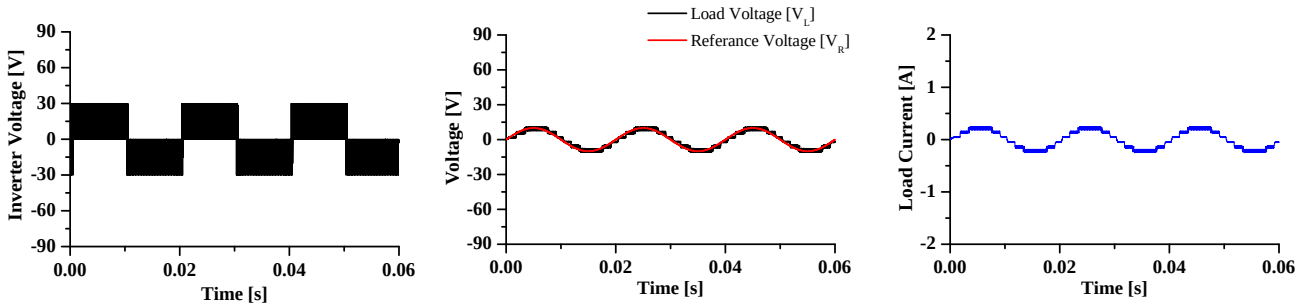
(a) (b) (c)

Fig. 7 Simulation results of the single-phase seven-level inverter using PWM Tech-I at *MI* = 0.44.



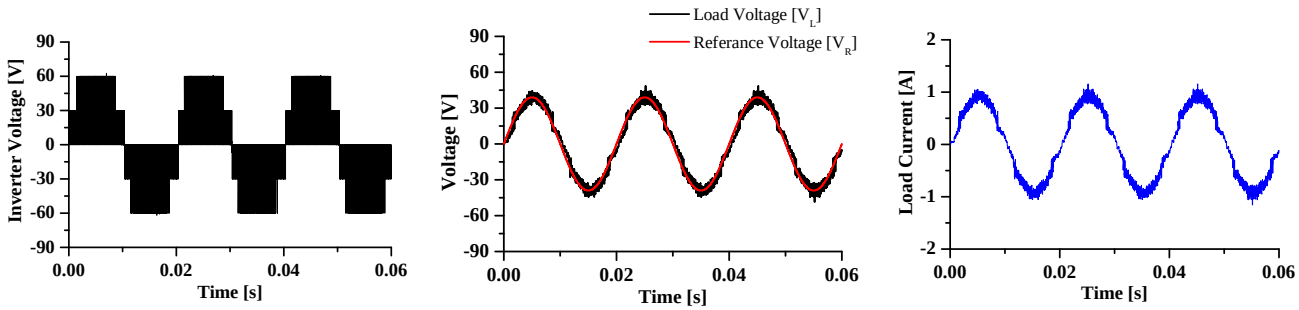
(a) (b) (c)

Fig. 8 Simulation results of the single-phase seven-level inverter using PWM Tech-I at *MI* = 0.77.



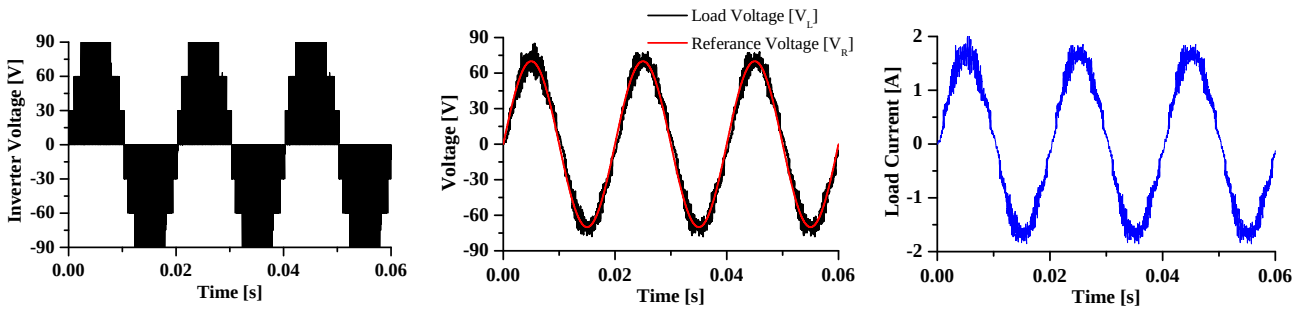
(a) (b) (c)

Fig. 9 Simulation results of the single-phase seven-level inverter using PWM Tech-II at *MI* = 0.11.



(a) (b) (c)

Fig. 10 Simulation results of the single-phase seven-level inverter using PWM Tech-II at *MI* = 0.44.



(a) (b) (c)

Fig. 11 Simulation results of the single-phase seven-level inverter using PWM Tech-II at *MI* = 0.77.

5.2 Simulation Results Using PWM Tech-II

Fig. 9, 10, and 11 display seven-level inverter simulation results using PWM Tech-II. Same as PWM Tech-I, Fig. 9(a) presents three levels at the inverter terminal as *MI* is less than 0.33. Fig. 9(b) presents the voltages for load and reference that are nearly identical. Load current is shown in Fig. 9(c). For 0.33 < *MI* <0.67, Fig. 10 presents the results of simulation to obtain five levels from the inverter. Fig. 10(a) shows the five levels while, Fig. 10(b) displays the load and reference voltages, and finally Fig. 10(c) presents the load current. Fig. 11(a) introduces the inverter's seven-level output voltage before filtering. As can be shown in both techniques, the waveform is not the same due to the change in generating the voltage levels. Fig. 11(b) displays the system reference results and the actual load voltages. The reference and the actual load voltages are almost identical. The waveform of the load current is shown in Fig. 11(c).

However, the ripples in the sinusoidal waveforms of the load voltages and currents are increased due to the rise in the switching time of each power switch. This condition in turn raises the harmonics in both voltages before and after use of the filter.

In order to present the effectiveness of each PWM technique, THD has been determined for both techniques before and after the filter at different *MI* values and the results are shown in Table 3. At *MI* less than 0.33, both techniques present almost the same THD for voltages as the switching period for power switches

under the PWM techniques is the same. However, the inverter exhibits better characteristics under PWM Tech-I compared to PWM Tech-II with low THD in both inverter and load voltage from the deep aforementioned comparisons at *MI* greater than 0.33. The reason for this is that the number of levels has increased and the switching period of the power switches has also changed.

Table 3 Total harmonic distortion for the inverter and output voltages at different values of MI for both PWM techniques

		PWM Tech-I	PWM Tech-II
THD of the inverter voltage (before filtering)	MI < 0.33	84.5 %	84.06 %
	0.33< MI < 0.67	39.41 %	67.32 %
	MI > 0.67	24.13 %	55.68 %
THD of the load voltage (after filtering)	MI < 0.33	14.06 %	15.65 %
	0.33< MI < 0.67	5.29 %	10.99 %
	MI > 0.67	3.39 %	9.85 %

6 Conclusions

In this paper, the performance of two PWM techniques is presented to generate a seven-level voltage using a reduced-component multi-level inverter topology. In all of the two PWM techniques, each technique depends on the duration of the switching signal for each power switch that contributes to the inverter topology used. The effectiveness of each PWM technique is theoretically checked by using MATLAB as a Simulink tool closed-loop system for stand-alone operation. It is clear that the gating method of each switch is the main element for low THD generation. The results show that PWM Tech-I can produce a low THD for the output voltage before and after filtering as the switching period of each power switch is lower than that of PWM Tech-2.

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