Structural, Electrical and Photovoltaic Characteristics of n-ZnSe/ p-GaAs Heterojunction

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Heterojunction of n-ZnSe/p-GaAs devices were fabricated by growing n-ZnSe films onto p-type GaAs using flash evaporation technique. The elemental composition of the prepared films was confirmed by energy dispersive X-ray (EDX) spectroscopy. The morphology and crystal structure of the film were characterized by scanning electron microscopy (SEM) and X-ray diffraction (XRD), respectively. The dark current–voltage (I–V) measurements were performed in the temperature range 300 to 400 K. The measured electrical parameters were used to determine the conduction mechanisms of this heterojunction. The forward current was found to be increased exponentially with the applied voltage in the region of $V \leq 0.3$ V, which was dominated by the thermionic emission over the n-ZnSe/p-GaAs interface. In the region $0.4 < V \leq 1$ V, the current transport was due to the space-charge-limited current controlled by single trap level of 0.29 eV. A free carrier concentration and built-in potential were estimated from the dark capacitance–voltage measurements at 1 MHz. The current-voltage characteristics were also studied for n-ZnSe/p-GaAs heterojunction under illumination and the photovoltaic parameters were evaluated.

1. Introduction:

The growth of the group of II-VI compound semiconductors has attracted considerable attention due to their novel physical properties and wide range of applications in optoelectronic devices [1]. The II-VI group compounds semiconductor films have played an important role in the development of semiconductor device physics. ZnSe has a direct band gap of 2.7 eV and is transparent over a wide range of the visible spectra [2]. The lattice mismatch between ZnSe and GaAs is quite small (0.27%) but the lattice mismatch between ZnSe and Si is quite large (4.4%) [3,4]. Flash evaporation is a powerful method for the deposition of films whose constituents have different vapor pressures [5]. The temperature of the boat is set as high as necessary to evaporate the least volatile component. This instantaneous evaporation prevents fractional decomposition or dissociation of the material, the feed of the powder into the boat should be continuous during the evaporation process [6]. The

parameters which have to be controlled critically are the particle size of the powder, the rate of powder delivery to the preheated boat and the temperature of the boat. This work is relevant with the research activities on electrical properties of ZnSe-based devices for production of photovoltaic electricity.

This work deals with the designing of n-ZnSe/p-GaAs using flash evaporation technique and characterization of this heterojunction. The electronic parameters that control the device performance, such as barrier height, ideality factor, series resistance and shunt resistance were evaluated from the dark current–voltage characteristics. Also, the capacitance–voltage characteristics were studied to give information about the type of this heterojunction. Moreover, photovoltaic parameters were extracted from the I–V characteristics under illumination.

2. Experimental Procedures:

Single crystal of (p-GaAs) wafer oriented at (1 0 0) with a thickness of 0.45 mm and carrier concentration of 10^{22} m^{-3} is obtained from Nippon Mining company. The p-GaAs wafer was etched in a solution containing hydrofluoric acid. After etching, the p-GaAs wafer was immersed and washed with distilled water and finally with ethyl alcohol. The p-GaAs wafer was inserted in a vacuum coating unit and an ohmic contact of back side of GaAs wafer was made by coating it with a thick pure Au film. At the front side of the p-GaAs wafer substrate, a thin layer of n-ZnSe was deposited through a special mask followed by deposition of thin film of pure In. Then, In / n-ZnSe/p-GaAs/Au device was constructed with a photo active area of 0.3 cm^2.

The films of n-ZnSe in this study were deposited by flash evaporation technique on p-GaAs substrates by using a high-vacuum coating unit (model E306 A, Edwards Co.-England); the pressure inside the chamber was pumped down to 5×10^{-4} Pa before starting the evaporation process. A mechanical shutter was used to avoid any contamination on the substrate in the first stage of the evaporation process. The rate of deposition and film thickness were controlled and adjusted during the evaporation by using a quartz crystal thickness monitor (type Edward FTM4)

The structural properties of the films were investigated by X-ray diffraction (XRD), Glancing incidence X-ray diffraction was performed to study the crystallinity of the films using analytical X'Pert PRO MRD diffractometer with CuKα radiation at 0.5◦ incidence angle. The film morphology was investigated by scanning electron microscopy (SEM) using Model Philips XL 30 attached with EDX Unit, with accelerating voltage 30 kV, magnification 10 up to 400,000 and 3.5nm resolution for EDX.

For the current-voltage (I–V) measurements at different temperatures, stabilized power supply and high impedance electrometer (Keithly 617) were used. The room temperature C–V measurements of the device were achieved at 1 MHz by using computerized C–V meter (model 4108, solid state measurements, Inc. Pittsburgh) in air and at dark conditions. The temperature of the sample was recorded during the electrical measurements by using NiCr–NiAl thermocouple with an accuracy of ±1 K. Photocurrent–voltage characteristics were carried out by using halogen lamp. The incident light falls normally on the device through the gold grid from the organic side. The intensity of the light was recorded with a calibrated digital light lux-meter situated in the same position of the sample of interest and calculated as 20 mW/cm^2.

3. Results and Discussion:

3.1. Structural Results:

X-ray diffraction study shows that the deposited ZnSe layer is amorphous as shown in Fig. (1). It is observed that there is a hump in the XRD pattern at $2\theta=25^{o}$. This hump corresponds to the maximum intensity inter-planar spacing 3.243 (Å) of cubic ZnSe [7], of (111) plane.

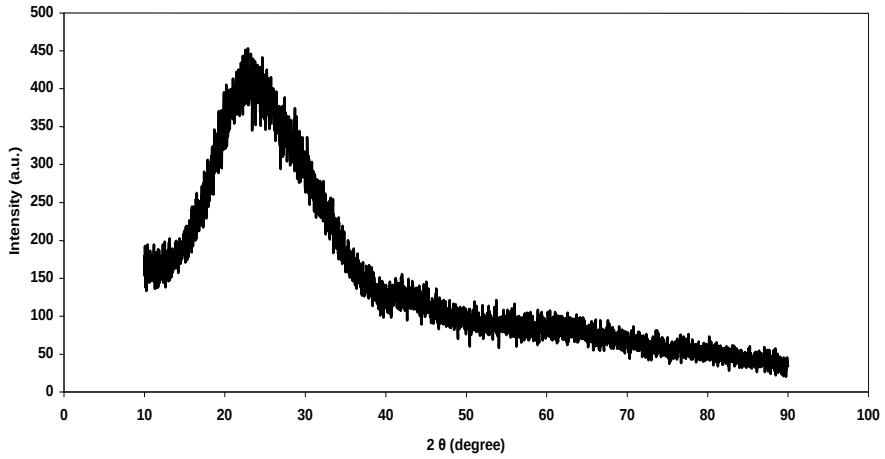

Fig. (1): X-ray diffraction of the deposited ZnSe layer

The surface topography of ZnSe films grown on GaAs single crystalline substrates by flash evaporation using SEM is shown in Fig.(2). There are fine particles grown on the GaAs surface which are nearly ordered but differ in grain size. There are also observed that the particles can be agglomerated to give an inhomogeneous in the grain size of the deposited films.

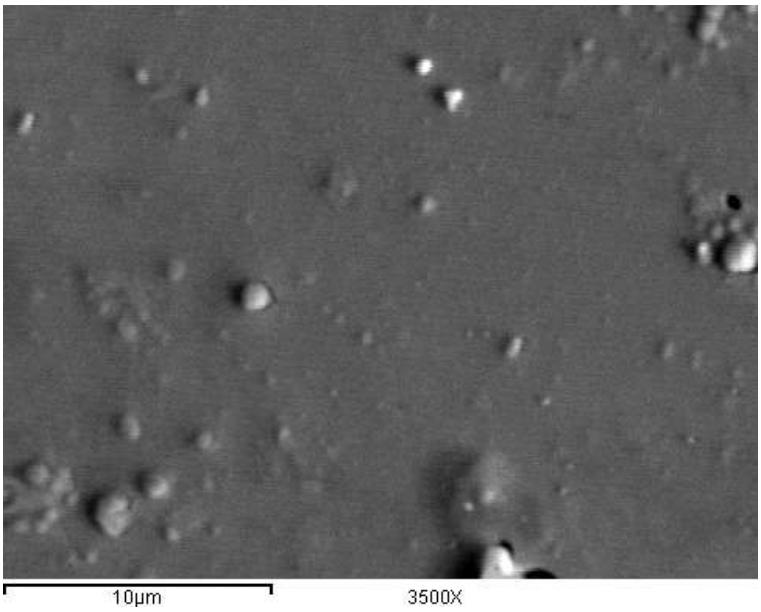

Fig. (2): The surface topography of the deposited ZnSe layer

Figure (3) shows the energy dispersive X-ray analysis (EDAX) spectrum of ZnSe layer and its elemental composition. The obtained atomic ratio of Zn:Se is 57.31:42.69 i.e. 1.34:1.0, this ratio agrees with that reported by EL Zawawi et al. [7] for ZnSe nanocrystalline film prepared by inert gas condensation.

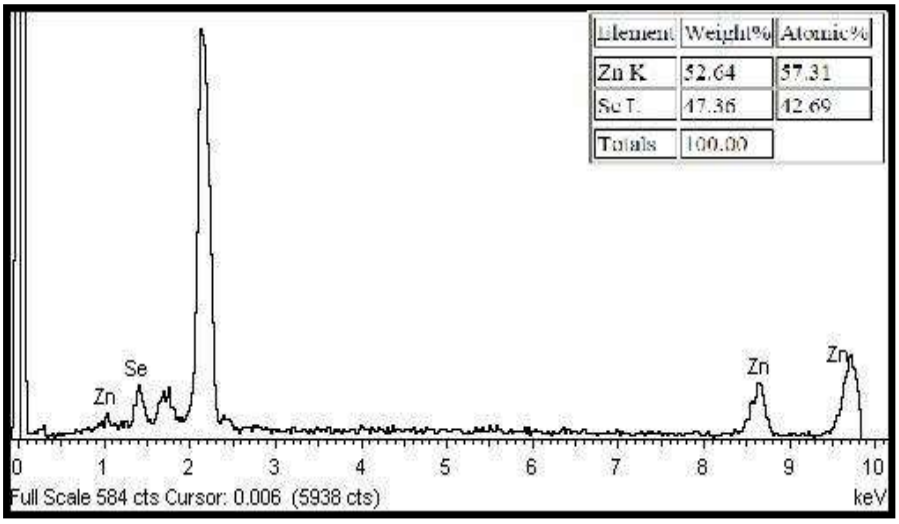

Fig. (3): The EDAX spectrum of ZnSe layer and its elemental composition.

3.2. Dark Current-voltage Properties of n-ZnSe/p-GaAs Device:

The dark current–voltage properties of the n-ZnSe/p-GaAs heterojunction in the temperature range 300-400 K are shown in Fig.(4). The strong voltage dependence of the forward current and low voltage dependence of the reverse current are characteristic properties of strong rectification performance for the junction diode interface. This behavior can be understood in terms of the width of depletion region by considering a diode behavior [8]. Moreover, at a certain applied voltage, the current increases with increasing temperature, indicating a negative temperature coefficient for the resistivity [9].

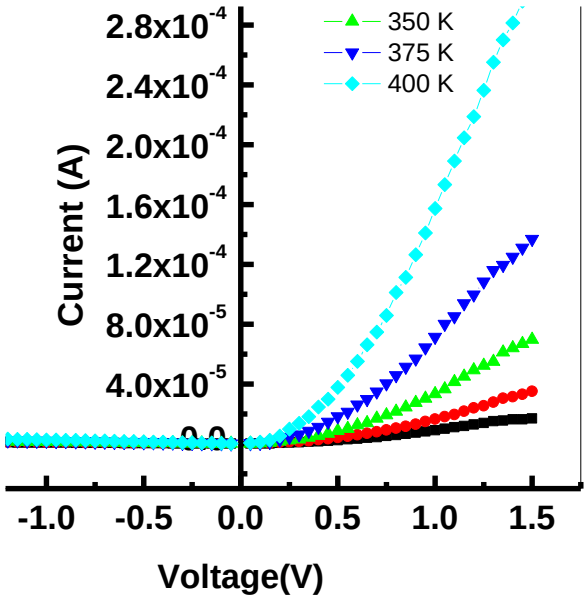

Fig. (4): I-V characteristic of n-ZnSe/p-GaAs heterojunction at different temperatures.

For non-ideal diode, the experimentally measured characteristics often present a more complex behavior than the ideal diode due to the presence of various conduction mechanisms. A summation of two (or sometimes more) exponential expressions is frequently used to model the various conduction mechanisms [10]:

$$I = I_{01}\left[\exp\frac{q(V-IR_s)}{n_1 kT}-1\right]+I_{02}\left[\exp\frac{q(V-IR_s)}{n_2 kT}-1`\right]+\frac{V-IR_s}{R_{sh}} \qquad (1)$$

where I_0 is the reverse saturation current, n is the diode quality factor, R_s is the series resistance and R_{sh} is the shunt resistance. The equation also includes the effects of parasitic series and parallel resistance, which can obscure the

intrinsic parameters of the device. The subscript 1 and 2 indicated that two possible contributions to the diode current could be present.

The series resistance, R_s, and the shunt resistance, R_{sh}, are determined from the plot of the diode junction resistance, R_J, against voltage [11], where $R_J = \partial V/\partial I$, which can be determined from the current–voltage curves. A plot of R_J against V is shown in Fig. (5) for n-ZnSe/p-GaAs heterojunction. The obtained values of the series resistance (R_s) and the shunt resistance (R_{sh}) at different temperatures are determined and listed in Table (1).

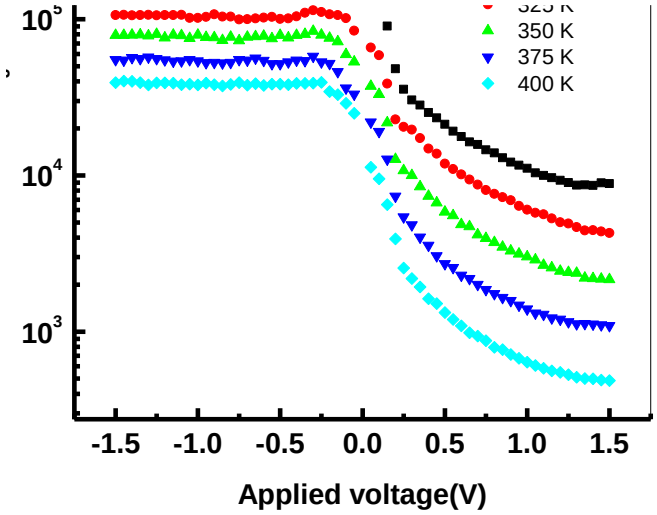

Fig. (5): Junction resistance vs.applied voltage of n-ZnSe/p-GaAs heterojunction at different temperatures .

The information about the conduction mechanism can be obtained from current–voltage characteristics at different temperatures. The semilogarithmic plots of the forward current–voltage characteristics of n-ZnSe/p-GaAs heterojunction at different temperatures ranging from 300 to 400 K are shown in Fig. (6). Two distinct regions characterize these curves indicating different conduction mechanisms. As it is observed in Fig. (6), within the narrow low forward voltage ($V \leqslant 0.30$ V), the current increases exponentially. Thus, the voltage dependence of the junction current can be expressed in the simplified form as [12]:

$$I = I_0\left(\exp\left(\frac{eV}{nkT}\right) - 1\right) \qquad (2)$$

where n is the ideality factor and I_0 is the reverse saturation current. The parameters I_0 and n can be readily determined from the curve different temperatures shown in Fig. 6 together with Eq. (2). The values of I_0 and n are calculated and listed in Table 1. The diode quality factor, n, was found to be depending on the temperature as shown in Fig. (7). This behavior is in accordance with the thermionic emission mechanism.

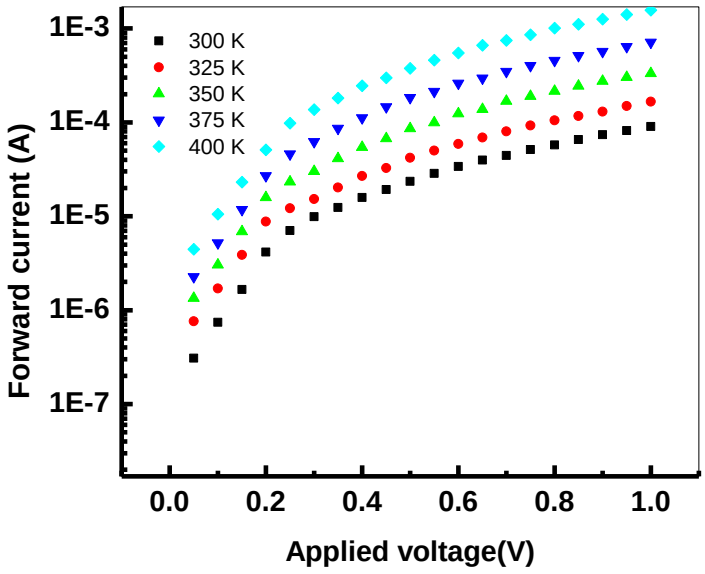

Fig. (6): Temperature dependence of the forward current.

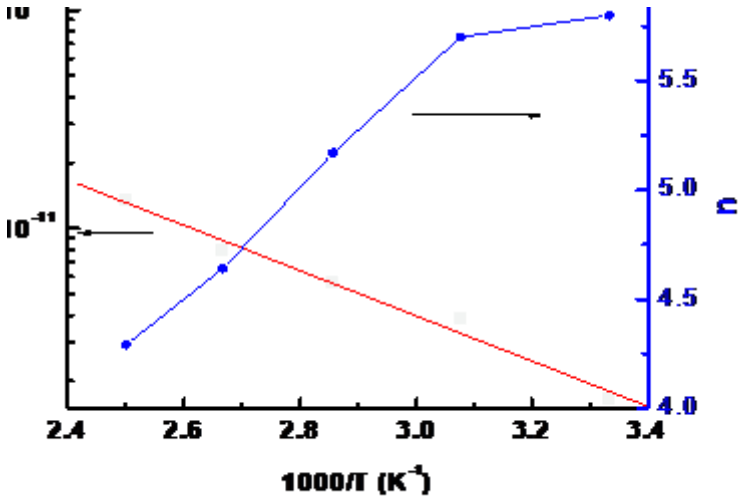

Fig. (7): Temperature dependence of I_0/T^2 and ideality factor.

For checking the presence of the thermionic mechanism as the predominant operating conduction mechanism, more analysis was carried out. According to this model, the saturation current is given by [13,14]

$$I_0 = AA^*T^2 \exp\left(\frac{-q\Phi_b}{kT}\right) \qquad (3)$$

where A is the area of the device, A^* is the effective Richardson constant and Φ_b is the barrier height. The relatively high value of *n* confirms the existence of a high density of interface states in equilibrium with the inorganic substrate [12]. According to Eq. (3), the barrier height, ϕ_b, can be obtained (see Fig. 8). The value of ϕ_b was obtained to be 0.153 eV from the slope of the straight line of $\ln(I_0/T^2) = f(1/T)$.

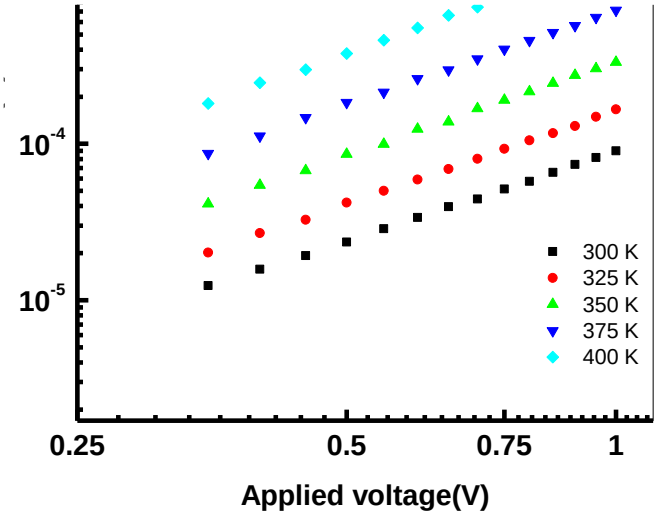

Fig. (8): Forward current versus applied voltage V in the higher voltage region.

On the other hand, the forward current as a function of applied voltage in the range $0.4 < V_f < 1.5$ V, is plotted on double logarithmic scale, and shown in Fig.(8) The current shows a power law dependence of the form $I \propto V^m$ where $m \approx 2$ indicating, that if in the n-ZnSe layer is a space charge limited current (SCLC) dominated by a single trapping level. The current density in this region is given by [15] :

$$I = \frac{9}{8} A\varepsilon_r\varepsilon_o\theta\mu\frac{V^2}{d^3} \qquad (4)$$

where $\varepsilon_r = 9.2$, and $\varepsilon_0 = 8.85 \times 10^{-12}$ F m^{-1}, are the relative permittivity of ZnSe and the permittivity of free space, respectively, μ is the hole mobility which is taken as 540 cm^2 V^{-1} s^{-2} for n-ZnSe [16], d is the film thickness and θ is the trapping factor given by:

$$\theta = (\frac{N_c}{N_t}) \exp(\frac{-E_t}{k\,T}) \qquad (5)$$

where N_c and $N_t(s)$ are the effective density of states in the valence band and the total trap concentration situated at energy level E_t above the valence band edge. The values of θ corresponding to different temperatures can be deduced from the intercept of the straight line of log I = *f*(log V) with the log I axis (Fig.8). According to Eqs. (4) and (5), a plot of log I vs. 1/T is shown at V= 1 V in Fig. (9). Assuming that $N_C = 3.1 \times 10^{18}$ cm^{-3} [17] the analysis of this curve yields $N_t(s) \approx 3.5 \times 10^{24}$ m^{-3} situated at 0.29 eV above the valence band edge.

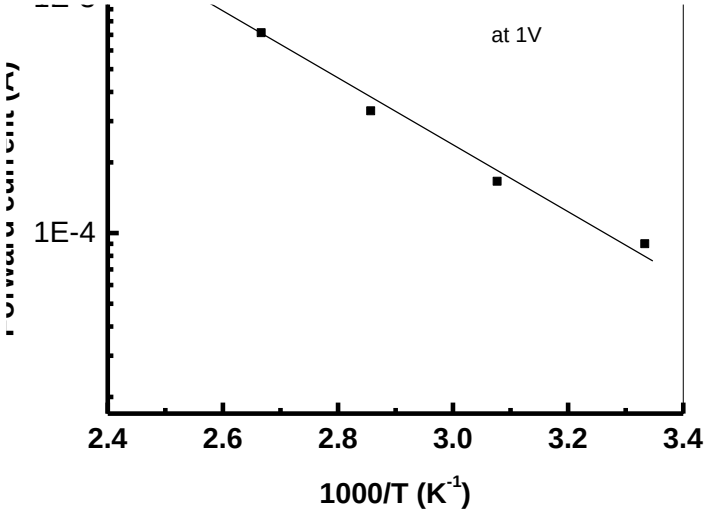

Fig. (9): Temperature dependence of the forward current in the higher voltage region.

3.3. Dark Capacitance-voltage Characteristics:

The capacitance of the n-ZnSe/p-GaAs heterojunction was measured at a high frequency of 1 MHz in dark and at room temperature. Fig. (10) shows a typical C–V characteristic obtained from as fabricated n-ZnSe/p-GaAs heterojunction. As observed from this figure, $1/C^2$–V variation is linear in the voltage range studied indicating that the junction is of abrupt nature. For abrupt junction, the junction capacitance as a function of reverse-bias potential is given by [18]:

$$C^{-2} = \frac{2(\varepsilon_1 N_1 + \varepsilon_2 N_2)(V_b - V)}{qN_1 N_2 \varepsilon_1 \varepsilon_2} \quad (6)$$

where N_1, N_2 are the donor and acceptor density in n-ZnSe, and p-GaAs respectively and ε_1, ε_2 are the permittivity of ZnSe and GaAs respectively and V_b is the built-in potential. The built-in voltage was calculated by extrapolating the $1/C^2$ curve to V=0 as 0.2 V and the slope of the straight line gives the donor concentration in ZnSe as 5×10^{15} cm^{-3}. The value V_b obtained from the C–V measurements is in agreement with the value of the potential height, Φ_b, that obtained from the I–V measurements.

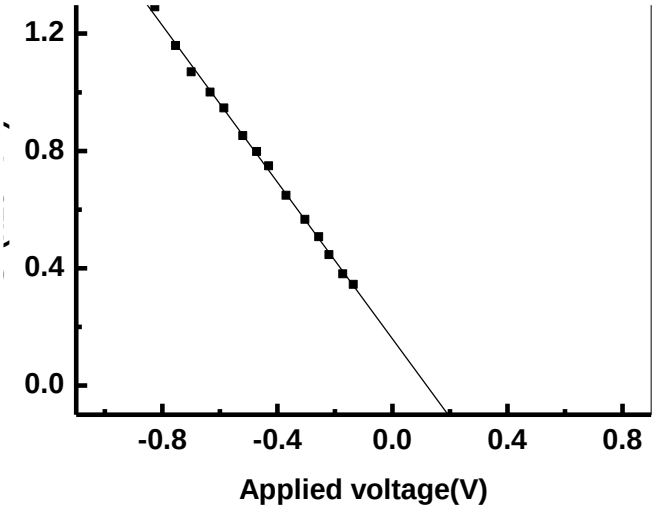

Fig. (10): The variation of $1/C^2$ versus bias voltage at room temperatures.

3.4. Photovoltaic Properties of the n-ZnSe/p-GaAs Heterojunction Device

The photovoltaic properties of n-ZnSe/p-GaAs heterojunction were determined by plotting the I–V characteristic curve under an illumination of power of 20 mW/cm^2.

The light illuminated I–V characteristics of n-ZnSe/p-GaAs heterojunction is illustrated in Fig. (11). It is evaluated that the series resistance and shunt resistance have an important effect on the I–V curve of the device under illumination. That is why the shape of the I–V curve under illumination indicates probably a very peculiar shape. This indicates that the resistance of the device decreases with illumination. The current in the reverse direction is

strongly increased by the illumination. This suggests that the carrier charges are effectively generated in the junction by illumination. This effect is due to electron–hole pair generation. When the junction studied is subjected to illumination, a current is created in the device. This indicates that the light illumination increases the production of electron–hole pairs [19, 20]. The increase in charge production is dependent on the difference in the electron affinities between n-ZnSe and p-GaAs semiconductors. The device shows photovoltaic behavior with a maximum open-circuit voltage, V_{oc} of 0.52 V, short-circuit current, I_{sc} of 10 μA, fill factor, ff of 0.33 and efficiency,η of 0.029% under 20 mW/cm2 light intensity. The main sources for the very low efficiency can be attributed to different sources: (1) the back contact to the semiconductor; (2) the contact made by the probe wire; (3) the resistance of the quasi-neutral bulk semiconductor at the back contact/semiconductor interface; (4) the depletion layer edge at the semiconductor surface and (5) the particular distribution interface states located at the metal/semiconductor interface [21–23].

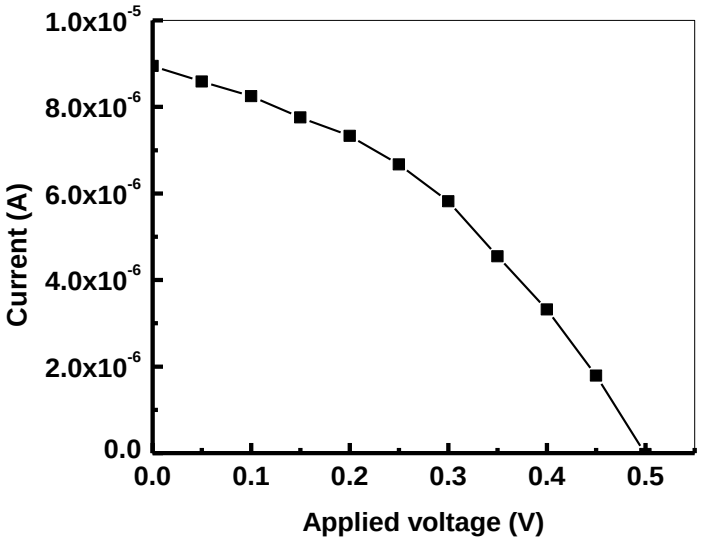

Fig. (11): Loaded I-V characteristic n-ZnSe/p-GaAs heterojunction under illumination

4. Conclusion:

The current–voltage (I-V) characteristic of n-ZnSe/p-GaAs heterojunction in dark condition showed rectification behavior. The series and shunt resistances were determined at different temperatures. The current in the device was found to obey the thermionic model in the voltage range V<0.3 volt from which the ideality n and the barrier height were determined. At higher voltages (V>0.4 volt) the operating conduction mechanism is the space charge

limited current dominated by single trap. By applying this mechanism the total trap concentration as $3.5\times 10^{16}cm^{-3}$ which are situated at 0.29 eV above the valence band edge.

The C–V characteristics of the device were performed at room temperature in dark condition. The barrier height (0.2 eV) value obtained from I-V characteristics is in good agreement with the built –in potential obtained from
C–V measurement.

The device under illumination with light intensity of $20mW/cm^2$ gave a maximum open-circuit voltage, V_{oc} of 0.52 V, short-circuit current, I_{sc} of 10 μA, fill factor, ff of 0.33 and efficiency,η of 0.029%.

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