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A Survey on Analog-to-Digital Converters' Architectures and Performance Analysis

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ABSTRACT

Analog to digital converter (ADC) represents the link between the real world represented by real time analog signals and the digitized world represented by digital integrated circuits. The performance of the ADC depends on some important parameters such as resolution, sampling frequency, Signal-to-Noise Ratio (SNR), Power consumption and Figure-Of-Merit (FOM). This paper introduces a brief discussion of the most common ADC architectures. More detailed discussion on time-based ADCs is introduced and recent architectures introduced by researchers are presented and compared with each other in terms of linearity error, resolution, and power consumption. Moreover, a comparison survey is presented on the most popular commercial ADCs. The data used in the survey are taken for about 1500 commercial ADCs from major integrated circuits companies such as Texas Instruments and Analog Devices. The aim of this paper is to give a detailed comparison on the most common ADCs to help researches to choose the best architecture that fits their desired application and to draw researchers' attention towards time-based ADCs as they proved a promising performance improvements compared with other ADCs architectures in many applications such as software radio receivers.

Keywords: Analog-to-digital converters, time-based analog-to-digital converters, survey, resolution, Signal-to-Noise Ratio.

1. INTRODUCTION

Analog to digital converter (ADC) is considered the link between the real world represented by real time analog signals (speech, radar, medical imaging… etc.) and the digitized world represented by digital integrated circuits, microprocessors and computer software. ADCs are the key components in most recent electronic devices especially in Software Defined Radio (SDR), biomedical devices and low power electronic devices.

The performance of ADC defines the whole performance of the system in terms of the power consumption, operation speed and resolution.

One of the most important problems that face researchers in the design of ADC is technology scaling. Technology scaling results in reducing the supply voltage which results in reducing the dynamic range of the input voltage. Also, the Signal to Noise Ratio (SNR) decreases as the noise level became significant with respect to the small input voltage (thermal noise does not scale with technology).

2. ADC DESIGN TRENDS

Seeking power efficiency improvement along with technology scaling, the following three design trends are introduced [1, 2]:

2.1. Minimalistic design

The main goal in this approach is to simplify the analog sub-circuits in the ADC to improve the overall power dissipation although this will affect the accuracy in measuring the input voltage. An example of this trend is to remove or simplify the op-amp blocks in ADC as in op-amp-less implementation of pipeline ADCs [3] in which the op-amp is replaced with open-loop amplifiers. Another example is to replace op-amps with comparators in switched capacitor circuits as shown in Figure 1 and Figure 2 [4].

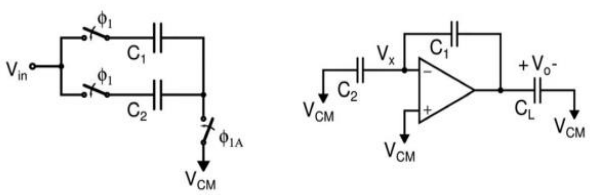

Figure 1: Conventional switched capacitor gain stage [4].

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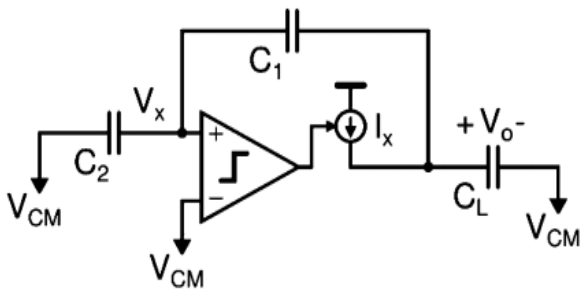

Figure 2: Comparator-based switched capacitor gain stage [4].

2.2. Digitally assisted analog design

In this trend, the main idea is to relax the precision of the analog circuitry (which reduces power consumption significantly), while correcting the input analog imperfections in the digital domain, resulting in lower power consumption and faster designs.

One example of this approach is the use of open-loop amplifiers in pipeline ADCs while correcting the nonlinearities resulted from these amplifiers in the digital domain [3]. Figure 3 shows the conventional pipeline stage while Figure 4 shows the usage of open-loop amplifier in the pipeline stage [3]. Figure 5 shows the digital non-linearity compensation circuit that makes the back-end conversion error (ε_r) very small [3].

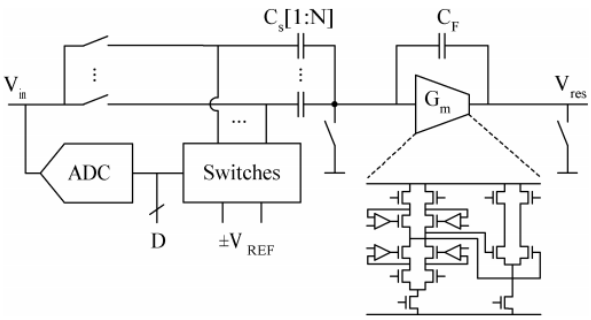

Figure 3: Conventional pipeline stage [3].

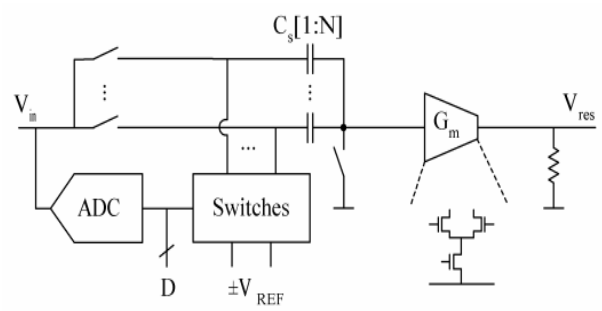

Figure 4: Pipeline stage with open-loop amplifier [3].

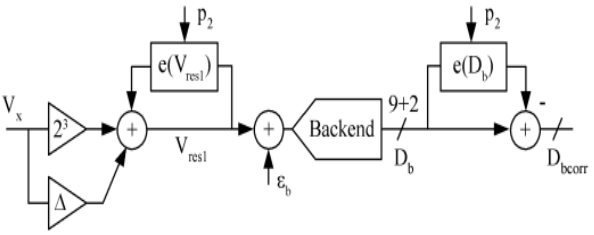

Figure 5: Digital non-linearity compensation [3].

2.3. Time domain analog signal processing

The idea behind this approach is that the analog signal can be processed in the time domain instead of the voltage domain. This makes it possible to process the analog signal by the digital circuitry instead of the analog one while taking advantage of technology scaling to significantly reduce power consumption and area at the same time.

This approach led to the design of Time-based Analog to Digital Converters (T-ADC) where the input voltage signal is converted to a delay signal before processing and converting it to a digital code. This type of ADCs is discussed later in details.

Another design has been introduced which is based on converting the voltage to frequency instead of time using the voltage-to-frequency converter [5] or by using a voltage-controlled oscillator (VCO)-based ADC, where the input signal changes the VCO frequency and the frequency is digitized with phase detectors [6].

3. PERFORMANCE METRICS

The overall dynamic performance of ADCs can be identified by five important metrics as follows:

3.1 Signal to Noise Ratio (SNR)

It is defined by the ratio between the signal power to noise power as shown below [7]:

$$\text{SNR} = 10\ \log_{10}\left[\frac{\text{Signal Power}}{\text{Noise Power}}\right] \quad (1)$$

3.2 Total Harmonic Distortion (THD)

It is defined as the ratio between the signal power to harmonic distortion power as shown below [7]:

$$\text{THD} = 10\ \log_{10}\left[\frac{\text{Signal Power}}{\text{Distortion Power}}\right] \quad (2)$$

3.3 Signal to Noise and Distortion Ratio (SNDR)

It is defined by the ratio between the signal power to the sum of distortion and noise power as shown below [7]:

$$\text{SNDR} = 10\ \log_{10}\left[\frac{\text{Signal Power}}{\text{Distortion Power+Noise Power}}\right] \quad (3)$$

3.4 Effective Number Of Bits (ENOB)

It represents the actual resolution of the ADC when taking in consideration the circuit noise as follows [7]:

$$\text{ENOB} = \frac{\text{SNDR(dB)} - 1.76}{6.02} \quad (4)$$

3.5 Figure of Merit (FOM)

It represents the efficiency of the ADC regardless of its design. This parameter can be used to compare the performance of ADCs with different architectures and applications. There are many equations that describe FOM. The most commonly used equation is Walden FOM [8] that describes the ADC performance in terms of power consumption, sampling frequency and ENOB as follows:

$$FOM = \frac{P}{2^{\text{ENOB}} F_S} \quad (5)$$

Where P is the power consumption and F_S is the sampling frequency.

4. ADC DESIGN SPECIFICATIONS

There are important parameters that should be taken in consideration during selecting the appropriate design of ADC for a specific application. These parameters are:

4.1. Resolution

It is the minimum required change in the input signal to increase the output digital code by 1 Least Significant Bit (LSB) and can be described as follows [7]:

$$\text{LSB} = \frac{V_{in\_FR}}{2^N} \quad (6)$$

Where V_{in_FR} is the full range of the input signal and N is the number of bits of the ADC.

4.2. Dynamic range

It represents the maximum range of the input signal that can correctly detected by the ADC. It represents an important metric during the appropriate ADC architecture for a specific application [7].

4.3. Latency (Output Delay)

It represents the time required by the ADC to convert the analog signal to the digital code [7]. As the latency decreases, the ADC becomes more efficient. Some applications require high speed ADCs such as pipeline ADCs at the cost of power consumption while other applications requires lower power consumption at the cost of operation speed [7]. These applications are discussed later in details.

4.4. Power Consumption

Although reducing the power consumed is a main goal in all ADC architectures especially in mobile devices, this power reduction comes at the cost of higher output speed in specific applications. In sum, there is a trade-off between the power consumption and the operation speed. Both parameters are decided based on the type of application.

5. ADC ARCHITECTURES

In this section, different ADC architectures will be discussed in detail. Some architectures convert the input voltage signal directly to digital code such as flash ADC, Successive Approximation Register (SAR) ADC, pipe-lined ADC and sigma-delta ADC.

Other types of ADCs convert the input voltage signal to intermediate signal (time or frequency signals) first before converting it to digital code such as single slope ADC, dual slope ADC, Pulse Width Modulation (PWM) ADC and a Voltage-to-Time Converter (VTC) circuit followed by a Time-to-Digital Converter (TDC) circuit. The VTC followed by TDC will be discussed later in details in a single section as it represents the main interest of this paper.

5.1. Flash ADC

An N-bit flash ADC is shown in Figure 6. It consists of 2^N resistors that form a ladder voltage divider in order to divide the reference voltage into 2^N equal intervals. This reference voltage represents the maximum value for the input voltage signal. The 2^N comparators compare the input voltage with each value of the voltage intervals resulting in logic '1' if the input voltage value is greater than the reference voltage of the corresponding bit. The output of these comparators is a thermometer code that needs a decoder to convert it to a digital code [7, 9].

The advantage of this design is its high speed as it is only limited by the delay of comparators and the decoder [7, 9]. However, this architecture has low resolution [7, 9]. For higher resolution, the speed of the flash ADC is affected by the loading of the large number of comparators. Moreover, the area and the power consumption increase due to using many comparators.

5.2. Successive Approximation Register (SAR) ADC

SAR-ADC is one of the most used architectures because it gives better resolution with no more silicon area or more consumed power. This high resolution comes at the cost of the operation speed.

An N-bit SAR-ADC is shown in Figure 7. It consists of a comparator, N-bit DAC and SAR. Its theory of

operation depends on iteration process for the output bits starting from the Most Significant Bit (MSB) to the LSB.

First, the MSB is initialized by logic '1'. Then, the input voltage after being sampled is compared with the DAC output ($V_{REF}/2$) using the comparator. If the input voltage is greater than the DAC output the output of the comparator will be "1", the MSB remains "1" and the next bit will be executed by comparing the sampled input with the new DAC output ($V_{REF}/2 + V_{REF}/4$) at the next edge of the clock signal. Else, the output of the comparator will be '0' and the MSB will be set to '0'.

Then, the sampled input is compared with the DAC output in this case at the next edge of the clock signal to determine the value of the next bit. This iteration process will be repeated until the LSB is executed and the End Of Conversion (EOC) signal becomes '1'. The operation procedure of this ADC is explained in the flowchart shown in Figure 8.

For further illustration, take the input voltage range equals to 1volt ($V_{ref} = 1$), $V_{in} = 0.6V$ and the SAR-ADC is a 4-bit ADC. The solution procedure is as follows:

Since $V_{in} > V_{ADC}$ ($V_{ref}/2$); (0.6 > 0.5), then the MSB (bit 3) is '1'. Since $V_{in} < V_{ADC} + V_{ref}/4$; (0.6 < 0.5+0.25), then the next bit (bit 2) is '0'. Since $V_{in} < V_{ADC} + V_{ref}/8$; (0.6 < 0.5+0.125), then the next bit (bit 1) is '0'. Since $V_{in} > V_{ADC} + V_{ref}/16$; (0.6 > 0.5+0.0625), then the next bit (bit 1) is '1'.

Hence, the final digital output that represents the input voltage of 0.6volts is '1001' which equivalent to 0.5+0.0625 = 0.5625V. This error difference decreases by increasing the number of bits (increasing resolution). Table 1 shows the voltage that corresponds to each bit.

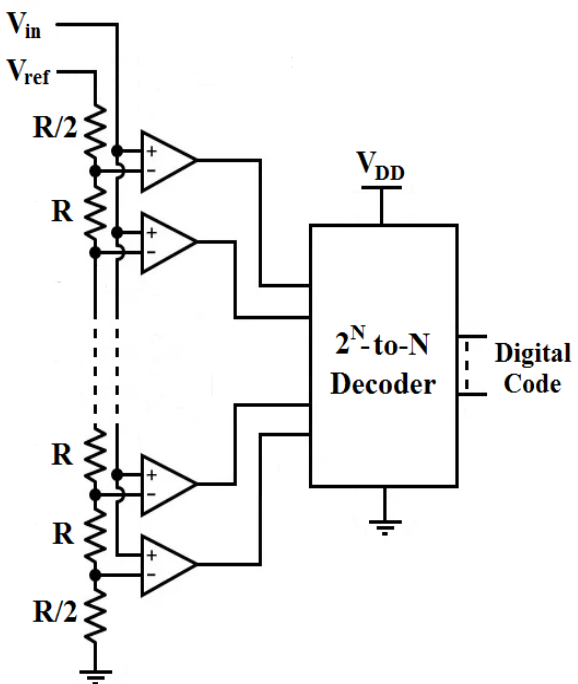

Figure 6: N-bit Flash ADC.

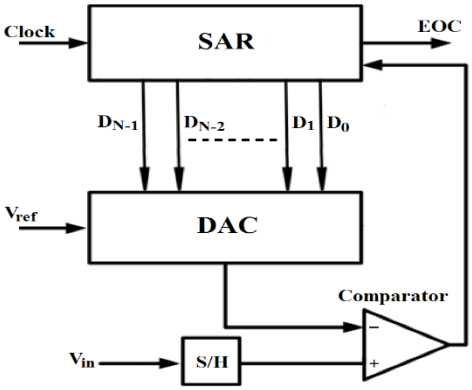

Figure 7: N-bit SAR-ADC.

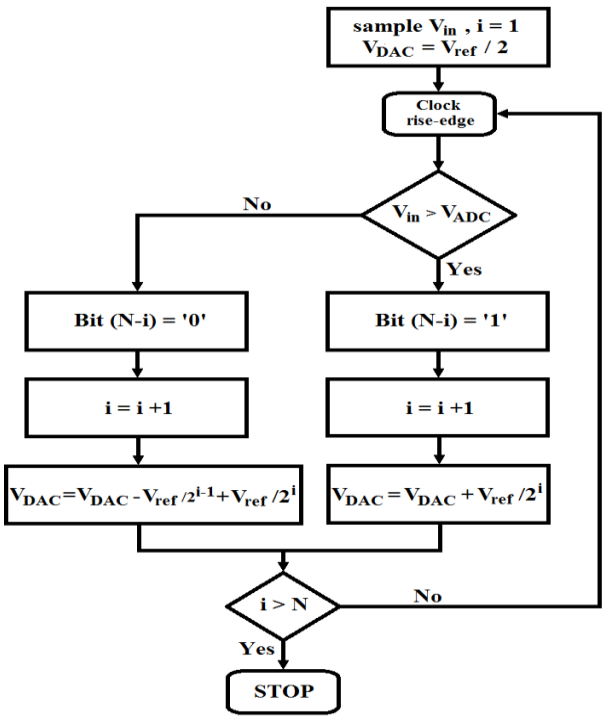

Figure 8: Operation flow chart for N-bit SAR-ADC.

Table 1: Performance Comparison.

Bit	Voltage
3	0.5
2	0.25
1	0.125
0	0.0625

5.3. Pipeline ADC

Its theory of operation based on obtaining higher resolution by cascading many lower resolution ADCs together. This helps in reducing the complexity of the circuit and reducing the chip area used. As an example, when using 8-bit flash ADC, 255 comparators are needed.

By using Pipeline ADC of 4 stages each stage is a 2-bit flash ADC; we can obtain the same resolution with only 12 comparators instead of 255 ones [7].

However, this simple architecture will be at the cost of latency. In another words, the delay time of pipeline ADC equals the sum of the delay time of each stage.

Figure 9 shows a single stage of an (N×M)-bit pipeline ADC. First, the input signal is sampled then converted to a digital code using an N-bit ADC, then the N-bits digital code is reconverted into an analog signal using an N-bit DAC. This analog signal is then subtracted from the sampled input signal to produce the residue signal. This residue signal is amplified by a gain of 2^N to convert it back to a full-scale signal to make it available for the next stage ADC. The shown stage is one of M- stages that form the (N×M) overall resolution.

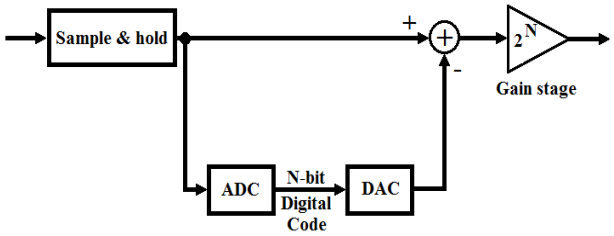

Figure 9: An N-bit single stage of (N×M) bit pipeline ADC.

5.4. Sigma Delta (SD) ADC

Its idea is based on oversampling for the input signal and reducing the error by the feedback system. Figure 10 shows a first order Sigma-Delta ADC. It consists of a summing node, integrator, ADC and a DAC feedback branch [10, 11].

First, the input voltage is summed with the output of the DAC feedback branch. This summing can be represented by a switched capacitor [10, 11].

Second, an integrator is used to add the present output value of the summing node with the previous value obtained at the previous integration step. After that, a comparator converts the integrator output to a logic bit. The output of the comparator is "1" if the integrator output voltage is greater than or equal zero and vice versa. If the input signal is increasing, the comparator generates a greater number of "1" and vice versa if the input is decreasing [10, 11].

Finally, the 1-bit DAC at the feedback branch produces "$+V_{ref}$" value if the output of the comparator is "1" and "$-V_{ref}$" value otherwise. The loop is executed many times which results in high resolution but at the cost of latency. Further details about SD ADCs and their different architectures can be found in [12, 13].

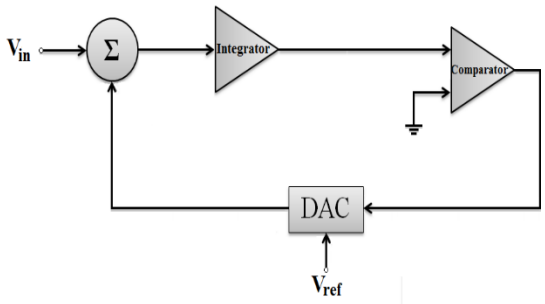

Figure 10: First order Sigma Delta (SD) ADC.

6. PERFORMANCE ANALYSIS

A study is conducted on about 1500 commercial ADCs to compare the performance of different architectures of ADCs in terms of sampling frequency, resolution, SNR, power consumption and FOM. These commercial ADCs are from the most popular integrated circuits' companies such as Texas Instruments and Analog Devices.

Figure 11 shows the resolution of ADCs versus the sampling frequency. It is obvious that sigma delta ADCs offer higher resolution than the other architectures while flash ADCs have the lowest resolution. Moreover, pipeline ADCs can be used for applications that need high sampling rates.

Figure 12 shows SNR of ADCs versus the sampling frequency. It is obvious that sigma delta ADCs have the highest SNR value. Figure 13 shows the power consumption of ADCs versus the sampling frequency. It can be concluded that pipeline ADCs consume higher power compared with other ADCs. Figure 14 shows FOM for ADCs. It indicates that SAR ADCs have the worst performance while pipeline ADCs have the best performance.

Table 2 shows performance comparison for the commercial ADC architectures in terms of sampling rate, resolution, SNR, power consumption and FOM. It is concluded from the previous analysis that sigma delta ADCs have a promising performance in terms of resolution, SNR and power consumption. However, they suffer from low sampling frequencies. In the other hand, pipeline ADCs have high sampling rate but consume high power and have low SNR values.

Each of the previous four architectures has the best performance that fits specific application. In other words, sigma delta ADCs can be used for low power applications that require high precision at high latency while SAR ADCs can be used for low power, high speed applications. Moreover, pipeline ADCs are the most popular ADCs for applications that need high sampling rates but at the cost of power consumption and latency.

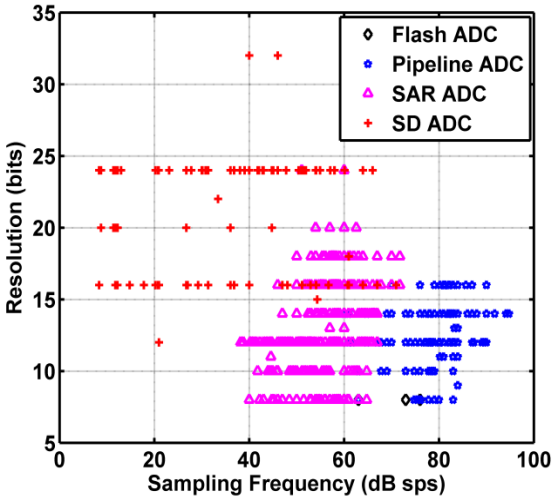

Figure 11: Resolution versus sampling frequency.

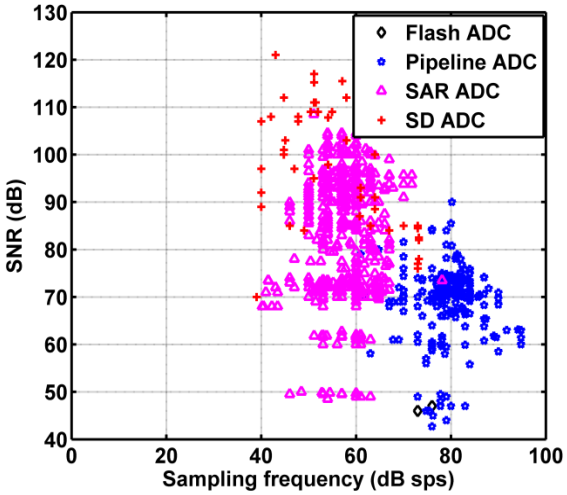

Figure 12: SNR versus sampling frequency.

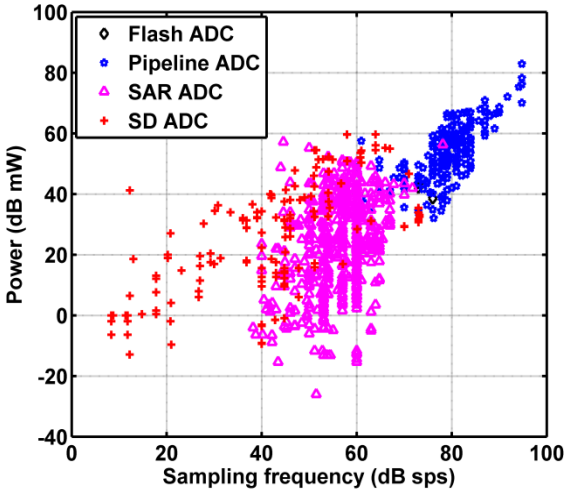

Figure 13: Power versus sampling frequency.

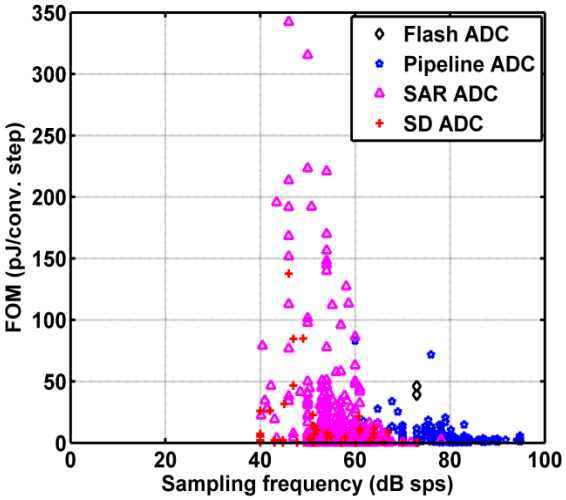

Figure 14: FOM versus sampling frequency.

Table 2: Performance Comparison for the recent commercial ADC architectures.

Architecture	Sampling rate	Resolution	SNR	Power consumption	FOM
Flash	Moderate high	Low	Low	High	Moderate
SAR	Low	Moderate	Moderate high	Low	High
SD	Low moderate	High	High	Moderate	Moderate
Pipeline	High	Moderate	Low moderate	High	Moderate

7. TIME-BASED ADCS

The design of Time-based Analog-to-Digital Converter (T-ADC) gains researchers' interests as a solution to the previously mentioned limitations that resulted from technology scaling.

In this type of ADCs, the input voltage signal is converted to a delay signal first where the delay is proportional to the input signal value. Then, this delay signal is converted to a digital code. In other words, the processing of the signal will be in the time domain which is a big advantage because time resolution has been improved in nanometer-scale devices due to the reduction of gate delay, despite the reduction in supply voltage.

Moreover, digital circuits can be used to perform analog processing instead of using analog circuits to take the advantage of technology scaling in reducing the area and power consumed significantly. As an example, some T-ADC designs don't need a sample and hold circuit for the input voltage signal such as Voltage to Time Converter (VTC) based T-ADC which results in improving the overall power consumed by a great amount. This type of time-based ADCs is discussed below in details.

VTC based T-ADC consists of two stages as shown in Figure 15. The first stage is a Voltage to Time (VTC) converter that converts the input signal to delay pulses. The delay in each pulse is proportional to the input voltage

signal value. The second stage is a Time-to-Digital Converter (TDC) that converts these delay pulses to a digital code. The VTC theory of operation is discussed below and the recent research that is done to improve its performance specifically increasing the output linearity.

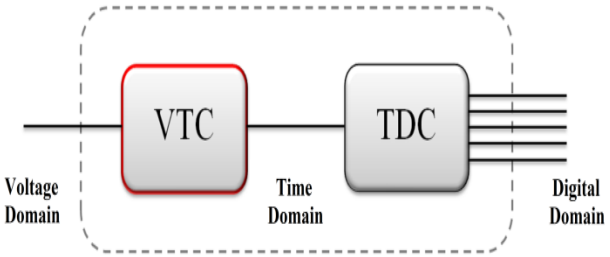

Figure 15: VTC based T-ADC.

7.1. Voltage-to-Time Converter (VTC)

There are numerous circuits that convert the voltage signal to delay-time signals. One of these circuits is the Ramp-and-Comparator-Based VTC explained in [7]. But, the most common circuit used is the current starving inverter circuit shown in Figure 16. It consists of a CMOS inverter with an NMOS starving transistor connected to the driver branch which is controlled by the analog input signal (Vin) [14].

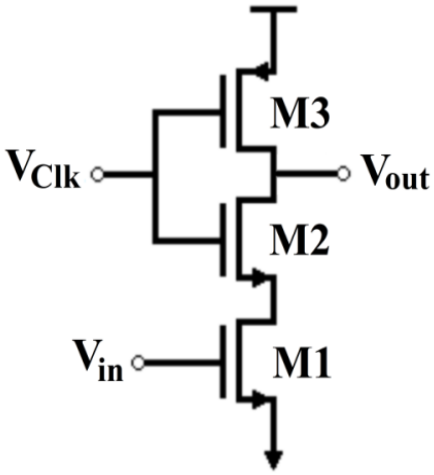

Figure 16: Current starving inverter VTC.

The input signal which is connected to the gate of the starving NMOS transistor controls the current of the driver branch during fall time. In other words, the fall time of the output voltage of the inverter is proportional to the input voltage signal. When the value of the input signal increases, the fall time of the output signal increases and vice versa. Figure 17 shows the fall time of the inverter for different input voltages. The rise time of the inverter output can be also controlled instead of the fall time by connecting a PMOS transistor with the load branch of the inverter as shown in Figure 18 [15].

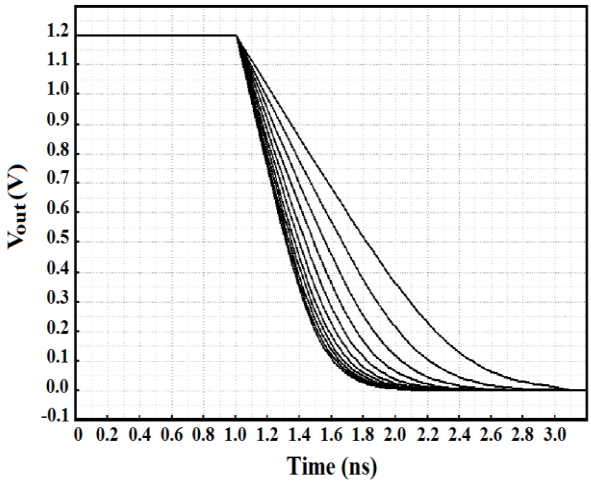

Figure 17: Fall-time of the output voltage of the conventional VTC for input voltage range from 0.7V to 1.2V at supply voltage of 1.2V.

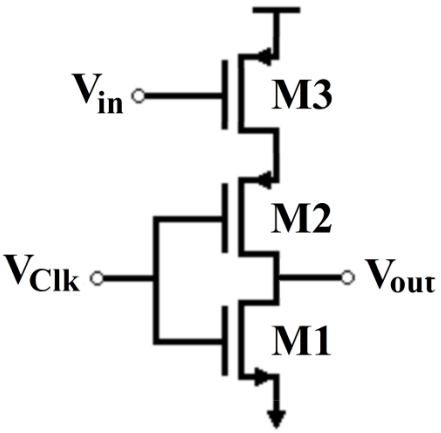

Figure 18: Rise-time current starving inverter VTC.

7.2. VTC performance limitations

The current starved inverter VTC suffers from severe limitations that affect the conversion process of the input signal. These limitations are listed as follows:

7.2.1. Limited dynamic range

The input signal cannot have small values because it is connected to the gate of the starving NMOS transistor. Thus, its value must be greater than the threshold voltage of the transistor for the transistor to be 'ON' to create a path for the output to ground.

To overcome this problem, a weak transistor (with small aspect ratio) is connected in parallel with the starving transistor at which its gate is connected to the supply voltage [15, 16]. This weak transistor is always 'ON' to guarantee that there is a path for the output to ground even for small values of the input voltage. Figure 19 shows the addition of a weak transistor M4 for the VTC to operate at small input values.

Moreover, the upper limit of the dynamic range is limited as it affects the linearity of the circuit response. In other words, the fall time of the output signal becomes more non-linear with respect to the input signal when the value of the input voltage increases. This point will be discussed below in details and how to overcome it.

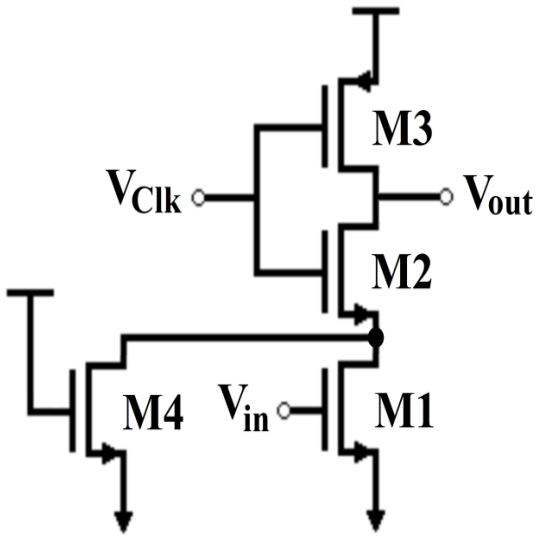

Figure 19: VTC with weak transistor M4.

7.2.2. Non-linearity effects

One of the biggest challenges in the design of VTC circuit is the non-linearity that appears in the fall time delay of the output response for high input values [16]. It is obvious from Figure 17 that when the input voltage increases, the delay curves for the output becomes more non-linear which results in inaccurate conversion of the input signal to digital code.

This non-linearity happens because during the fall time of the output signal, the starving transistor will be operating in saturation mode with a current of:

$$I_D = \frac{K'}{2} \times \frac{W}{L} (V_{GS} - V_{th})^2 \qquad (7)$$

Where $V_{GS} = V_{in}$, W/L is the aspect ratio of the transistor, k' is a constant and V_{th} is the threshold voltage of the starving transistor.

Also,

$$I_D = C \frac{dV}{dt} \quad ==> \quad dt = C \frac{dV}{I_D} \qquad (8)$$

Where C is the parasitic capacitance at the output node, dV is the voltage change at the output during discharging from '1' to '0' and dt is the delay fall time of the output.

From the two previous equations we can conclude that the relation between the input voltage and the output delay time is non-linear and this non-linearity increases by increasing the input voltage.

7.3. Time-to-Digital Converter (TDC)

Time-to-Digital Converter (TDC) converts the delay signal that produced by the VTC into a digital code for a complete analog to digital conversion process. The performance of the TDC should be investigated as it limits the performance of the whole ADC in terms of linearity, resolution and power consumption.

The most important parameters that represent the Linearity in the whole ADC are Differential Non-linearity (DNL) and Integral Non-Linearity (INL). DNL is defined by the conversion step deviation from its ideal value (1 LSB) in ADCs. INL is defined by the deviation of the whole transfer function of the ADC from its ideal value [17]. The maximum value of DNL should not exceed 1 LSB to avoid missing codes [17].

There are many TDC architectures that have been proposed to improve the resolution without affecting the linearity of the ADC. The most common types of TDCs are discussed below in details. The advantages and disadvantages of each type are also discussed.

7.3.1. Delay Line Based TDC (Flash TDC)

Flash TDC architecture is shown in Figure 20. It consists of cascaded buffer stages with a delay unit before each stage [7]. The buffer consists of a D-flip flop with two inputs; the start and the stop signals. The start signal represents the input delay signal that comes from the VTC. The difference between the start and the stop signal represents the time range of the input delay signal. Each delay unit has more delay than the previous one by td which represents the resolution of the TDC or LSB (the minimum delay time that can be detected by the TDC).

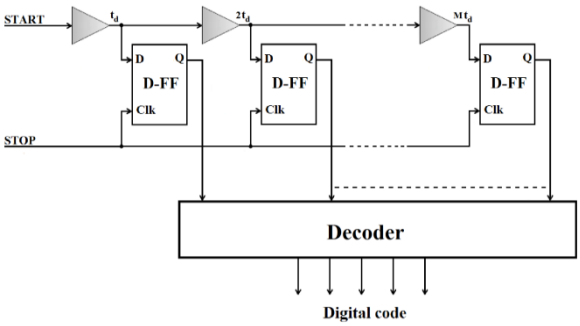

Figure 20: Flash TDC.

The start signal which represents the input delay signal passes through the buffer stages. It activates the number of flip-flops that resembles its delay value. Then the stop signal arrives and the activated flip-flops record logic '1' as their current states. The output of the flip-flops is a thermometer code which is converted to a digital code using a decoder.

The most important drawback of this architecture is the trade-off between the speed and resolution [7]. For higher resolution, the number of buffer stages is increased (as t_d decreases) which reduces the speed of operation for the TDC.

7.3.2. Vernier Delay-Line Based TDC

This architecture has solved the problem of having a small resolution less than the minimum gate delay in the technology used. Its architecture is shown in Figure 21. Both the start and stop signals have delay units in their path but with different values making the stop signal path faster than the other. The difference between the delay units of the two paths equals to the resolution of the TDC (LSB).

The stop signal comes after the start signal with a delay time chosen to be equal to the maximum delay of the input signal ((M+1) x LSB).

As the start signal starts to pass through the buffer stages, the output of the D flip-flop is set as "High" if the start signal comes before the stop signal. Once the stop signal reaches the start signal, the output of the flip-flops which is a thermometer code is converted to a digital code using a decoder.

Vernier delay-line TDC has the advantage of its high resolution that can be less than the minimum gate delay in the technology used. However, this architecture suffers from significant drawbacks such as transistors' mismatch, noise, and delay line physical length [18]. Much research is done [19-24] to achieve higher resolution that can reach 2ps [24].

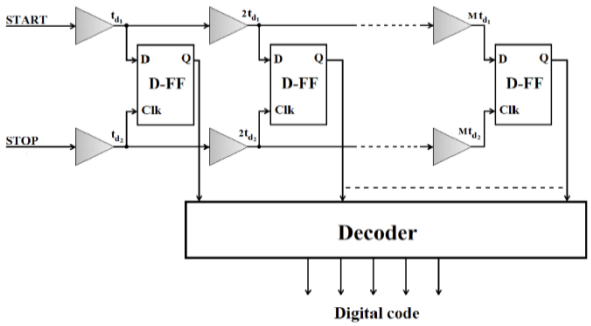

Figure 21: Vernier delay-line TDC.

7.3.3. Hybrid TDC

In the Vernier Delay-line based TDC, we can only measure short time range with high resolution. With the hybrid TDC, we can measure large time range with high resolution. This can be achieved by using a counter with the delay line to increase the time range used. The delay line TDC is employed as a fine quantizer to resolve the residual error of the counter measurement. More details about the structure and architecture of Hybrid TDCs are available in [25].

8. NOVEL TRENDS AND FUTURE WORK

Research now is focusing on improving the performance of the VTC circuit rather than the TDC circuit as the non-linearity of the VTC is much large and affects the linearity of the following TDC stage. Hence, this paper focuses on the novel trends in the design of VTC circuits.

A lot of research is done to improve the performance of the VTC circuit. Circuits in [16] and [26-35] are proposed to overcome the previously mentioned limitations of the conventional VTC circuit. In [16], a linearization circuit is proposed to achieve a maximum linearity error of 2%. However, it has a limited input dynamic range of only 200mV.

A VTC circuit is proposed in [26] which operate at a high sampling rate of 5GS/s but consumes high power of 3.6mW and has only 100mV input dynamic range. The VTC proposed in [27] is a modification to the VTC circuit in [26] in order to increase the input dynamic range to 140mV which is still insufficient.

In [28], the theory of operation of the proposed VTC circuit is modified at which the input signal is compared with a voltage ramp signal. This design has the advantage of low power consumption but operates at a small sampling frequency of 1MHz. In [29], a differential input is applied to the proposed VTC circuit to achieve a maximum linearity error of 3%. However, the input dynamic range is still very small (172 mV).

In [30], a Voltage-to-Frequency Converter (VFC) is proposed and a 3% maximum linearity error is achieved. However, this design suffers from small input dynamic range of 320mV and consumes high power of 477µW. In [31], the linearity of the VTC is improved by adding track-and-hold circuit, level shifter and a pulse shape restorer. However, the improved linearity is not sufficient and the proposed VTC consumes high power. In [32], a VTC with a two-step transition inverter delay line is proposed which consumes 180µW of power. However, the proposed VTC has very low sensitivity of 0.1ps/mV.

In [33], a current-to-time converter (CDC) is proposed which achieves a maximum linearity error of 2.1%. However, the sampling rate is very small (50MS/s). In [34], although the proposed VTC achieves a better dynamic range of 400mV, the power consumption of this design is relatively high (3.35mW). In [35], a fully digital time-based ADC is proposed to reduce the chip area at which the power consumption is reduced to 380µW.

Future work is expected to focus on the design of alternative circuits for the VTC in order to increase the output delay linearity with respect to the input signal. A promising solution is to connect the input signal to the body terminal of the starving transistor forming a forward-body biasing circuitry. This solution has shown a great improvement in reducing the non-linearity error to about 0.5% which represents, up to the authors' knowledge, the minimum error in all recent research. The authors are working on an analytical proof to confirm the results obtained from simulations.

9. CONCLUSIONS

This survey is presented to analyse and compare the performance of the most common commercial ADC

topologies in terms of sampling frequency, resolution, SNR, power consumption and FOM. It is concluded that pipeline ADCs can be used for applications that require high sampling rate but at the cost of having lower resolution and higher power consumption. SAR ADCs have high SNR, low power and good overall performance. Sigma-Delta ADCs are preferred for applications that need high resolution at moderate power consumption. This paper focuses more on time-based analog-to-digital converters. The theory of operation for time-based ADCs is discussed in details with a detailed study on the recent research done to improve the performance of this type of ADCs. This paper helps researchers to choose the proper ADC architecture that fits their specific application and encourage for more research to be done on time-based ADCs especially on finding novel solutions to improve the performance of the VTC circuit.

Credit Authorship Contribution Statement:

Ahmed L. Elgreatly: Methodology, Investigation, Software, Original draft, Review and Editing; **Ahmed A. Shaaban**: Conceptualization, Methodology, Formal analysis, Supervision; **Rania M. Abdalla**: Validation, Formal analysis, Review and Editing, Supervision; **El-Sayed M. El-Rabaie**: Validation, Supervision, Review and Editing.

Declaration of competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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