Design and Simulation of 140 dB Dynamic Range and 20 uV_{rms} Readout Noise CMOS Image Sensor

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***Abstract*— This paper provides the design, simulation and implementation of a very wide dynamic range and a low readout noise CMOS image sensor (CIS) with high sensitivity by using a diode connected transistors in parallel with floating diffusion node and sensor output. The sensor is simulated, designed and implemented in a 130 nm CMOS technology using cadence tool. The area of the proposed pixel reaches to 3 um x 3 um and consists of seven NMOS transistors and one capacitor. The readout circuit has the following parameters as very low output noise of 20 uV_{rms} with a 5 MHz bandwidth for pixel circuitry. Power dissipation of 10 uW was achieved at an operation voltage of 1.6 V for pixel circuitry. The proposed sensor has good features of low noise and a 140 dB wide dynamic range due to the diode connected transistor configuration that has been used. This paper provides the effect of adding a diode connected transistors M7 and M8 on an increasing dynamic range of CMOS image sensor to 140 dB and reducing its readout noise to 20 uV_{rms}. Also, this paper provides a mathematical simulation of noise model of CIS using Matlab and cadence.**

Keywords*— CMOS image sensor (CIS), wide dynamic range (WDR), bandwidth, readout noise, diode connected transistor

I. INTRODUCTION

The active pixel sensors (APS) are implemented in a commonly used CMOS technology, these sensors which fabricated using CMOS technology are very useful in many scientific, commercial and consumer applications [1]. Recently, CMOS image sensors allow integration of all functions required for timing, exposure process, color processing, compression of the image and analog to digital converters (ADCs) on the same die. In addition, CMOS image sensors provide additional advantages over CCD in terms of small consumption of power, small operating voltage, smaller noise and high sensitivity.

Low noise CMOS Image Sensor (CIS) plays an important role in the image efficiency and clearance [2]. As, low noise sensor increases the sensor's ability to see the image by only a few photons. This sensor has a wide application in different fields.

Wide dynamic range CMOS image sensor, also considered very important parameter in determining the sensor performance. Wide dynamic range increases the sensor's ability to capture the details of the image under low and high light conditions [3].

The image sensor is considered the main part of a digital camera, which converts optical information of the light photons into electrical signals. Nowadays, CMOS based imaging arrays have a great growing stage. Besides the low cost and low power consumption advantages, the continual development of CMOS image sensor publicity goes to other parameters such as the capability to integrate the sensors with electronics and the ability to achieve fast, customizable frame rates [4]**.** For all image sensors the low readout noise and high dynamic range are considered two important factors define the sensor quality**.**

Nowadays, the development of CMOS image sensor technology is requiring a lot of efforts to be made to get CMOS image sensor with factors suitable with the existing requirements for imaging technology. Dynamic range of CIS is considered one of the most important parameters of the sensor which must be improved to increase the sensor quality in capturing the image details [5], [6], [7]. In this decade, increasing the dynamic range of CMOS image sensor became the main target even though there are initial methods were already proposed in most commercial sensors in which the dynamic range of the sensor is limited to about 72 dB [8]. There is a more common implementation using multiple exposures which achieved a high dynamic range reaches to 112 dB [9]. Reference [10] provides a new method to increase dynamic range by reducing the input referred noise as the temporal read-out noise. The CIS in [11] introduces a method that achieved a 40% reduction in the input–referred temporal noise.

This paper focuses on increasing the dynamic range of voltage-mode CMOS image sensor and reducing its readout noise by providing a new technique that uses a diode connected transistors in pixel circuitry, and get CIS with high speed.

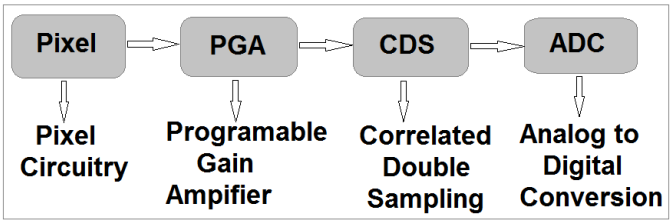

Fig. 1. Block diagram of a typical image sensor.

II. CMOS IMAGE SENSOR OVERVIEW

The block diagram of the typical CMOS image sensor (CIS) system is shown in Fig. 1. The sensor structure consists of a pixel circuitry, programmable gain amplifier (PGA), sample and hold (S&H), and analog to digital converter (ADC). This one pixel can be extended to an array of pixels. Programmable gain amplifier (PGA) is used to amplify the pixel output, (PGA) acts as a variable gain amplifier. In PGA the amplification is controlled by the values of the capacitor array connected between the input and output nodes of the amplifier. To reduce the sensor noise, it must use the sample and hold circuit (S&H) which used as correlated double sampling circuit (CDS). The analog output of the image sensor is then digitized by using analog to digital converter (ADC).

Fig. 2 shows the pixel circuitry structure. The first part of pixel circuitry is photodiode (PD), the pixel uses photodiode (PD) to convert photons of an optical signal into a photocurrent in the electrical signal. After the light incident on the photodiode (PD), the charges will be accumulated and (electron/ hole) pairs will be generated. These charges will be converted into voltage through the floating diffusion capacitance (C_{FD}). Source follower amplifier (SF) is then transferring the produced voltage signal to the output. As a result, the total image system converts the input light into a voltage signal which is converted into a digital signal at the output of the sensor.

A. Traditional Wide Dynamic Range CIS

The traditional voltage mode image sensor circuit diagram [12], [13] is shown in Fig. 3. The pixel circuit contains a photodiode, charge transfer switch (M1) to transfer charge from PD to be stored in C_{FD}. Source follower input transistor (M4) to transfer the voltage on C_{FD} to the output node, (M5) switch for row selection and (M6) is the biasing transistor which can be shared by multiple rows of pixels. There is reset1 switch (M2) and reset 2 switch (M3) are used for reset operation. A lateral overflow capacitor (C_v) is used to improve the dynamic range [12], [13]. The sequence of operation is as follows. Initially the photodiode (PD) is empty from any charges. The reset 2 switch (M3) and the row select switch (M5) are ON, and at the same time the remaining transfer switch (M1) and the reset 1 switch (M2) are OFF. The reset 1 switch (M2) is then ON to enable resetting the floating diffusion capacitance (C_{FD}) and for resetting (Cv).

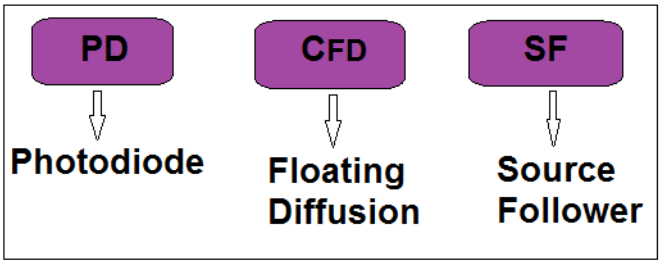

Fig. 2. Pixel circuitry structure.

After turning the switch (M3) OFF, the transfer gate switch (M1) is turned ON, then for getting the voltage on (C_{FD}) another read is occurring. After transferring the generated charges in the photodiode to the floating diffusion capacitance (C_{FD}), the signal will be read by SF (M4, M5, M6). So the total signal will be read out after turning the reset 2 switch (M3) ON. The dynamic range of this technique will increase by increasing the area of the overflow capacitor (Cv) to get a large one. This will reduce the sensor bandwidth so the dynamic range will increase. The drawback of this CIS is the reduction in the bandwidth of the sensor, this reduction in the bandwidth will decrease the camera speed and the maximum frame rate. Also the complexity in designing of the driver control signal circuits is increased.

In the next section we will introduce our proposed WDR CIS, which solve the bandwidth problem required for high frame rate applications.

B. The proposed WDR CIS with Diode Connected Transistors

Fig. 4 shows the proposed voltage mode WDR image sensor. The effect of the added diode connected transistors (M7) as a load and (M8) as a capacitor in the dynamic range, the output noise and the linearity of the image sensor will be described. That the additional transistors (M7) and (M8), which are a diode connected transistor, improves the dynamic range by introducing second current pass and by reducing the readout noise as follow. As M7 gate and drain are short, the transistor operates in saturation.

In saturation for diode mode ($V_{DS} = V_{GS}$) so drain current is given as in (1).

$$I_{DS} = \mu C_{OX} (W/2L)(V_{DS} - V_{TH})^2 \quad (1)$$

Where, V_{TH} is threshold voltage, W is channel width and L is channel length. Cox is oxide capacitance.

The equivalent resistance of this device is given as in (2).

$$R = V_{DS}/I_{DS} = 2L/W\ (1/\mu C_{OX})\ V_{DS}/(V_{DS} - V_{TH})^2 \quad (2)$$

Therefore, the equivalent resistance is depending on the output voltage, it will be changed by changing output voltage (V_{DS}).

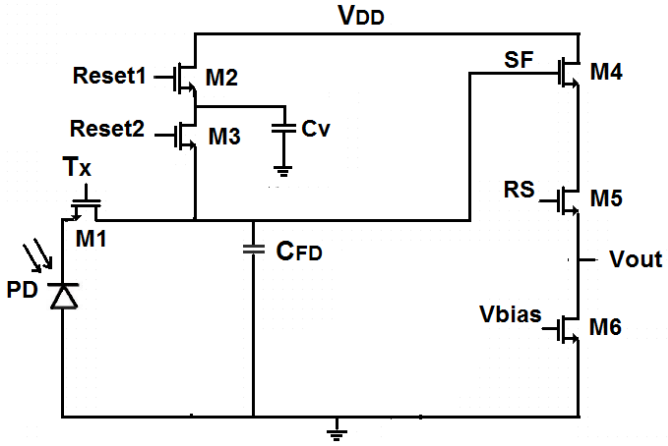

Fig. 3. Circuitry diagram of traditional WDR CIS.

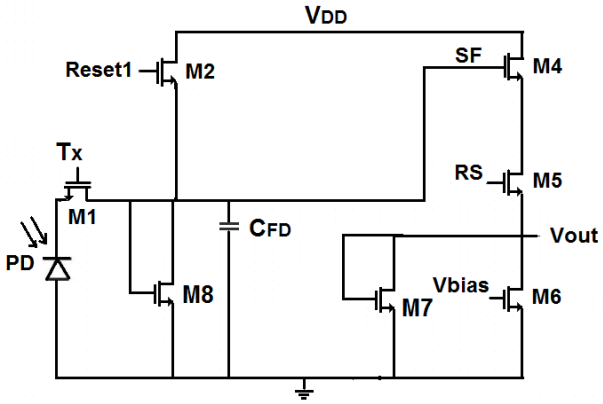

Fig. 4. Circuitry of the proposed WDR CIS with Diode connected transistors M7 and M8.

Because of the increasing in the photodiode current I_{ph}, the voltages on C_{FD} will be increased. Then M4 tries to increase its I_{DS} but it is constant because of the M6 is a constant current source. If M7 is not connected, there will be a large increase in the $V_{DS,M6}$ (V_{out}) to keep $V_{GS,M4}$ constant and so its $I_{DS,M4}$. If M7 is connected, M7 introduces a second path for the currents, so $I_{DS,M4}$ can increase when reducing C_{FD} which results in a smaller increase in $V_{DS,M6}$ (V_{out}). This effect will increase the maximum output voltage linear range at high input photocurrent I_{ph} and so the dynamic range of the sensor will be increased. For connecting M8 in parallel with floating diffusion capacitance, this parallel connection will increase the total capacitance for floating diffusion node as so this will increase the total number of stored charges an so the dynamic range for the sensor will be increased. The effect of connecting M7 and M8 on readout noise reduction will be discussed as follows. If the transistor sees its own output impedance only as a load, then the maximum output noise will be occurred. So if the MOS transconductance decreases, then the noise current of the MOS transistor will be decreased. Because the connection of M7 in parallel with the current source M6 and as discussed previously, M7 will introduce second path for current and so the drain current for M6 will be decreased and so a smaller current and smaller g_{m6} can be used and this will decrease M6 noise and the total output noise of the CIS. By using M7 $I_{Ds,M4}$ can be larger as it equal to $I_{DS,M6}+I_{Ds,M7}$ and higher transconductance of source follower $g_{m,M4}$ is achieved. The source follower noise decreases with increasing its g_m. So the total output noise of the circuit will be decreased. For the effect of (M8) which connected in parallel with floating diffusion node on readout noise reduction as follows. As shown from (7) which is the equation of second noise component, if the total impedance of floating diffusion node is decreased then the total output noise will be reduced. This has been occurred by connecting a diode connected transistor M8. Because of the equivalent resistance of the diode connected transistor is very small which connected in parallel with a floating diffusion node and so the total output impedance of floating diffusion node is deceased and so the total output noise in the image sensor will be decreased due to connecting M8.

III. SIMULATION RESULTS AND DISCUSSION

A comparison between the traditional and the proposed WDR CIS in their results was made , such as maximum input photocurrent, maximum output voltage, bandwidth, output noise, dynamic range and linearity to show the effect of adding a diode connected transistors (M7) and (M8) . This comparison is shown in Table I. As expected the proposed WDR CIS has a bandwidth of (5 MHz) which is higher than the traditional WDR CIS using a lateral overflow integration capacitor, because of the elimination of the overflow integration capacitor (C_v).

A higher dynamic range of 140 dB is also achieved because of the diode connected M7 and M8 effect.

Noise reduction for the proposed CIS can be proved mathematically as following. Firstly, we will prove the total output noise of the circuit before adding the diode connected transistors M7 and M8 as in Fig. 5 and Fig. 6 by using the small signal model of the circuit as follows:

From Fig. 6, we can calculate the components of the output noise, the first component of the noise ($V_{n,out1}$) is due to transistors (M4 and M6) is given as in (3), g_{m4} is the - transconductance of transistor M4. Output sensor circuitry impedance Z_{out} is given as in (4).

$$V_{n,out1}(1-g_{m4}Z_{out})=(I_{n,M4}+I_{n,M6})Z_{out} \quad (3)$$

$$Z_{out}= r_{ds4}//r_{ds6}//X_{CL} \quad (4)$$

The second component of the noise ($V_{n,out2}$) is due to R_x is given in (6) and (7). Equation (5) shows relation between the gate to source voltage (V_{gs4}) and the second component of noise.

$$V_{gs4}= V_{g4}-V_{s4}= I_{n,Rx}X_{CFD}-V_{n,out2} \quad (5)$$

$$V_{n,out2}=g_{m4}V_{gs4}Z_{out} = g_{m4}Z_{out}(I_{n,RX}X_{CFD}-V_{n,out2}) \quad (6)$$

$$V_{n,out2}(1+g_{m4}Z_{out}) = g_{m4}Z_{out}I_{n,Rx}X_{CFD} \quad (7)$$

Where, $I_{n,Rx}$ is a small signal noise component due to M1, and X_{CFD} is floating diffusion capacitance impedance.

From the two components of the noise the total output noise can be reduced by reducing the output resistance Z_{out}, because $g_{m4}\,Z_{out}$ <1 for the SF. Therefore, as shown from equations the total output noise is reduced by reducing the output resistance. This can be done by adding the diode connected transistor (M7) to the circuit as in Fig. 7 and Fig. 8. We replaced the diode connected model with an output resistance = $r_{ds7} = 1/g_{m7}$ and it is very small resistance so as will be discussed later the total output resistance of the circuit will be reduced and the total output noise will be decreased.

TABLE I. Comparison between the proposed WDR CIS with and without diode connected M7 and M8 and the traditional CIS.

Parameter	Traditional WDR CIS	WDR CIS without M7and M8	Proposed WDR CIS
Maximum input photocurrent (I_{ph})	10 µA	11 µA	22 µA
Output noise	94.5 μv_{rms}	92 μV_{rms}	20 μV_{rms}
Maximum output voltage	1.5 V	1.4 V	1.5 V
Bandwidth	43 KHz	45 KHz	5 MHz
Dynamic range	83.7 dB	83.6 dB	140dB
Non Linearity	2.2 %	1.8 %	1.1 %

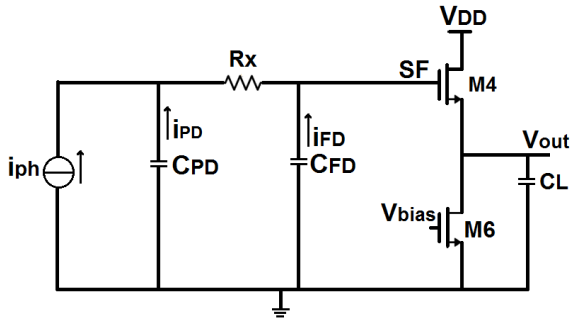

Fig. 5. Equivalent circuit for noise analysis.

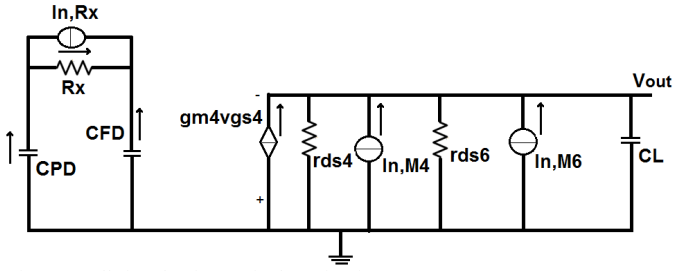

Fig. 6. small signal noise equivalent circuit.

Now we calculate the output noise after adding the diode connected transistors (M7) and (M8) as in Fig. 8. The first component of the noise ($V_{n,out1}$) is due to transistors (M4, M6 and M7) is given as in (8) and (9).

$$V_{n,out1}=(I_{n,M4}+I_{n,M6}+I_{n,M7}+g_{m4}V_{n,out1})Z_{out} \quad (8)$$

Z_{out} = r_{ds4} // r_{ds6} // r_{ds7} // X_{CL} so it is very small resistance because (r_{ds7}) of the diode connected transistor is very small

$$V_{n,out1}(1-g_{m4}Z_{out}) = (I_{n,M4}+I_{n,M6}+I_{n,M7})Z_{out} \quad (9)$$

Where $I_{n,M4}$, $I_{n,M6}$, and $I_{n,M7}$ are small signal noise components due to M4, M6, and M7 respectively.

The second component of the noise ($V_{n,out2}$) is due to the R_X is given in (10).

$$V_{n,out2}(1+g_{m4}Z_{out}) = g_{m4}Z_{out}I_{n,Rx}X_{CFD} \quad (10)$$

A comparison between the proposed CIS simulated output noise results using Cadence and the Matlab has been done. In Matlab circuit model has been built using pixel circuitry equations for output noise and drawing a relation between the output noise power and the frequency. In cadence the relation between noise power and frequency has been drawn by cadence tools. As shown in Table II that both results are nearly equal to each other, this proves that our noise model is valid. Fig. 9 and Fig. 10 prove the validation of the proposed noise model by plotting the output noise power spectral density results obtained by circuit simulation using Cadence and Matlab calculations in the noise model.

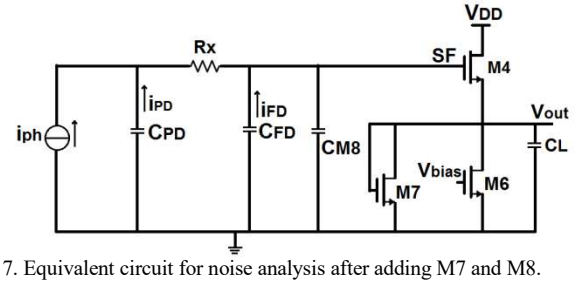

Fig. 7. Equivalent circuit for noise analysis after adding M7 and M8.

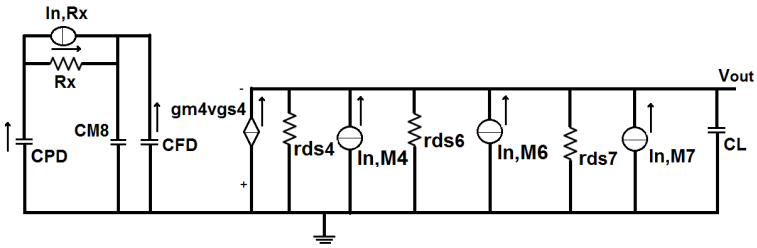

Fig. 8. small signal model and noise equivalent circuit for proposed WDR CIS.

TABLE II. Comparison between the output noise values by using Cadence and the developed mathematical model using Matlab.

Traditional WDR CIS	In Cadence = 94.5μV_{rms}	In Matlab = 95μV_{rms}
Proposed WDR CIS	In Cadence = 20 μV_{rms}	In Matlab = 21μV_{rms}

Fig. 9 and Fig. 10 show the plotted results of the mathematical noise power model by Matlab and simulated results for the proposed pixel output noise power using Cadence. It is clear from the plotted results that they are nearly equal to each other. This means that our noise model is correct. The output noise power shown in Fig.9 for the proposed CIS is smaller than the CIS output noise power for traditional CIS shown in Fig. 10.

Fig. 11 shows the readout timing diagram of the CMOS image sensor. Fig.11 shows the input and the output signal shapes on transfer gate switch (M1), Reset1 switch (M2), Row select switch (M5), and the pixel output. During readout the photodiode accumulates the photogenerated electrons. The transfer gate switch (M1) will transfer these charges from the photodiode to the floating diffusion (FD). During readout the Row select switch (M5) is always on, and the Reset1 switch (M2) is turned on to empties the floating diffusion (FD) from electrons. After the accumulation of the photoelectrons in the photodiode, the transfer gate switch (M1) is turned ON to transfer the cumulative photoelectron to the capacitor (C_{FD}). Then the source follower (SF) will sense the voltage on (C_{FD}) so the reading out of the signal is performed. M8 will increase the dynamic range because it connected in parallel with C_{FD}, and so this will increase the capacity of the floating diffusion node to store more charges so the dynamic range will be increased.

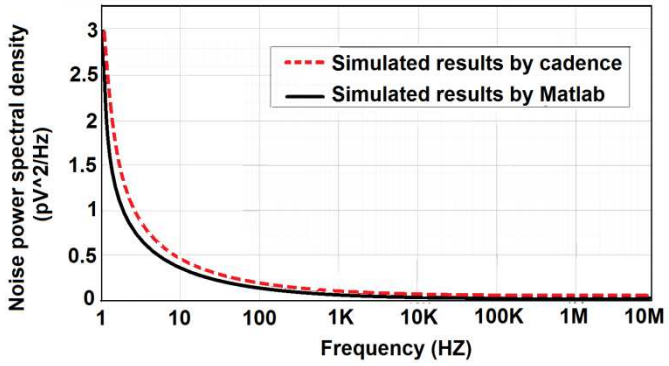

Fig. 9. The simulated output noise power spectral density of the image sensor by Cadence compared with calculated noise model results by Matlab for proposed WDR CIS.

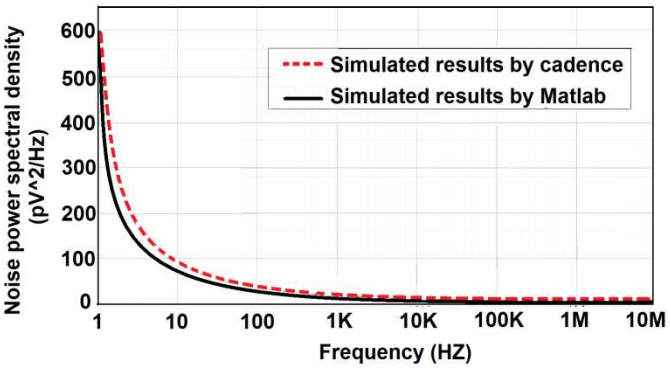

Fig. 10. The simulated output noise power spectral density of the image sensor by Cadence compared with calculated noise model results by Matlab for the traditional CIS.

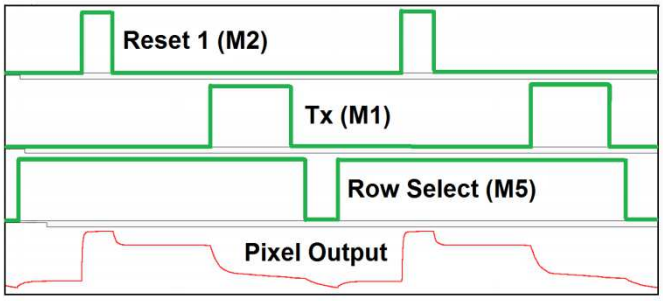

Fig. 11. The simulated transient waveforms of (transfer, reset, row select and pixel output) at input current of 50 nA.

Fig. 12 shows the plot between sensor output voltage and input photocurrent to show how the sensor nonlinearity can be measured. The calculation of the nonlinearity begins with the plot of the output signal level versus the input photocurrent. The nonlinearity value is usually expressed in percentage, based on the swerve of the output signal from an ideal straight line, based on the measurement results, there will be some restrictions that must be taken into account during the analysis of the proposed CMOS image sensor to reduce the nonlinearity of the sensor such as the sizing of the source follower transistor and the floating diffusion capacitance, which must be kept as small as possible to get a high linearity. From the plotted results it is clear that the linearity of the image sensor is ensured for input photocurrents up to 22 µA, since the pixel nonlinearity reaches to 1.1%. In the proposed results the nonlinearity was reduced due to the small area used for source follower and diffusion capacitance and due to diode connected load technique.

Fig. 13 shows a typical layout of the proposed image sensor. The sensor was designed and implemented in a 130 nm CMOS technology, the pixel occupies an area of 3 µm x 3 µm, which is the typical area for CIS. The proposed pixel's area contains seven NMOS transistors and one capacitor. To get a good fill factor for the sensor which is the ratio between the-photodiode area and total sensor area, so the distance between the n-well, the neighboring NMOS and the capacitors must be as small as possible. This small distance taken into account during the design of the proposed CIS, also the layout keeps all the rules required for the technology.

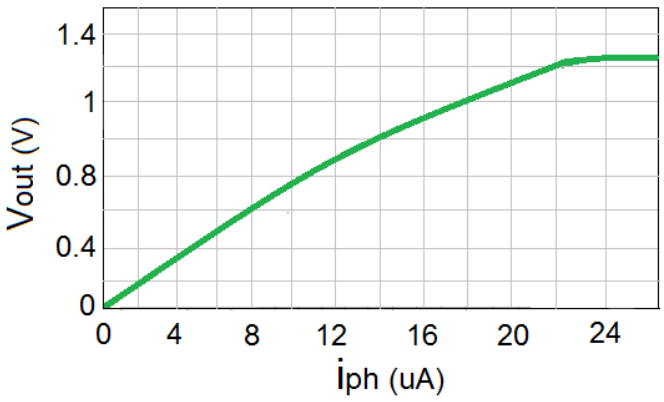

Fig. 12. Simulated results of the input photocurrent with the image sensor output voltage.

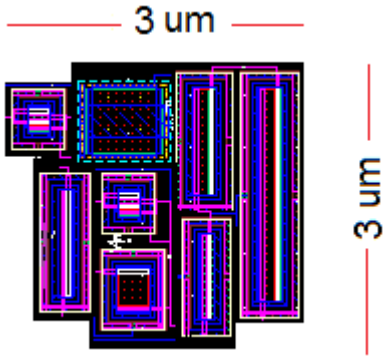

Fig. 13. Proposed pixel circuitry layout.

Table III summarizes all the simulated results for the proposed CMOS image sensor. From these results it is clear that the dynamic range is enhanced to 140 dB. This WDR is achieved by reducing the noise of the image sensor which reached to 20 μV_{rms}, in addition to extending the maximum input current range up to 22 µA. Also the bandwidth extends to 5 MHz, which helps to increase the CIS frame rate. The pixel is consuming 10 µW using 1.6 V single power supply which is considered as low voltage operation.

TABLE III. Summary of The post Layout Simulation Results Obtained From The analysis of the proposed CMOS Image Sensor.

Parameter	Results
Technology	130 nm CMOS technology
Power supply	1.6 V
Maximum input current (I_{ph})	22 µA
Maximum output voltage	1.5 V
Conversion gain	36 µV/electron
Output noise	0.61 e-rms (20 µVrms)
Bandwidth	5 MHz
Dynamic range	140 dB
Dissipated power	10 µW
Non Linearity	1.1 %

TABLE IV. Comparison of the proposed CMOS image sensor (CIS) with the recently published CIS.

	This Work	[14]/ 2020	[15]/ 2017	[16]/ 2018	[17]/ 2018	[18]/ 2020
Technology	**130 nm**	40 nm	0.14 um	BSI	65 nm	0.18 um
Voltage supply	**1.6 V**	1.8/ 3.3 V	2.7/1.8 V	-----	1.2/ 2.5 V	3.3 V
Bandwidth	**5 MHZ**	-----	72 MHZ	-----	-----	20 MHZ
Readout noise	**0.6 e-rms**	0.6 e-rms	1.3 e-rms	1.1 e-rms	6.2 e-rms	-----
Dynamic Range	**140 dB**	132 dB	-----	90 dB	121 dB	120 dB
Pixel Area (μm^2)	**3 x 3**	3x 3	1.65x1.65	3 x 3	3 x 3	16 x 16
Dissipated Power	**10 uW**	-----	40 mW	280 mW	-----	-----
Conversion Gain	**36 uV/e-**	54/6.7 uV/e-	77 uV/e-	21 uV/e-	-----	-----

Table IV compares the proposed CIS performance with the state of the art of recently published CIS. It is clear from this comparison that the proposed noise results are reduced a lot compared with the others work. Also, the supply voltage operation (1.6 V) is considered a small supply compared with the others work. The dynamic range was extended to 140 dB. The pixel area which is considered small and suitable area for high fill factor CIS. The only drawback in our work is the slightly bandwidth reduction of CIS, but our value is still considered a suitable value for CMOS image sensor (CIS).

IV. CONCLUSION

Based on the obtained results, the effect of adding diode connected transistors M7 and M8 improves a lot in the dynamic range and readout noise of CMOS image sensor. As shown in the traditional WDR CIS the use of overflow integration capacitance reduces the bandwidth of the sensor and so its speed is reduced. In the proposed WDR CIS by using diode connected transistors the readout noise reduced to 20 μV_{rms} (0.6 e-rms**)** compared with in traditional CIS, which reached to 94.5 uV_{rms} also, bandwidth in the proposed circuitry extendes to 5 MHz compared to the traditional one in which reached to 43 KHz. As this reduction in readout noise in the proposed CIS, the dynamic range is extended to 140 dB after adding a diode connected transistors M7 and M8 compared to traditional in which dynamic range reached to 83.7 dB.

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