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A 10W, 2-5 GHz Highly Linear Power Amplifier

B. M. AbdelRahman^{*}, H. N. Ahmed[†], M. E. Gouda[‡]

Abstract: In this paper, a 2 to 5 GHz (116% fractional bandwidth), highly linear power amplifier – based on GaN HEMT- with an output power excess of 10W is presented. The load pull technique is used to reach the optimum performance within the useful bandwidth. Electromagnetic simulations are carried out to model the matching networks on the substrate. The design is optimized based on the results of these electromagnetic simulations. Wideband matching, together with stability circuits are adopted to achieve a flat power gain of 7.7 ± 0.75 dB over the entire operating bandwidth, providing optimal fundamental and harmonic impedances within more than one octave of operation. The designed power amplifier exhibits a small signal gain more than 7.85 ± 0.75 dB, third-harmonic intermodulation distortion products (IMD3) far below -35 dBc at an input power of 29 dBm over the entire frequency band, and a power added efficiency (PAE) better than 15%. Using a two-tone test bench with a frequency spacing of 100KHz, a maximum value of the output OIP2 and OIP3 are found to be greater than 55 dBm and 45 dBm, respectively.

Keywords: linear, wideband, GaN, power amplifier

1. Introduction

Broadband power amplifiers covering L, S and C frequency bands have very great challenge in communication systems because of their applications in wireless, radar, aerospace and military systems [17]. This has triggered an increasing demand for ultra wideband RF amplifiers as part of the next generation base station transmitters. Design of such amplifiers to cover multi-octave bandwidth needs an accurate and efficient procedure starting with transistor selection.

Load pull characterization and precise modeling of components used. An increasing attention of scientific research is dedicated to the design of high performance power amplifiers [1][2][3][6].

Recently, different types of broadband power amplifiers, based on GaN HEMTs, have been published [6][10][11]. One of GaN's unique properties is its device physics properties, which enable it to perform in existing and new applications of wide-bandgap, high breakdown voltage, high power density, and high-gain performance. Using GaN for microwave devices provides 10 to 30 times more power and insulated gate advantages over competing technologies, such as silicon. Due to their superior thermal and voltage breakdown properties and the feasibility of growing them on relatively high-thermal conductivity SiC substrates, GaN devices have relatively high power density with smaller die size, as well as smaller

^{*} Arab Academy for Science & Technology, Cairo, Egypt; <u>major.bassem@yahoo.com</u>

[†] Egyptian Armed Forces, Egypt; <u>hnmahmed@ieee.org</u>

[‡] Misr University for Science & Technology, Cairo, Egypt, <u>dr_mamdouh2004a@yahoo.com</u>

parasitic capacitances, when compared to silicon LDMOS FETs and GaAs MESFETs of similar output power. This allows relaxed operating conditions, low supply currents, and easy impedance matching which reduce design effort and makes GaN HEMTs the optimum choice to handle high power while exhibiting broader bandwidths than those demonstrated by other technologies[1], [6].

In this work, a broadband, highly linear power amplifier based on Cree's commercially available CGH40025F 25-W GaN HEMT [9] is presented. The paper is organized as follows; section II presents transistor selection. Section III introduces the proposed amplifier design procedure together with the synthesis of the low loss of the input and output matching networks. Small signal, as well as large signal simulation results, is presented in section IV. Section V summarizes and concludes the work.

2. Transistor Selection

The goal of this work is the development of a wideband, highly linear amplifier covering the frequency band from 2 to 5 GHz with the following design specifications: saturated output power Pout \geq 40dBm, power gain Gp \geq 7.7dB, OIP2 and OIP3 of more than 55 and 45 dBm, respectively and IMD products \leq -35dBc.The first and most important step is the selection of the appropriate transistor so as to meet the above mentioned amplifier specifications. Cree's CGH40025F GaN HEMT renders itself as one of the most appropriate choices for such a design [9], with a wide frequency range extending up to 6GHz, an output saturation power Psat of 30W, and a small signal gain of 13dB at 4 GHz. The operating drain voltage, according to the manufacturer recommendations, is chosen to be 28V. For class AB operation, the optimum gate biasing is found to be -2.865V which produces a drain current of 250 mA.

3. Proposed Amplifier Design

Based on the selected transistor, two tone load pull simulation test bench, as shown in Fig. 1, has been setup using source and load tuners to characterize the used device within the required bandwidth in an attempt to reach the optimum source and load impedances that deliver the maximum power, as well as maximum possible linearity, with appropriate power added efficiency.

Load pull simulation is used to obtain the optimized load and source impedance providing the best trade-off between maximum output power and maximum intermodulation (IMD) suppression over the whole bandwidth. Optimization was necessary in order to find a tradeoff between output power and IMD, and to obtain a flat behavior over the whole bandwidth. Table I depicts the optimized values of the source and load impedance for maximum P_{out} and maximum IMD suppression over the entire operation bandwidth [6][17].

After extraction of the optimum values for source and load impedances, a design procedure is followed to reach the input/output matching networks. First, Design the output matching circuit as an impedance transformer to transfer 50 Ohm into the optimum load impedance of the output stage. Second, Design the input matching circuit to provide a conjugate match between the input impedance and 50 Ohm so that a good input return loss can be obtained conjugate matches the obtained optimum load from the load pull simulation. The broadband input/output matching circuits are designed as in [18]. Finally, the input and output matching networks are optimized to stabilize the circuit, decrease the power loss, and flatten the gain within the operation bandwidth. [17][6][18].



Fig. 1 Test bench used for two tone load pull simulation

Frequency [GHz]	Optimum Source Impedance Z _s		Optimum Load Impedance Z_l		Maximum Output Power	IMD[dBc]
	Re Z_s	$\mathrm{Im}Z_{s}$	Re Z_L	$\mathrm{Im}Z_{L}$	[dBm]	
2.2	5.502	5.6285	6.1075	3.01265	37.5	-40.2
3	4.9475	5.6415	5.545	3.02065	36.6	-37.5
4	3.1652	9.6815	6.973	2.99885	36.4	-36.4
5	1.0526	10.079	6.473	2.49885	38.1	-35.6

 Table 1 Optimized source and load impedances for maximum output power and minimum IMD

To enhance the amplifier's unconditional stability (K>1) at low frequencies, an R-C parallel combination $(R_S//C_S)$ is inserted at the input. This combination also gives better performance concerning input impedance matching; this technique is called lossy match technique. To furthermore enhance the amplifier's unconditional stability R_G is added in the gate bias line [17][6][18].

4. Simulation Results

4.1. Small Signal Performance

The simulated results of the amplifier stability, small signal gain, input and output return losses are depicted in Fig. 2 and Fig. 3, respectively. From Fig. 2, it is clear that a linear gain of 7.85 dB with a flatness of ± 0.75 dB is achieved, while a stability factor k, better than 2.5, is obtained throughout the whole bandwidth. From Fig. 3, an input return loss of better than 7 dB is achieved.



Fig. 2 Gain and stability factor vs. frequency



Fig. 3 Small signal gain, input return loss

4.2. Output Power and Linearity Performance

The power performance of the designed power amplifier at 5 GHz is shown in Fig. 4. The designed amplifier achieves a 1-dB compression point of 33 dBm. At the 1-dB compression point, the power gain is 7.7 dB and the PAE is 27%. Wideband power performance as well as power gain flatness is shown in Fig. 5; the input power is swept over a range from 10-34dBm, a flatness of ± 0.75 dB for the power gain is evident from the graph.



Fig. 4 Output power, power gain and PAE @ 5 GHz



Fig. 5 Output power over the operation bandwidth for input power from 10-34 dBm

Linearity performance is quantified using the two-tone test; two tones, 27dBm each, 100 kHz apart, centered around 2.4 GHz, 3GHz, 4GHz and 5GHz, respectively are applied to the amplifier input. The resulting third order inter-modulation distortion product, shown in Fig. 6 is found to be at -40.2dBc,-37.5dBc,-36.4 dBc and -35.6dBc, respectively. It is clear from the results that the designed PA shows good linearity.



Fig. 6 Two-tone simulation results

The third order intercept point over the whole amplifier operation bandwidth is shown in Fig. 7. It is found to be greater than 45dBm in the frequency range between 2-5 GHz.





Agilent's Advanced Design System (ADS) has been used to perform EM-simulation of the complete power amplifier circuit to account for the board layout parasitic effects (such as coupling, bends, steps, discontinuities, GND pads, via holes, etc.)., Fig. 8 shows the results of the EM-simulation for the output power as a function of the input power. The obtained result is comparable to the circuit simulations as that shown in Fig. 9. The circuit together with the designed multi-section input/output matching circuits uses Rogers 4350B laminate with 0.762mm thickness, a dielectric constant of 3.48, and a loss Tangent of 0.004.



Fig.8 Output power after EM-simulation for the designed PA



Fig. 9 10 W power amplifier layout for EM-simulation

5. Conclusion

In this paper, a 10W, wideband, highly-linear RF power amplifier has been designed using GaN HEMT, covering the frequency range from 2-5 GHz (116%). The transistor is biased at $V_{DS} = 28$ V and $I_D = 250$ mA, where all small/large signal parameters are evaluated. A small signal gain of 7.85 dB with gain flatness of ±0.75 is achieved using both lossy match and broadband matching networks. Power performances and amplifier linearity obtained at this operating point result in 7.7 dB power gain, 33dBm 1-dB output power, 15% PAE and >45dBm OIP3. Third order inter-modulation products have been evaluated and found to be better than -35dBc over the whole amplifier bandwidth.

6. References

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