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New Digital Testing of Analogue Circuits

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Abstract: This paper presents a new parametric fault detection approach for analogue circuits based on the digital signature analysis. This approach has two main parts, an analogue test pattern generator (ATPG), and an analogue test response compactor (ATRC). The proper ATPG is designed to sweep the applying sinusoidal frequencies to match the frequency domain of the analogue circuit under test (ACUT). The output test response of the ACUT is acquired via the analogue-to-digital converter (ADC). The ATRC accumulates digital samples of the output response from the ADC to generate a digital signature that can characterize the situation of the ACUT. The signature comparison is achieved based on signature boundaries and the worst-case analysis. In addition, the signature curve for each component variations in the ACUT is presented. It combines effective parameters of the transfer function of the ACUT with respect to the component variations. These parameters are the band-width and the passband transmission. In this paper, the hardware implementation is achieved using the field programmable gate array (FPGA) technology as the digital part and the analogue part that includes the data conversion. The digital test controller is designed to enable the proper control and synchronization of the analogue test cycle for stable digital signature generation. The presented testing approach is applied to the ACUT in the range of biomedical applications to validate it. Based on the presented hardware implementation, the signature curve for each component of the ACUT is derived for the ACUT judgment.

Keywords: Fault detection, Parametric faults, Signature analysis of analogue testing, Testing of analogue circuits.

1. Introduction

Automatic testing techniques play a great role in industrial applications. They are considered as standard way for detecting faults in digital and analogue electronic systems. Researchers are concentrated their major attention to the automatic testing of the digital systems [1-9]. However, in most cases the digital system exists within an analogue enclosure system. This analogue part of the mixed-signal system requires to be tested for increasing the system performance. Testing applications of analogue circuits are still in research phase. In general, the most challenge of fault detection of the analogue circuits is to unify test procedures to properly generate test signals that are capable of stimulating faults, and to compact the test response for fault detection [10]. The analogue testing has to fit the specifications of the the analogue circuit under test (ACUT) [11]. In addition, the modeling of hardware defects of the ACUT and the usage of these models for developing and improving test signals is considered another analogue testing challenge.

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The manufacturing defects may have two types of permanent faults, namely catastrophic (hard) or parametric (soft) faults [12]. A catastrophic fault is one in which discrete component of a circuit is destroyed (e.g. short circuit, open circuit as well as topological change). With parametric fault, the component is still functioning but out of nominal tolerance band (out of specification). Figure 1 depicts the classification of analogue circuit faults. The range of the acceptance for the good ACUT, and the non-acceptance are illustrated for ± 5 %. Comprehensive researches have been conducted on analogue testing issues. Faults in an analogue circuit may occur due to a catastrophic fault model, considered easily to test. In the parametric fault model, it is hard to test, and its effect is represented by means of the change in circuit output signals.

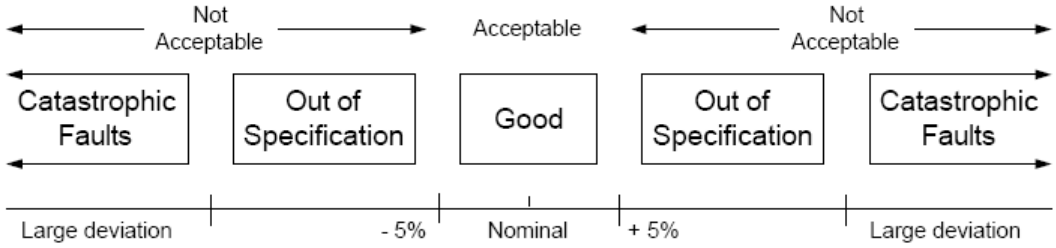

Fig. 1. Classification of analogue circuit faults.

The testing of digital and analogue circuits for correct operation after manufacturing is an important issue. It is how to apply the proper test patterns to the PCB, to analyze the test response, and to locate faulty components. The automatic test equipment (ATE) architecture achieves this objective and is considered a standard way for detecting faults in digital and analogue electronic systems. Researchers are concentrated their major attention to test digital systems since two decades. However, in most cases, the digital systems exist within an analogue enclosure system. This analogue portion of the mixed-signal system requires to be tested for increasing the system performance. In general, the most challenge of fault detection of analogue circuits is to unify test procedures to properly generate test signals that are capable of stimulating faults, and to compact the test response for fault detection [13]. The analogue testing has to fit the specifications of the analogue circuit under test (ACUT).

Several testing techniques for analogue circuits are attempted. Some testing approaches aim to test analogue circuits based on approximated impulse and step test signals [14-20]. The limitation of these approaches is the requirements generation of the ideal impulse. Therefore, an approximation of large-amplitude and narrow-duration is performed. As an impulse signal is shortened, its amplitude must be increased, and this may overload the ACUT. The shape and scale of the frequency spectrum of an impulse response or a step response is fixed. In other word, the power cannot be concentrated to any arbitrary frequency bands, which is not useful to target specific faults. In addition, impulse and step responses can characterize only linear system, which limits their applicability. The other testing approaches aim to test analogue circuits based on the input binary sequence [21-23]. They require extra hardware for stimulus generation and extra hardware at the output for analogue test response analysis (e.g. ADC or cross-correlators). Binary sequence (Square wave) has fixed frequency spectrum shape depending on the clock frequency. Its frequency spectrum follows the shape of the $(sin(x)/x)$ function and includes only the odd harmonics. The binary signals (Impulse, step, square wave and binary sequence) cannot have more power at any arbitrary frequency bands. Thus, they cannot effectively excite the ACUT at pre-specified parts of the frequency spectrum.

Another testing approach aims to test analogue components in mixed-signal circuits, based on oscillation-based BIST (OBIST) methodology [24]. The limitations with that approach are that the catastrophic faults are considered only. The Multi-Detect test method for test

generation is another test approach to identify a set of sinusoids. It forms the test set that maximizes the difference between the responses of the good and faulty ACUT [25]. A faulty circuit is detected from a deviation of its oscillation parameters. The detection circuitry is provided by a single reference value as a reference input to the response comparator instead of multiple reference values for all faults in an ACUT. The limitations of that approach are the problem of finding the minimum detectability threshold between good and faulty circuits for detecting a fault. Estimating the detectability threshold for a given fault is affected by increased number of components, tolerances associated with each component, evaluation of the complex equations, and measurement accuracy of the response analysis circuit (i.e., comparator circuit). Therefore, this approach became too expensive in terms of computation time. Any attempt to reduce the computation time by using simple design models may result in inaccurate detectability threshold value. The testing approaches, based on wavelet filters to analyze and compress signatures [26-27], depend on acquiring the ACUT output response, and processing this response via an array of filters, each operates within a defined band, followed by a signature generator and comparison module for each band. The limitation of that approach is not using the multi-tone test input. Since a single frequency component is not effective in detecting faults.

From the most collected published testing approaches of analogue circuits, the practical implementation of the analogue testing focused on the detection of the catastrophic faults in the ACUT, but it has a shortage of the testing application of parametric faults in the ACUT. The main motivate is to build an efficient analogue testing scheme including the multi-test pattern generation capabilities (ATPG) to match the ACUT, the ATRC to characterize the ACUT based on inserted faults and component tolerances. The main objective of this paper is to design, and implement the parametric fault detection approach for analogue circuits. The proper ATPG is designed to sweep the applying sinusoidal frequencies to match the frequency domain of the ACUT and then is acquiring the output test response, via the ADC. The analogue test response compactor (ATRC) acquires and then compacts digital samples of the output response to generate a digital signature that characterize the situation of the ACUT. The signature comparison is achieved based on the pre-calculated signature boundaries, calculated based on the worst-case analysis of both the minimum and the maximum of the output analogue response of the ACUT using PSpice circuit simulator. In this paper, the presented testing approach achieves the concept of the signature curve generation for each component of the ACUT. Based on this curve, the relation between the digital signatures and the component variations of the ACUT is presented. The signature curve combines the effects of both the band-with (BW) and the passband transmission (A_{max}) in the amplitude response of the ACUT with respect to the component variations of the ACUT. In the hardware testing architecture, the proper digital test stimulus, applied to the DAC, is used to generate the ATPG that sweeps its frequency to match the ACUT. The test response from the ACUT is acquired through the ADC, and then is compacted to generate a digital signature from the ATRC. The performance evaluation is achieved by the frequency sweep to stimulate parametric hardware faults of ACUTs, and the signature curve of each components of the ACUT is deduced from the real hardware system. In addition, the test controller enables the control and synchronizing of the analogue test cycle. The presented hardware testing architecture is applied to the practical implementation of the ACUT, selected from the standard analogue benchmark circuits [28]. The presented ACUT, utilizing in this paper, is concerning to the frequency range of biomedical applications.

Bio-potential signals mostly arise from natural physiological processes, such as potentials of the muscular tissues (electro-myogram - EMG), brain potential (electro-encephalogram - EEG), cardiac potentials (ECG - electro-cardiogram), potentials of the ocular tissue (EOG - electro-oculogram), blood pressure signals, and respiratory signals, etc. These signals are

interfaced to the real world in the analogue nature using analogue amplifiers and analogue filters [29-30]. The frequency ranges of bio-potential signals are illustrated in Table 1.

Table 1. Frequency range of bio-potential Signals.

Bio-potential signals	Frequency Range
Electrocardiogram (ECG)	0.05 – 100 Hz
Electroencephalogram (EEG)	DC – 100 Hz
Electromyogram (EMG)	DC – 5000 Hz
Electrooculogram (EOG)	DC – 50 Hz
Blood flow	DC – 20 Hz
Respiratory Rate	0.1 – 10 Hz
Body Temperature	DC – 0.1Hz

This paper starts with the introduction summary of the new analogue testing approach. The second section is concerned with the design of the presented analogue testing approach. The third section will focus on the PSpice circuit model simulation of the ACUT and the parametric fault analysis of the selected ACUT as the case study. The fourth section is concerned with the implementation of the new analog testing approach. Finally, experimental results and conclusions are presented.

2. Design of the New Analogue Testing Approach

The objective of the presented analogue testing approach is to design the proper ATPG (stimulus) for stimulating the highest possible proportion of all hardware faults, and to design the proper ATRC that can detect the stimulated faults. The main block diagram of the analogue testing architecture, presented in this paper, is shown in Figure 2. This testing architecture is suitable in the external testing approach. The ATRC consists of three sub-modules; the rectifier, the ADC, and the test response compactor (TRC). The rectifier is designed to rectify the negative analogue signal to positive one in the case of the bipolar analogue signals. The ADC is used to convert the analogue signal of the output response of the ACUT into the digital samples. The TRC, composed of the double-precision accumulator, accumulates and compacts the generated samples to produce a digital signature.

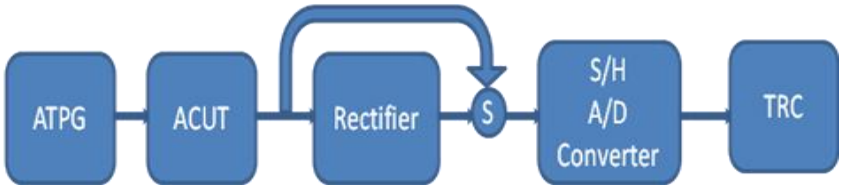

Fig. 2. Main block diagram of the presented analogue testing approach.

Most of faults in analogue circuits can affect the frequency response of the ACUT. Therefore, in this architecture, the proper ATPG is designed to sweep the applying sinusoidal frequencies that provide a stimulation to detect faults in a wide range of analogue circuits. The frequency sweep in the sinusoidal waveform can exercise the frequency response of the ACUT. The existence of faults can affect the frequency response of the ACUT, and change the output waveform of the ACUT. Therefore, the change of the generated digital signature from the ATRC will be significant. The transfer function coefficient variations of the ACUT will prevent an exact output response sequence. Unique digital signature cannot be obtained for the fault-free ACUT. Therefore, in this paper, the ATRC function is an accumulator that sums the sample magnitude of the absolute analogue output response. This facilitates the determination of a range of good digital signatures to account for acceptable changes in the output response due to component variations of the transfer function coefficient of the ACUT.

The analogue output response is generated from the circuit model of the ACUT to verify the effectiveness of this presented analogue testing approach.

During analogue fault simulation, many parametric faults have been considered for each component of the ACUT, including ±5%, ±10%, ±20%, ±50%, … variations of specified component values, short-circuit and open-circuit (i.e., very small value and very large value) in the components of the ACUT. The analogue fault simulation of the ACUT is performed using in the PSpice circuit simulator to illustrate the effectiveness of the new digital signature approach for analogue fault detection technique. Digital signatures based on the accumulation absolute sum of the sample magnitude of the ACUT outputs during test window can be plotted against the selected component variations of the ACUT, called signature curve with respect to that component. This curve illustrates the classification of the fault-free and the faulty ACUT with respect to that component based on parametric faults.

2.1 Analogue test pattern generator

The frequency change of the input signal, applied to the ACUT, controls the amplitude response of the output response. The rate of the frequency sweep is not a constant, but it may vary with each new generated cycle of the ATPG. In this section, the sweep sinusoidal frequency extraction procedure is used to affect the amplitude response of the ACUT and consequently affect the output response of the ACUT through its time domain I/O relation. Figure 3 illustrates the simulation model of the ATPG in this analogue testing architecture [31]. It is the modeling of voltage controlled oscillators (VCOs) using PSpice circuit simulator. It consists of two parts; the Sin Source Model, and the Integrator Model. A simple form of the VCO is obtained by starting with the time domain function for a sinusoidal source model (sin((2π × fc × time) + phi)). In this example, 2π, fc and phi are all constant global parameters. The single frequency source can be turned into a VCO by making phi a function of a controlling voltage instead of a constant. y(t) = sin (2π fct+φ(t)). The instantaneous frequency is given by the time derivative of total phase: 2πfinst = 2π fc + φ′(t). The relationship between the frequency deviation fd = finst – fc, and□ φ□□ is given by: φ (t) = ∫ 2π fd(t) dt. For a linear VCO, we want fd to be proportional to the controlling voltage vctrl, therefore: φ (t) = 2π k1∫vctrl(t) dt, where k1 is in Hertz/volt. Using PSpice circuit simulator [7], the integrator can be modeled as a controlled current source plus a capacitor. The varying phase term is added into the controlled voltage (Sine) source.

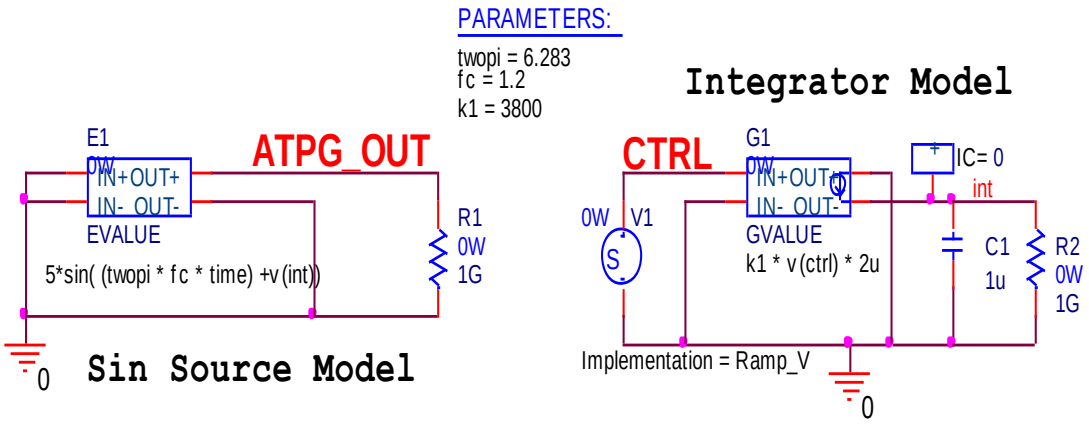

Fig. 3. Model of the ATPG model in the PSpice simulation.

Figure 4 shows the timing diagram of the output signal ATPG_OUT of the VCO model. The sweep signal CTRL controls the frequency sweep to produce the output signal ATPG_OUT. It is the mix of multi-frequency sinusoidal signals. The amplitude is set to 5 Vpp, fc is set to 1.2 Hz and k1 is set to 3.8 kHz/volt. The extracted sinusoidal signals have the frequency

sweep from 1.2 Hz to 1.5 kHz. The output signal ATPG_OUT can be used to stimulate analogue filter circuits in the frequency range of the biomedical applications.

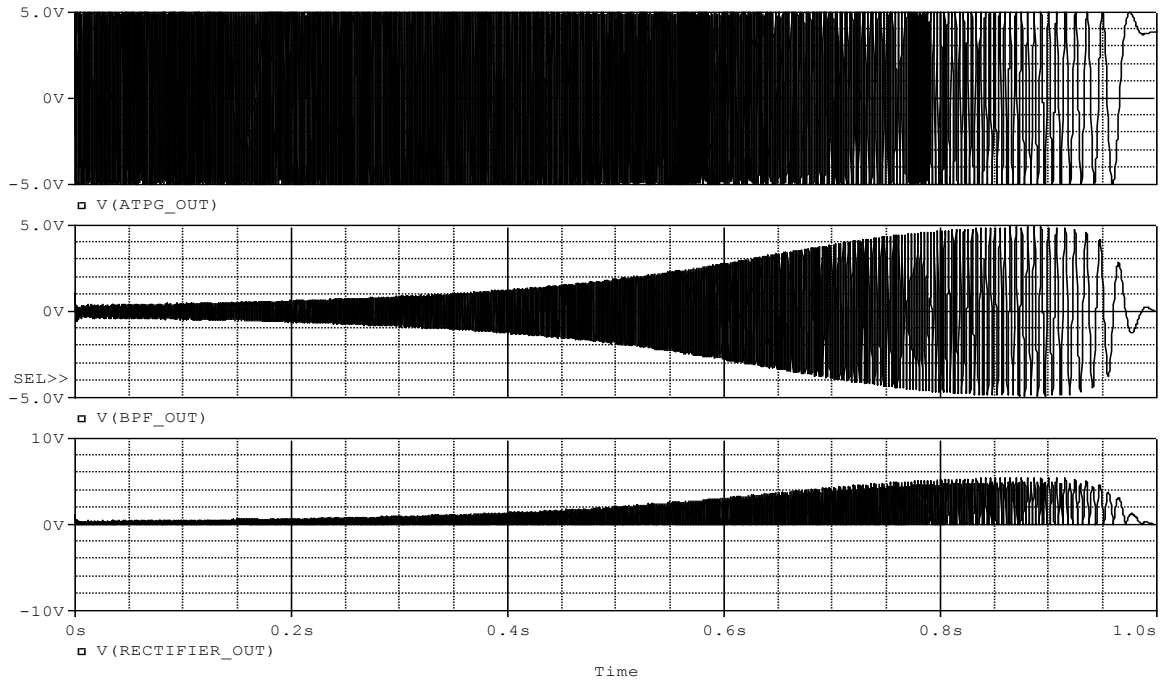

Fig. 4. Timing diagram of the circuit model of the analogue testing.

2.2 Full rectifier circuit and Analogue-to-digital converter

According to Figure 2, the output signal of the ATPG model is applied to the ACUT whose output signal is applied to either the full rectifier circuit or the ADC. The output waveform of the rectifier stage produces unified signal waveform in the positive polarities. Figure 4 shows the timing diagram of the output signal of the ACUT and the output signal of the rectifier.

The ADC is the main part of data acquisition systems. To process applied signals, the sample and hold (S/H) process and data conversion are required. Figure 5 shows the 8-bit ADC model. The control signal S/H is generated to place the input analogue signal ADC_In in the sample mode and the hold mode, and the control signal RESET is generated to start the data conversion cycle. The proper data conversion is to sample the analogue signal in the sample mode, and holds the signal constant during the hold mode. The timing is adjusted so that the encoder performs the conversion during the hold time. The control signal S/H clocks the ADC and the input analogue signal ADC_In is converted. Once a conversion cycle is started, it cannot be stopped or restarted until the data conversion cycle is complete and the data is available from the binary output, A[8:1]. The binary data output of the ADC is applied to the test response compactor (TRC) stage.

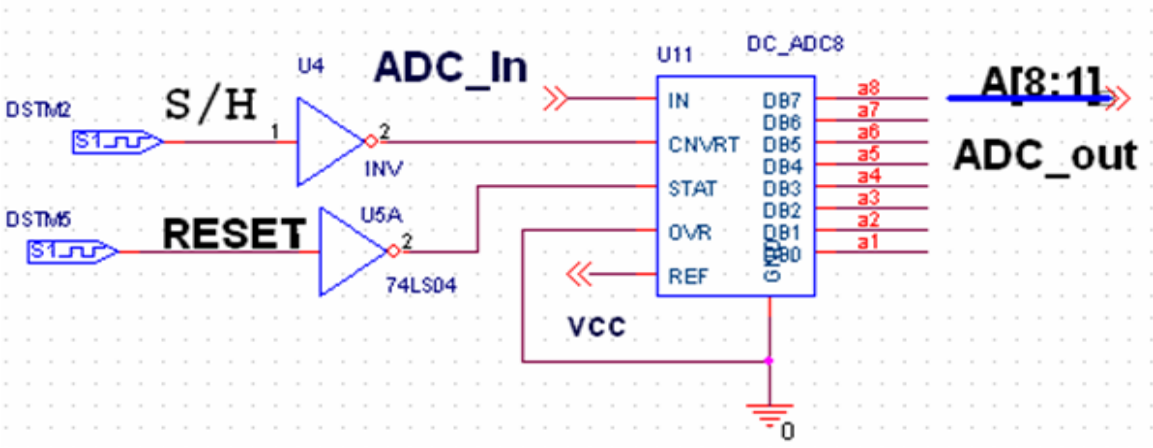

Fig. 5. Schematic diagram of the 8-bit ADC model in PSpice simulator.

2.3 Test response compactor

In traditional testing approaches of digital circuits, the good circuit is tested by a digital signature, generated from the linear feedback shift register (LFSR) [3, 5]. In addition, the single-shot circuit is tested by generating a digital signature based on the measurement of the time duration that expresses the proper functionality of the single-shot circuits [7]. In analogue circuits, the test response (TRC) function is design to generate a digital signature based on accumulation weighting sums of the sample magnitude of the analogue output response. These samples are generated from the ADC, and the required digital signature is generated from TRC by accumulating those samples. These samples are based on the analogue output response of the ACUT and the applied signal generated from ATPG. The schematic diagram of the TRC module, shown in Figure 6, is responsible for simulating the TRC scheme in the presented analogue testing. The generated signature from the TRC module can represent the analogue output response of the ACUT in the criteria of the ACUT judgment.

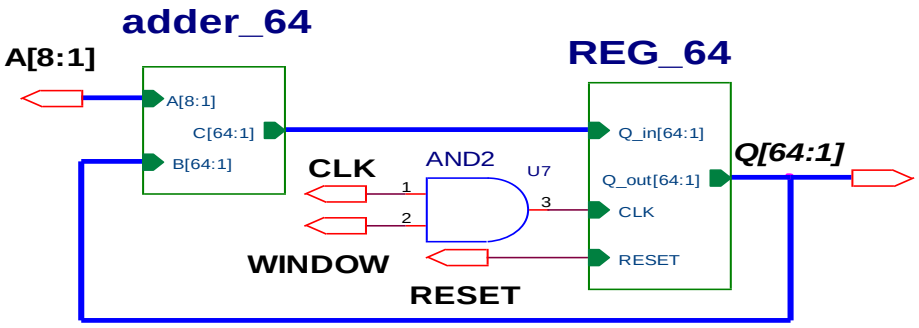

Fig. 6. Schematic diagram of the TRC stage.

The TRC module has two main modules; 64-bit adder, and 64-bit register. The 64-bit adder is represented by module, ADDER_64, and the 64-bit register is represented by module REG_64. The adder accepts sample outputs of the ADC (A[8:1]) and outputs of the REG_64 (Q[64:1]), and produces the sum of them. The input clock of the 64-bit register is the gated clock inside the test gate. After one clock shift, the sum Q[64:1] is generated. The test gate is controlled for proper signature generation. The control signal RESET is the signal that clears the REG_64 in the beginning of each test gate WINDOW. The TRC generates a digital signature after the test gate WINDOW is closed. Figure 7 illustrates the timing waveform cycle of the TRC stage. The control signals are the RESET, S/H, CLK, and WINDOW. In addition, the digital buses are A[8:1], Q[32:1], and Q[64:33]. The accumulation process of the TRC module is triggered by the RESET signal to execute a number of iterations equals to the

number of weighted samples. All control signals, presented in Figure 7, are properly asserted to generate a digital signature.

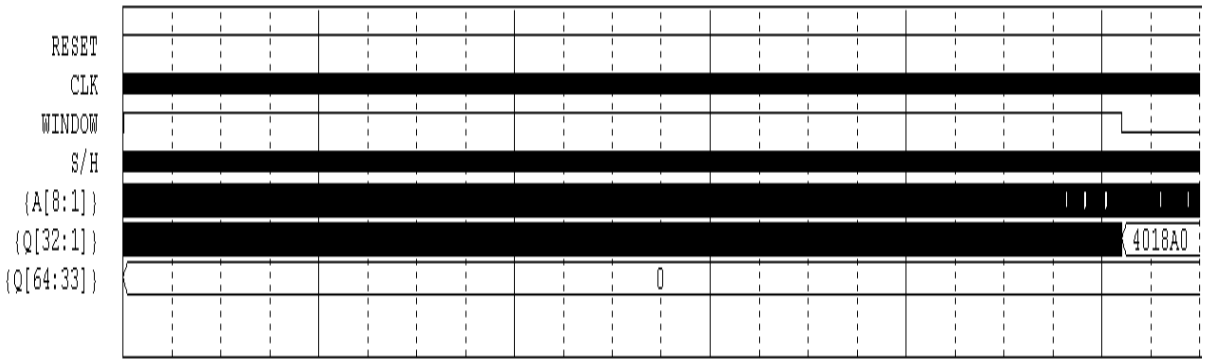

Fig. 7. Full Timing diagram of the circuit model of the analogue testing.

3. PSpice circuit model simulation of the ACUT

The modeling of ACUT transfer function is the main step to predict the output response of the ACUT. Analogue circuit differs by their characteristics and parameters that control its analogue response. These parameters have a great role in the process of predicting the fault-free output analogue response and accordingly improve the process of detecting different ACUT faults. The ACUT model selected from a group of standard analogue circuits called benchmark circuits [29]. Each benchmark circuit could be modeled through its transfer function in the frequency domain that requires a specified input sinusoidal signal swept in frequency.

The developed approach is verified and validated the decision for the ACUT in two major phases. The first phase is for a golden fault-free ACUT and the second phase is for predefined faults in the same ACUT. The presented testing approach determines each ACUT status in both cases based on the generated digital signature. The signature comparison is achieved based on the pre-calculated signature boundaries in the first phase. Signature boundaries are calculated from the analogue output response of the simulated ACUT model using the PSpice circuit simulator and based on the worst-case analysis of both the minimum and the maximum of the output analogue response of the ACUT. This boundary calculation considers the tolerances of ACUT components that affect the transfer function of the ACUT. If the calculated signature in the second phase lies within the pre-calculated signature boundaries, it judged as a fault-free ACUT, otherwise it judged as a faulty one.

One of the benchmark circuits as an ACUT is selected. It is low pass filter (LPF) in the frequency range of the biomedical circuits. The schematic diagram of the selected LPF is shown in Fig. 8. By a simple analysis, it is clarified that its transfer function (TF) and its transfer function coefficients are as follow:

$$TF = \frac{a}{s^3 + a_2 s^2 + a_1 s + a} \qquad (1)$$

where,

$$a = \frac{1}{C_1 C_2 C_3 R_1 R_2 R_3} \quad a1 = \frac{1}{C_2 C_3 R_2 R_3} + \frac{1}{C_1 C_2 R_2 R_3} + \frac{1}{C_1 C_2 R_1 R_3} + \frac{1}{C_1 C_2 R_1 R_2}, \quad a2 = \frac{1}{C_1 R_1} + \frac{1}{C_1 R_2} + \frac{1}{C_2 R_3} + \frac{1}{C_2 R_2}$$

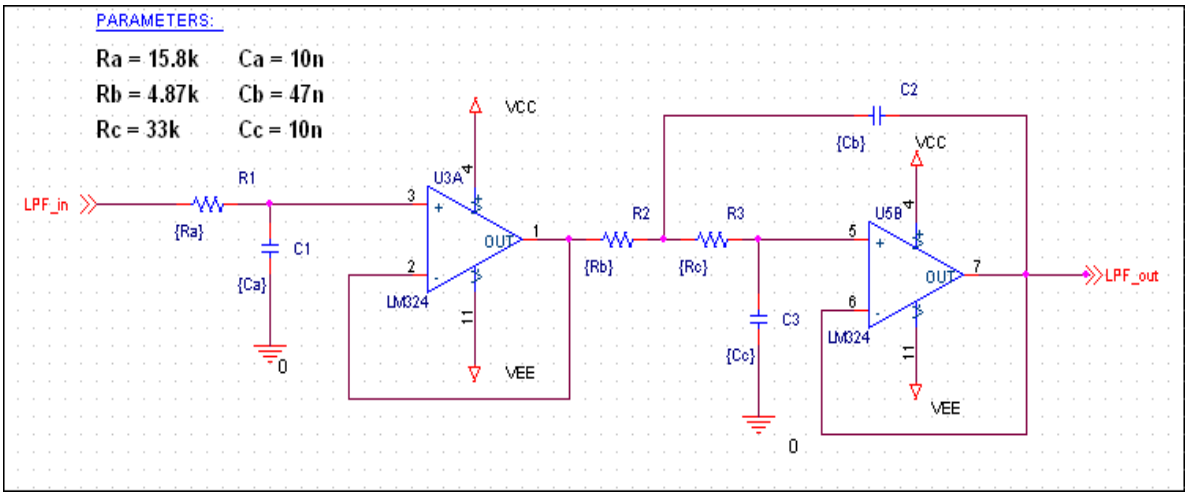

Fig. 8. Schematic diagram of the LPF.

The worst-case analysis is used to find the worst-case probable output of an analogue circuit, given the circuit description, and the restricted parameter tolerances. It is the upper or lowest possible collating function relative to the nominal run. PSpice circuit simulator allows tolerances to be set on any number of the parameters that characterize a model. Models can be defined for nearly all primitive analogue circuit components (resistors, capacitors, semiconductor devices, etc). PSpice reads the standard model parameter tolerance, and uses the nominal, minimum, and maximum probable values. For instance, if the values of *R1*, *R2*, *R3*, *C1*, *C2*, and *C3* in the case of LPF can vary by ±5%, ±10%, or ±20%, then the worst-case analysis will attempt to find the combination of possible resistor values and capacitor values which result in the worst simulated output. For the worst-case analysis, each component value is taken from its nominal as allowed by its tolerance, in the direction which should cause the collating function to be its worst (given by the upper or lowest specification). A summary of that analysis is illustrated in Table 2 that shows the percent change corresponding to each component. For example, *R1* equals 1.05 of nominal value for the lowest bound and equals 0.95 of nominal value for the upper bound. It indicates that resistor value increases (I) by +5% for the lower bound, and decreases (D) by -5% for the upper bound. In addition, Table 3 illustrates the signature boundaries in hexadecimal format, and the nominal and worst-case component values based on the worst-case analysis. For example, S_L equals 2C7DC3 for the lowest signature bound and S_U equals 32ED2B for the upper signature bound according to the listed component values and ±5% component tolerance in Table 3. In this case, the output signal frequency sweeps from 1.2 Hz to 1.5 kHz according to Figure 3.

Table 2. Component tolerances for the worst-case analysis of the LPF.

Comp.	**±5%**		**±10%**		**±20%**	
	LOWEST	***UPPER***	***LOWEST***	***UPPER***	***LOWEST***	***UPPER***
R1	1.05 (I)	0.95 (D)	1.1 (I)	0.9 (D)	1.2 (I)	0.8 (D)
R2	1.05 (I)	0.95 (D)	1.1 (I)	0.9 (D)	1.2 (I)	0.8 (D)
R3	1.05 (I)	0.95 (D)	1.1 (I)	0.9 (D)	1.2 (I)	0.8 (D)
C1	1.05 (I)	0.95 (D)	1.1 (I)	0.9 (D)	1.2 (I)	0.8 (D)
C2	0.95 (D)	1.05 (I)	0.9 (D)	1.1 (I)	0.8 (D)	1.2 (I)
C3	1.05 (I)	0.95 (D)	1.1 (I)	0.9 (D)	1.2 (I)	0.8 (D)

Table 3. Signature boundaries for the worst-case analysis of the LPF.

Comp.	*Nominal*	±5%		±10%		±20%	
		LOWEST	***UPPER***	***LOWEST***	***UPPER***	***LOWEST***	***UPPER***
R1(Ω)	15.8k	16.56k	15.14k	17.38k	14.22k	18.96k	12.64k
R2(Ω)	4.87k	5.1135k	4.6265k	5.357k	4.383k	5.844k	3.896k
R3(Ω)	33k	34.65k	31.35k	36.3k	29.7k	39.6k	26.4k
C1 (F)	10n	10.5n	9.5n	11n	9n	12n	8n
C2 (F)	47n	44.65n	49.35n	42.3n	51.7n	37.6n	56.4n
C3 (F)	10n	10.5n	9.5n	11n	9n	12n	8n
	Digital Signatures						
	S_N	S_L	S_U	S_L	S_U	S_L	S_U
	2F05DC	2C7DC3	32ED2B	29B52A	36DAA5	24FCA2	4018A0

4. Parametric fault analysis of the low pass filter based on the signature curve

In this section, the effect of the parametric fault of the component in the LPF (as an ACUT), illustrated in Figure 8 is presented. The parameter variations affected on the performance of the LPF is studied. The effects of all component variations in the LPF with respect to the passband transmission (A_{max}) and the cut-off frequency (F_c) as the parameters of its transfer function are taken in the consideration. According to the nominal values of resistors and capacitors presented in Figure 8 and the AC Analysis of the PSpice circuit simulator, the value of the F_c equals 521 Hz, and the A_{max} equals 0.999323044 V. (This filter can be used in the extraction circuit of muscle potentials of EMG waveform.)

In this section, component variations will sweep from very small value (or short circuit (SC) in the case of impedances), ±10%, ±20%, ±50% …, until very large value (or open circuit (OC) in the case of impedances). Therefore, the effect of component variations on the LPF output response is achieved, and consequently the relation between generated digital signatures with respect to component variations is required to be stated and analyzed. The derived curve is called the *signature curve*. The requirement of the signature curve combines the effect of the A_{max} and the F_c in one curve that illustrates the ACUT status. The analysis of the output response based on the amplitude response of the LPF is done using the PSpice circuit simulator (AC Analysis). The amplitude response of the LPF based on each resistor variation (*Ra*, *Rb*, *Rc*) and each capacitor variation (*Ca*, *Cb*, *Cc*) is presented. The resistor variation is achieved from 1Ω (SC) to 1MΩ (OC), and the capacitor variation is achieve from 1 *pF* (very small value) to 1 *mF* (very large value). The F_c values, the A_{max} values, and the corresponding digital signatures in the hexadecimal form and the decimal form with respect to each component variations of the LPF are illustrated in Table 4.

Table 4. Signatures, F_c, and A_{max} for each component variation of the LPF.

Component values			F_c	A_{max}	Signature (Hex.)	Signature (Dec.)	Component values			F_c	A_{max}	Signature (Hex.)	Signature (Dec.)
Ra (Ω)	1	short	592.431	1.000	35198B	3479680	*Ca* (pF)	1		592.431	1.000	35198B	3479947
	10		592.431	1.000	35170D	3479921		10		592.198	1.000	35170D	3479309
	100		592.427	1.000	35161F	3479217		100		591.504	1.000	35161F	3479071
	1000		592.059	1.000	3512F6	3477513		500		570.896	1.000	3512F6	3478262
	7900	50%	570.896	0.999	34FE9E	3341261		1000		542.665	0.999	34FE9E	3473054
	10000		559.254	0.999	32FD76	3276099		5000	50%	532.045	0.999	32FD76	3341686
	12640	20%	542.665	0.999	30A5FD	3187685		8000	20%	542.665	0.999	30A5FD	3188221
	14220	10%	532.045	0.999	2FD47A	3134805		9000	10%	532.045	0.999	2FD47A	3134586
	15010	5%	526.602	0.999	2F6F70	3108702		9500	5%	526.602	0.999	2F6F70	3108720
	15800	nom	521.091	0.999	2F05DC	3081692		10000	nom	521.091	0.999	2F05DC	3081692
	16590	5%	515.525	0.999	2EA114	3055602		10500	5%	515.525	0.999	2EA114	3055892
	17380	10%	509.917	0.999	2E39F3	3029090		11000	10%	509.917	0.999	2E39F3	3029491
	18960	20%	498.616	0.999	2D716F	2977858		12000	20%	498.617	0.999	2D716F	2978159
	23700	50%	464.608	0.999	2B3665	2831507		15000	50%	464.608	0.999	2B3665	2831973
	50000		302.893	0.999	149FA8	2236940		1E+05		100.719	0.999	149FA8	1351592
	1E+05		159.101	0.999	A1BD1	1672550		5E+09		20.150	0.998	A1BD1	662481
	1E+06	open	15.948	0.996	7C974	811046		1E+06		10.148	0.994	7C974	510324
								47E+06		1.428	0.209	49A1D	301597
								1E+09		1.412	0.010	491D0	299472
Rb (Ω)	1	short	407.696	0.999	2FA9E5	3123685	*Cb* (pF)	1		366.793	0.999	2D234F	2958159
	10		408.004	0.999	2FAEE7	3124967		10		366.822	0.999	2D23C8	2958280
	100		411.100	0.999	2FDE7D	3137149		100		367.113	0.999	2D2850	2959440
	1000		443.510	0.999	313777	3225463		500		368.415	0.999	2D5683	2971267
	2435	50%	492.602	0.999	31511F	3232031		1000		370.055	0.999	2ED1AD	3068333
	3896	20%	519.215	0.999	3017CD	3151821		23500	50%	456.565	0.999	2FB825	3127333
	4383	10%	521.458	0.999	2F8F81	3116929		37600	20%	504.416	0.999	2F7E1A	3112474
	4626	5%	521.564	0.999	2F4C4B	3099723		42300	10%	514.413	0.999	2F4661	3098209
	4870	nom	521.091	0.999	2F05DC	3081692		44650	5%	518.150	0.999	2F27B9	3090361
	5113	5%	520.115	0.999	2EC192	3064210		47000	nom	521.091	0.999	2F05DC	3081692
	5357	10%	518.698	0.999	2E81E6	3047910		49350	5%	523.289	0.999	2EE53D	3073341
	5844	20%	514.585	0.999	2DF444	3011652		51700	10%	524.807	0.999	2EBED2	3063506
	7305	50%	491.777	1.016	2C57CE	2906062		56400	20%	524.835	1.002	2E73E3	3044323
	10000		443.874	1.061	29AD2A	2731306		77700	50%	493.415	1.063	2D1ADC	2955996
	50000		211.011	1.191	13362A	1259050		1E+05		452.050	1.153	2BB767	2864999
	1E+05		146.638	1.102	A97CA	694218		1E+06		203.786	2.382	1AD092	1757330
	1E+06	open	17.914	0.997	88187	557447		5E+07		140.303	3.344	A079A	657306
								1E+08		12.811	23.262	79508	496904
								1E+09		4.066	19.651	5821E	2958159
Rc (Ω)	1	short	928.794	0.999	47531B	4674331	*Cc* (pF)	1		510.083	1.259	4949CF	4803023
	100		938.770	0.999	47531B	4674331		10		15289	1.424	4949CF	4803023
	1000		1047.835	0.999	479A9A	4692634		100		742.321	1.286	496BAC	4811692
	10000		1047.416	0.999	48EA30	4778544		1000		2014.37	1.233	4FC205	5227013
	16500	50%	814.535	1.003	3EADE6	4107750		5000	50%	863.093	1.198	4227EB	4335595
	26400	20%	611.919	0.999	33F669	3405417		8000	20%	628.282	1.037	3423B0	3417008
	29700	10%	563.360	0.999	3153FB	3232763		9000	10%	570.766	1.000	31A8E5	3254501
	31350	5%	541.523	0.999	2F2567	3089767		9500	5%	545.015	0.999	304D1A	3165466
	33000	nom	521.091	0.999	2F05DC	3081692		10000	nom	521.091	0.999	2F05DC	3081692
	34650	5%	501.926	0.999	2DF953	3012947		10500	5%	498.810	0.999	2DD70E	3004174
	36300	10%	483.912	0.999	2CFAE1	2947809		11000	10%	478.017	0.999	2CCB9E	2935710
	39600	20%	450.947	0.999	2B271C	2828060		12000	20%	440.375	0.999	2AB7D8	2799576
	49500	50%	371.365	0.999	26AFF8	2535416		15000	50%	352.105	0.999	25E542	2483522
	50000		367.968	0.999	268169	2523497		1E+05		44.187	0.999	E036E	918382
	1E+05		182.256	0.997	1AFC4D	1768525		5E+05		8.591	0.999	74FBB	479163
	5E+06		89.230	0.844	C7A75	817781		1E+06		4.445	0.992	5FDD6	392662
	1E+06	open	16.230	0.999	9EE7B	650875		1E+08		1.415	0.972	494CF	300239
								1E+09		1.412	0.089	491D0	299472

Discussion and comments

Figure 9 illustrates the signatures with respect to *Ra*, *Rb*, and *Rc* variations, called the *signature curve of Ra*, *Rb*, and *Rc*, and Figure 10 illustrates the signatures with respect to *Ca*, *Cb*, and *Cc* variations, called the *signature curve of Ca*, *Cb*, and *Cc*. From Table 4, Figure 9, and Figure 10, we can conclude the following comments. During *Ra*, *Rb*, and *Rc* variations, the variation of A_{max} is nearly unity gain. The signature curves of *Ra*, *Rb*, and *Rc* clearly have the same corresponding variations of F_c**.** In these cases, the signature curves are affected with the F_c, while it is not affected with the A_{max}.

During *Ca* variation from 1 μF to 1 *mF*, the variation of A_{max} is largely decreasing and has unity gain from 1 *pF* to 1 μF**.** In addition, the signature curve of *Ca* clearly has the same

variation of F_c where the signature variation is slightly small from the 1 *pF* to 1 *μF*, and largely decreasing from 1 *μF* to 1 *mF***.** In this case, the signature curve, illustrated in Figure 10, is affected with the F_c, while it is not affected with the A_{max}. When the value of F_c is large, the bandwidth of the LPF is also large, and consequently the number of generated samples and their accumulation are large.

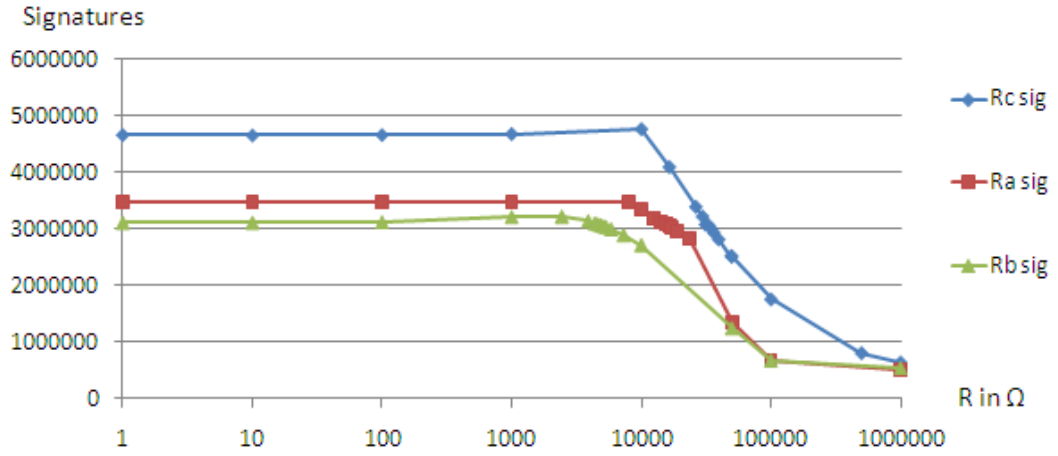

Fig. 9. Signature curves of all resistors in LPF.

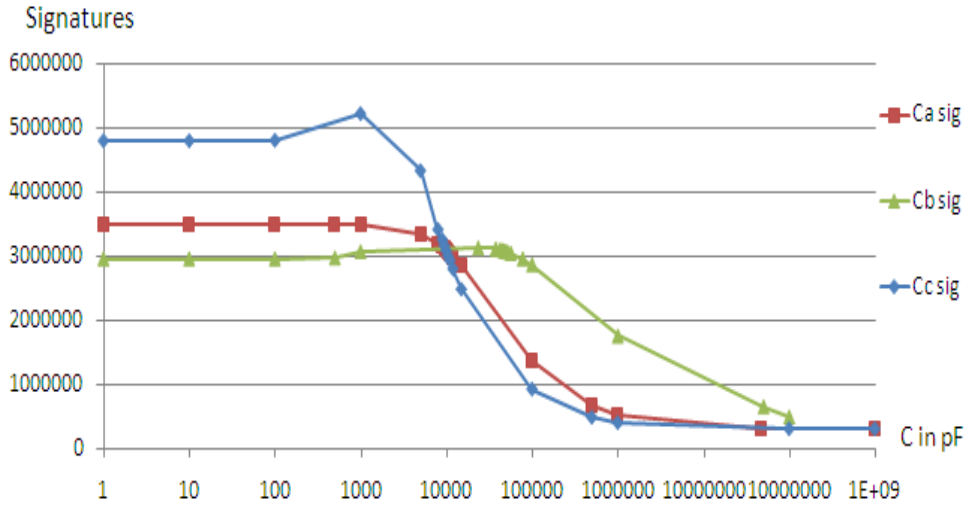

Fig. 10. Signature curves of all capacitors in LPF.

During *Cb* variation from 1 *μF* to 1 *mF*, the variation of A_{max} is largely increasing and has no change from 1 *pF* to 1 *μF***.** The signature curve nearly has the same variation of F_c where the signature variation is slightly small from the 1 *pF* to 100 *nF*, and largely decreasing from 100 *nF* to 1 *mF***.** During *Cb* variation from 1 *pF* to 100 *nF*, the variation of A_{max} is nearly unity gain. Therefore, the signatures are affected by the F_c. When the values of F_c are large with unity gain of the A_{max}, the number of generated samples and their accumulation are large, illustrated in Figure 10. During *Cb* variation from 100 *nF* to 1 *μF*, the variation of A_{max} is slowly increasing, and in the same time the variation of F_c is largely decreasing. Therefore, the signature variation is largely decreasing. During *Cb* variation from 1 *μF* to 0.1 *mF*, the variation of A_{max} is largely increasing, and in the same time the variation of F_c is gradually decreasing. Therefore, the signature variation is gradually decreasing, illustrated in Fig. 10. During *Cb* variation from 0.1 *mF* to 1 *mF*, the variation of A_{max} is largely decreasing, and in the same time the variation in F_c is slowly decreasing. Therefore, the signature variation is slowly decreasing. Finally, the signature curve of *Cb* is affected with the F_c, while it is not affected with the A_{max}.

The amplitude response of the LPF based on the capacitance *C3* (*Cc*) variation from 1 *pF* to 1 *mF* and through the nominal value of *Cc* (10 *nF*) is illustrated in Figure 11. The relation of the F_c and the A_{max} with respect to the *Cc* variation is presented in Table 4. During *Cc* variation from 1 *pF* to 1 *mF*, the variation of A_{max} is small above the unity gain and nearly has unity gain for all values except for *Cc* = 1 *mF*, the A_{max}= 0.089 V/V. The signature curve will be affected with the variation of F_c. During *Cc* variation, the variation of F_c is increasing from 1 *pF* to 10 *pF*, then is decreasing from 10 *pF* to 100 *pF* and then is increasing from 100 *pF* to 1 *nF*. But, the signature variation in the signature curve is nearly constant during *Cc* variation from 1 *pF* to 100 *pF*. The reason is that the output signal frequency sweeps from 1.2 Hz to 1.5 kHz according to Figure 3. Therefore, the output response of the LPF is not affected by presented overshoot after cut-off frequency 1.5 kHz during *Cc* variation from 1 *pF* to 100 *pF*. During *Cc* variation from 100 *pF* to 1 *nF*, the variation of F_c is largely increasing. Therefore, the signature variation is increasing, illustrated in Figure 10. During *Cc* variation from 1 *nF* to 0.1 *μF*, the variation of F_c is largely decreasing. Therefore, the signature variation is decreasing. During *Cc* variation from 0.1 *μF* to 1 *mF*, the variation of F_c is tiny decreasing. Therefore, the signature variation is slowly decreasing.

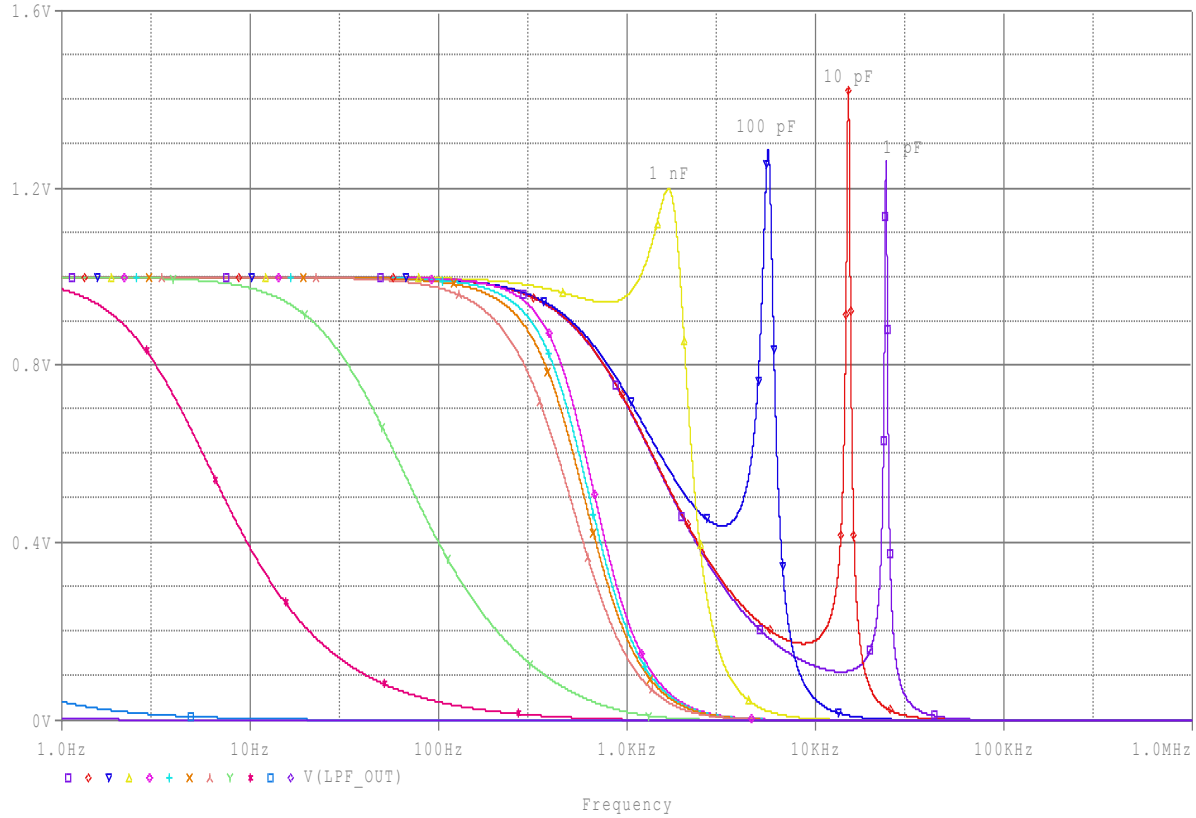

Fig. 11. Amplitude response of the LPF based on *Cc* variations.

5. The implementation of the presented analogue testing approach

Direct hardware mapping of the analogue testing approach needs some modifications to obtain the practical hardware realization. This section presents the practical design and implementation of the presented digital testing of analogue circuits to detect parametric faults. The main testing block diagram and its implementation architecture are illustrated in Figure 12. This testing architecture has two main parts. The first part is the FPGA digital part, and the second one is the analogue part including the DAC, the analog conditioning, the full wave rectifier, and the ADC.

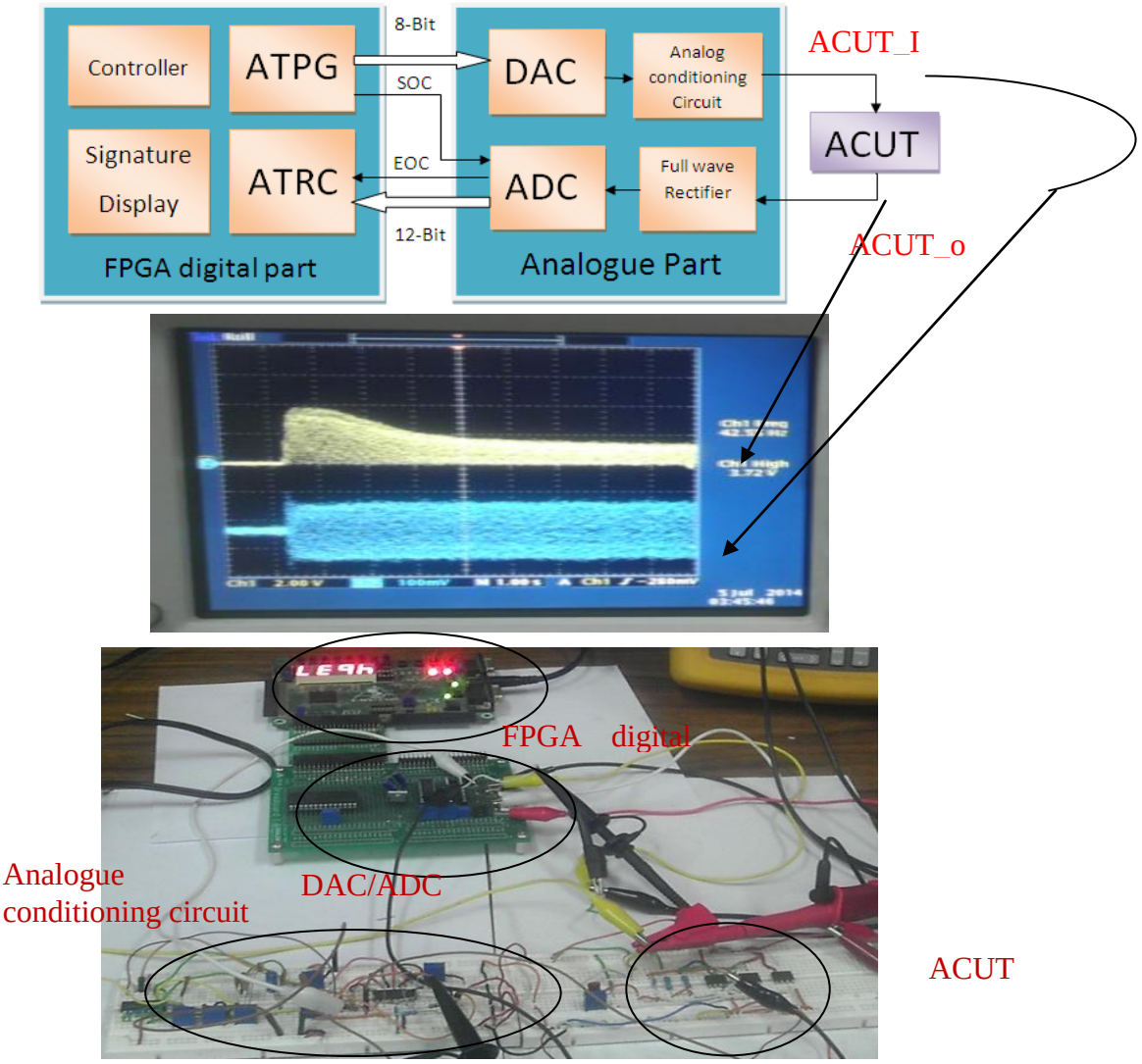

Fig. 12. Main block diagram of the presented analogue testing architecture.

The concept of the design is to use an economical FPGA chip (Spartan3-200kgate) as the digital part to generate and receive required digital signals of the presented testing architecture. The ATPG of the FPGA digital part generates the required digital samples of the sinusoidal signal. By using variable clock period to those samples, the complete sinusoidal cycle are properly generated and swept in the required frequency domain. These samples are applied to the DAC and the analogue conditioning circuit in the analogue part to produce the required analogue test signal for ACUT. This analogue signal is considered the stimulus of the ACUT, and the sweep in the frequency is properly selected to match the frequency domain of the ACUT and to stimulate the faults of the ACUT.

The output of the ACUT that is the most sensitive to the input test signal is applied to the full wave rectifier with the DC bias adjustment to make the analogue output signal of the ACUT above the zero volt. After that the rectified analogue signal is converted into digital samples during the reading process by the ADC. The ADC represents the analog part of the ATRC, and receives the start of the conversion (SOC) control signal from the FPGA digital part. After digital samples are ready to send to the FPGA digital part, the ADC generates the end of conversion (EOC) control signal to the FPGA digital part. Digital samples, generated from the ADC, are accumulated by the ATRC in the FPGA digital part, and the result of that accumulation process is divided by the number of the extracted samples during the test window to produce the quotient and the residue. The residue is ignored and the quotient is considered as a digital signature for the analogue waveform of the ACUT. The controller

controls the proper timing of the analogue test cycle. During the generation of the test window, analogue test generation, the sample extraction, and signature generation are properly synchronized to provide the stability of the generated quotient (digital signature) and correctly make the ACUT judgment. The accumulation process is synchronously executed sample by sample during the testing cycle process.

The presented testing approach introduces the concept of the signature curve generation for each component of the LPF. Based on this curve, the relation between the digital signatures and the component variations of the LPF is presented. In this section, the practical implementation of the analogue testing is focused on the detection of parametric faults in the ACUT, and the signature curve of each components of the ACUT is deduced from the real hardware system. The schematic diagram of the FPGA digital part will be shown in Figure 13. It consists of three sections: (1) *control* section for timing control and synchronization, (2) *analogue test pattern generator* section, and (3) *analogue test response compactor* section for sample accumulation and signature generation.

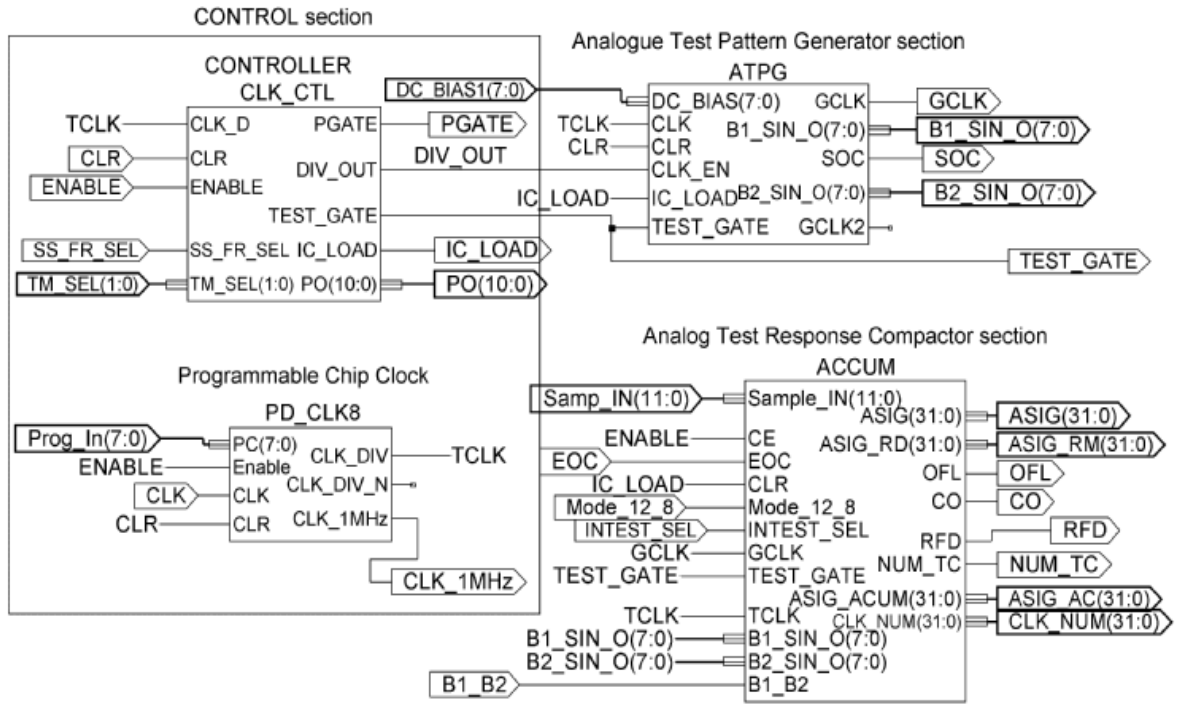

Fig. 13. The schematic diagram of the FPGA digital part of the testing approach.

The control section in Figure 13 has two modules; *CLK_CTL*, and *PD_CLK8*. The module *CLK_CTL* is used to generate all required control signals for proper analogue test cycle. The objective of the control section is to control the full test gate that the frequency sweeps. Figure 14 shows the main control signals of the FPGA design of the *complete analog test cycle*. The module *PD_CLK8* is the programmable test clock. The main control signals, generated from the control section, control both the *analogue test pattern generator* section and the *Analogue Test Response Compactor* section. The control section performs several control operations. It controls the gate and sub-gate generation, the test gate selection, the enable of the test cycle, and the selection of the single-shot or free-running of the test window cycle. It generates all test windows required to generate the full analogue test cycle and for the test sub-gate of the sweep frequency of the ATPG. It generates the following control signals; *TEST_GATE*, *IC_LOAD*, and *PGATE*. Control signal, *TEST_GATE*, is the test window to enable the analogue test cycle. It is asserted at the falling edge of clock, *CLK_D*, at the start and the end of the analogue test cycle. Control signal, *IC_LOAD*, is used once at the start of the analogue test cycle to set all memory cells to initial state. Control signal, *PGATE*, is used as clock-

enable (CE) for clock *CLK_D* of the programmable counter. The programmable clock that changes the frequency during the frequency sweep is properly design and implemented. The control signal *PGATE* is used to generate the frequency frame pulse for each sub-gate window that enables the *CLK_D* to increment programmable counter in module *CLK_CTL*. The *PGATE* is considered the start of each frequency frame during the frequency sweep in the test window. The value of the bus *PO*(10:0) is called frequency frame number. *PO*(10:0) is used to assign the programmable code for *DIV_OUT* that is the output control signal to enable the clock of the ATPG module. In the frequency frame number (001h), the period of *DIV_OUT* is 20 µs. Figure 14 illustrates the last frequency frame number (768h) during the test gate whose corresponding period 18960 µs.

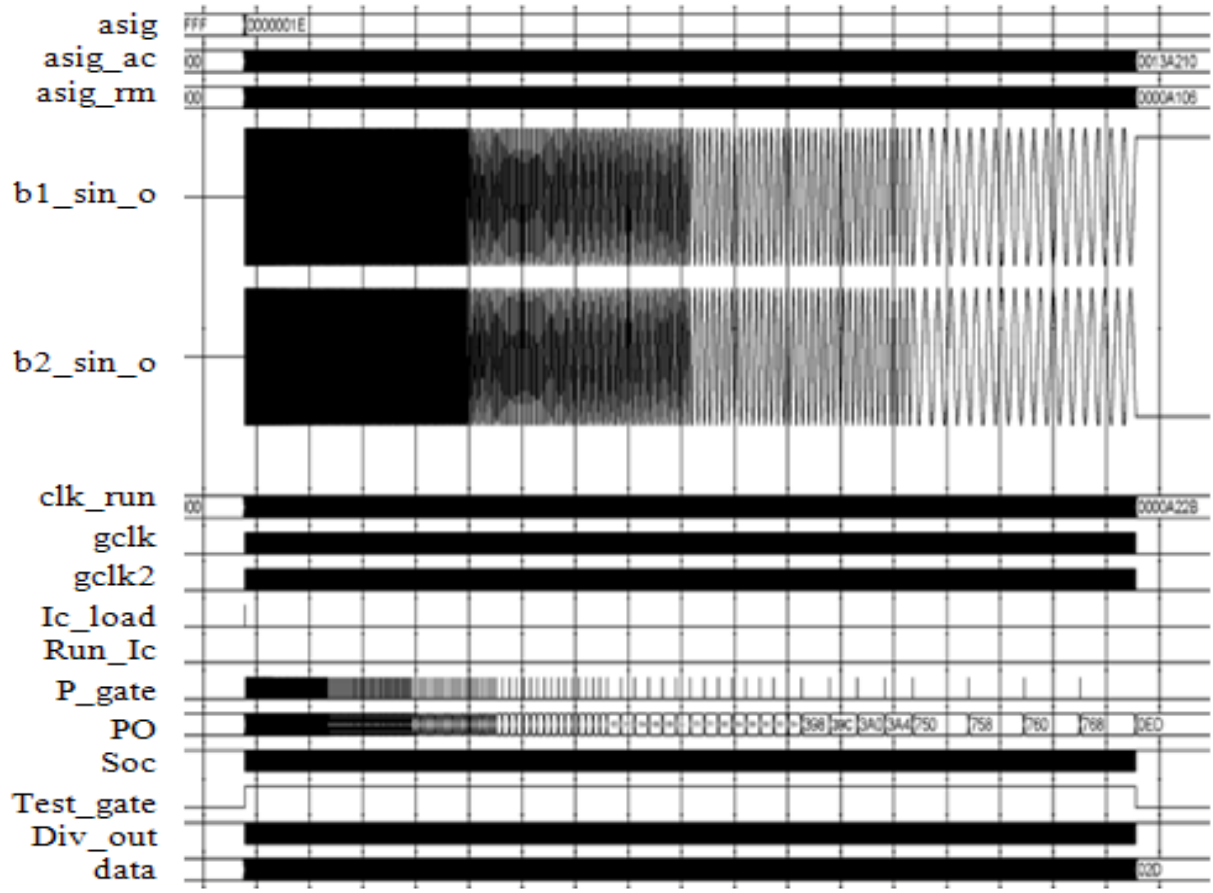

Fig. 14. Timing diagram of main control signals of the FPGA design of the *complete test cycle*.

The second module, *PD_CLK8*, of the control section is the programmable test clock of the internal board clock (50 MHz). This cell divides the clock board *CLK* into another clock *CLK_1MHz* of the required testing operation, 1 MHz, and then from clock *CLK_1MHz* to clock *CLK_DIV* (clock *TCK* in Figure 13). This module receives the following signals; *CLK*, *CLR*, *Enable*, and *PC*(7:0). Control signal *Enable* enables this module to active high during the testing operation. Control bus *PC*(7:0) is used to generate the required clock, *CLK_DIV*. Table 5 illustrates the setting of the *PC*(7:0) and the corresponding frequency values of the *CLK_DIV* of the module *PD_CLK8*. For example, when the period of the *CLK_DIV* is 10 µs for frequency 100 kHz, the *PC*(7:0) is set to "11110110".

The *analog test pattern generator* section has one main block *ATPG*, illustrated in Figure 13, to generate the sinusoidal waveform swept in frequency. The *ATPG* consists of SINE generator core, and 8-bit binary counter. Module ATPG accepts the control signals; *CLK_EN*, *CLK*, *TEST_GATE*, *DC_BIAS*, *IC_LOAD*, and *CLR*, and produces sample outputs (SINE

B1_SIN_O(7:0)), and the start of the conversion (*SOC*). In addition, the gated clock *GCLK* is applied to the *analogue test response compactor*, discussed later. The SINE core that computes sin(θ) accepts an unsigned input value *THETA*(5:0) from the 8-bit binary counter cell. The output sample values of the full wave 360-degree output sine wave, expressed as fractional fixed-point. The use of properly selected bit-widths can provide high quality and efficiently utilize the available hardware overhead area. In this design, the width of the *THETA* input and the width of the SINE output are 6-bit; therefore, the complete cycle of the sinusoidal signal consumes 64 samples. The SINE output samples is converted to signal bus *B1_SIN_O*(7:0) to add the DC component *DC_BIAS*(7:0) to produce *B1_SIN_O*(7:0).

Table 5. Generated clock frequency from module *PD_CLK8*.

PC(7:0)	*CLK_DIV*		*PC*(7:0)	*CLK_DIV*	
	Period	Frequency		Period	Frequency
"11111110"	2 µs	500 kHz	"10011100"	100 µs	10 kHz
"11111101"	3 µs	333.3 kHz	:	:	:
"11111100"	4 µs	250 kHz	"01111111"	129 µs	7.75 kHz
"11111011"	5 µs	200 kHz	"01111110"	130 µs	7.69 kHz
:	:	:	:	:	:
"11110110"	10 µs	100 kHz	"00110000"	208 µs	4.8 kHz
"11110101"	11 µs	90.9 kHz	:	:	:
:	:	:	"00001000"	248 µs	4 kHz
"11101100"	20 µs	50 kHz	:	:	:
:	:	:	"00000001"	255 µs	3.92 kHz
"11011000"	40 µs	25 kHz	"00000000"	256 µs	3.9 kHz

Control signals, generated from the *CONTROL* section, generates the following control signals; *DIV_OUT*, *TEST_GATE*, *IC_LOAD*, *PGATE*, and *TCLK*. Control signal, *DIV_OUT*, is applied to drive the input signal *CLK_EN* for module *ATPG*. It is used as enable of the clock of 8-bit binary counter. This counter is asserted at the rising edge trigger of *TCLK* and the control signal, *DIV_OUT*, is asserted at the falling edge trigger of *TCLK*. The programmable period of the control signal, *DIV_OUT*, is changed during the frequency frame of the sub-gate in the test window. All control signals, *DIV_OUT*, *TEST_GATE*, *CLK*, are applied to the AND operation to produce the gated clock, *GCLK*. The *GCLK* is inverted to produce the control signal, *SOC*. The *SOC*, applied to the ADC outside the FPGA chip, is used to start the conversion from analogue to digital for each sample. Signal bus, *B2_SIN_O*(7:0), generated from the module *ATPG*, is another sinusoidal generator swept in the frequency with the phase shift 180-degree with clock *GCLK2*.

In the first frequency frame and in all testing modes of analog testing operation, the period of the sinusoidal waveform equals 640 µs (64 samples per single frequency cycle × 10 µs). Therefore, the highest frequency will be 1.5625 kHz. The choice of the minimum sample period (T_{s_min}) is 10 µs because the time of conversion of the used ADC of the presented design (t_{conv}) is 10 µs. This presented design is capable to work with higher-speed sinusoidal waveform when the time of conversion of the ADC is reduced. In addition, the use of lower bit-widths can assist in this issue. The implementing of the ATPG to produce high-resolution samples with good resemblance to the characteristics of the sinusoidal signal is required. Signal buses *ASIG*, *ASIG_AC*, and *ASIG_RM* in Figure 14 will be discussed next.

The *analogue test response compactor* (ATRC) section has one module *ACCUM*. In analogue circuits, the ATRC function is design to generate a digital signature based on accumulation weighting sums of the sample magnitude of the analogue output response. These samples are generated from the ADC, and the required digital signature is generated from ATRC by accumulating those samples. These samples are based on the analogue output response of the

LPF and the applied signal generated from the ATPG. The main block diagram of the ATRC, illustrated in Figure 15, is the analogue compaction scheme. According to Figure 14, the accumulator accepts sample inputs by sample acquisition unit and the outputs of the register, to produce the sum of them. The sample inputs are processed every clock cycle during the test window to generate a digital signature (S_t). Another way to generate a digital signature is to divide S_t by the number of those samples (N) to produce the quotient (Q_t) that is considered the digital signature. The *controller* section administers the compaction process to execute a number of iterations equals to the analogue output samples, N. The generated digital signature is a measure for the LPF validity for fault-free operation. The presented digital signature in this paper is considered the criteria in the LPF as the ACUT judgment.

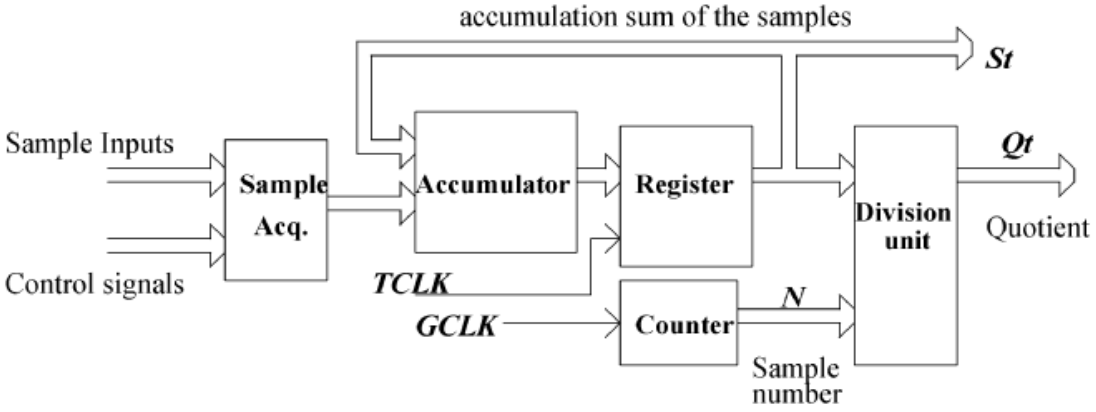

Fig. 15. Main Block diagram of the *ATRC*.

The module *ACCUM* in Figure 13 receives the input control signals; *Sample_IN(11:0)*, *INTEST_SEL*, *CE*, *GCLK*, *CLR*, *EOC*, *Mode_12_8*, *TCLK*, and *TEST_GATE*. Control signal *INTEST_SEL* is used to enable the sample accumulation either from the ADC or from the generated samples of the ATPG in the build-in self-test (BIST) mode. Control signal, *CE*, enables the operation of the ATRC. Clock *GCLK* is used to control the throughput of the samples into the 32-bit accumulator in the BIST mode, and to count the number of the samples during the analogue test window in the module *ASIG_DIV*, illustrated in Figure 14. The sample inputs, *Sample_IN(11:0)*, is applied to the module, *ACCUM*. The width of the samples generated from the ADC is 12-bit (AD1674 - 100 kSPS). The control signal *Mode_12_8* is used to enable the sample accumulation either in 12-bit format or 8-bit format. The latched sample is asserted either at the falling edge trigger of the control signal *EOC* (end of conversion) from the ADC or at the falling edge trigger of the clock *GCLK* in the BIST mode. The output bus, *ASIG_ACUM*(31:0) at the end of the test gate window is considered the accumulation sum of the samples, S_t. This bus is applied as divisor of the division operation to the division module, *ASIG_DIV*. The clock, *GCLK*, is used to count the number of the samples using 16-bit binary counter. The *CLK_NUM*(31:0) is the number of samples, *N*, and is used as dividend of the division operation. This division operation produces the quotient, *ASIG*(31:0), considered a digital signature, and ignores the remainder, *ASIG_RM*(31:0).

Table 6. Generated sinusoidal frequencies according to the *TCLK* and *Testing mode* selection.

TCLK Selection	Testing mode *TM_SEL*(1:0)	Starting Frequency	Ending Frequency
TCLK = 100 kHz	Mode 0 "00"	1.5625 kHz	23.67 Hz
	Mode 1 "01"		5.95 Hz
	Mode 2 "10"		3.77 Hz
	Mode 3 "11"		0.824 Hz
TCLK = 50 kHz	Mode 0 "00"	781.25Hz	11.835 Hz
	Mode 1 "01"		2.975 Hz
	Mode 2 "10"		1.885 Hz
	Mode 3 "11"		0.412 Hz
TCLK = 25 kHz	Mode 0 "00"	٣٩٠.625 Hz	5.9175 Hz
	Mode 1 "01"		1.4875Hz
	Mode 2 "10"		0.9425Hz
	Mode 3 "11"		0.206 Hz
TCLK = 10 kHz	Mode 0 "00"	156.25 Hz	2.367 Hz
	Mode 1 "01"		0.595 Hz
	Mode 2 "10"		0.377 Hz
	Mode 3 "11"		0.0824 Hz

All modules of the FPGA digital part are connected and the timing simulation of the complete design is achieved to verify the proper operation of the chip design before the implementation on the FPGA chip (Xilinx - X3S200FT256-4). Table 6 illustrates the generated sinusoidal frequencies from the *analog test pattern generator* section in the sweep frequency according to the *TCLK* and *testing mode* selection. These ranges of sinusoidal frequencies are suitable for the analogue circuits of biomedical applications. The device utilization summary report generated due to this implementation is presented in Table 7.

Table 7. Device Utilization Summary of the Spartan-3 FPGA.

Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	2,999	3,840	78%
Number of 4 input LUTs	1,545	3,840	40%
Logic Distribution			
Number of occupied Slices	1,795	1,920	93%
Number of Slices containing only related logic	1,795	1,795	100%
Number of Slices containing unrelated logic	0	1,795	0%
Total Number of 4 input LUTs	1,585	3,840	41%
Number used as logic	1,545		
Number used as a route-thru	40		
Number of bonded IOBs	60	173	34%
Number of Block RAMs	2	12	16%
Number of GCLKs	3	8	37%
Number of RPM macros	88		
Total equivalent gate count for design	171,311		

6. Experimental Results

In this section, the effect of the parametric fault of the component in the LPF as the ACUT, illustrated in Figure 8, will be explored. In section 4, the relation between the generated digital signatures with respect to component variations of the ACUT, called the signature curve based on the simulation environment, was presented. This curve combines the effect of the A_{max} and the *BW* of the LPF in one curve to illustrate the ACUT judgment. In this section, the measured signature curve is generated, based on the presented testing hardware implementation. A measured signature mainly depends on the LPF component values in

addition to the applied ATPG. Due to the variation of the surrounding environment and the tolerance in the ACUT components itself, this signature may vary within bounded limits. For multi-test sessions, the signature may differ each time but within a certain predicted boundaries. Table 8 illustrates the measured signature boundaries for the worst-case analysis of the LPF. In Table 8, two way approaches to generate the measured digital signature are presented. The analogue compaction scheme in the practical ACUT is based on either the accumulation sum of the sample values (S_t), or the quotient (Q_t) of the dividing S_t by the number of those samples (N). If a measured signature lies within the signature boundaries, it judged as a fault-free ACUT, otherwise it judged as a faulty one based on predefined hard faults in the LPF. Contrary to that of the signature of the digital CUT, it is a unique signature for all identical test sessions, and the signature is the residue of the dividing of the polynomial representing the bit stream of the test output response of the digital CUT by the primitive polynomial of the linear feedback shift register (LFSR) [1].

The effect of hard faults in the filter performance is fully studied by component variations (one at a time) in the LPF. The measured signatures of component variations, including ±10%, ±20%, very low value and very high value are recorded, and then the measure signature curve for every component variation is plotted. The resistor variations are achieved from 1Ω (SC) to 10MΩ (OC), and the capacitor variation is achieve from 1 pF (very small value) to 1 mF (very large value). Figures 16 through 19 illustrate the measured signature curve for all resistors and capacitors of the LPF. In this paper, there are two different signature curves; derived from the accumulation sum and derived from the quotient. In the measured signature curve, the recorded number in the hexadecimal format is converted to decimal format to be plotted. The comparison between the normalized signature curve derived from PSpice circuit simulator in section 4 and the normalized measured signature curve presented in this section (S_t) is presented in Table 9 for each resistor variation and in Table 10 for each capacitor variation. The sweep sinusoidal frequency of the ATPG in the simulation environment is different from the presented in section. Therefore, small deviations of the normalized values in both Table 9 and Table 10 are presented. However, the measured signature curve for each component variation of the LPF was practically achieved the same behavior of the signature curve derived in the model version of the simulation environment.

Table 8. Measured signature boundaries for the worst-case analysis of the LPF.

ACUT components	***Nominal***	**±5%**		**±10%**		**±20%**	
		LOWEST	***UPPER***	***LOWEST***	***UPPER***	***LOWEST***	***UPPER***
R1 (Ω)	15.8k	16.56k	15.14k	17.38k	14.22k	18.96k	12.64k
R2 (Ω)	4.87k	5.1135k	4.6265k	5.357k	4.383k	5.844k	3.896k
R3 (Ω)	33k	34.65k	31.35k	36.3k	29.7k	39.6k	26.4k
C1 (F)	10n	10.5n	9.5n	11n	9n	12n	8n
C2 (F)	47n	44.65n	49.35n	42.3n	51.7n	37.6n	56.4n
C3 (F)	10n	10.5n	9.5n	11n	9n	12n	8n
	Digital Signatures						
		S_L	S_U	S_L	S_U	S_L	S_U
S_t		14AEA74	١٦٣٦٩٧٥	132C861	16ABDC9	11FA1E7	18FCDB3
Q_t		2ED	2F7	2E3	2FA	1F2	318

7. Conclusion

This paper presented the new testing approach of analogue circuits for detecting parametric faults based on the signature analysis. The proper ATPG that matches the frequency domain of the ACUT and the ATRC that generates a digital signature are presented. The ATPG generates the required stimulation for the ACUT (the LPF in this paper) in the frequency sweep manner. Control signals are used to synchronize the ATPG and ATRC for digital signature generation based on accumulation weighting sums of the sample magnitude of the

analogue output response. The signature comparison is achieved based on signature boundaries, calculated from the worst-case analysis in PSpice circuit simulator for the ACUT judgment. In this paper, the presented testing approach enables the concept of the signature curve for each component of the ACUT. Based on this curve, the relation between digital signatures and component variations of the ACUT combines the effects of the band-width (*BW*) and the passband transmission (A_{max}) on the output response of the ACUT during component variations. The proper decision is taken based on the frequency swept manner of the input signal contrary to the previously published work that states that the suitable input signal type for the ACUT was the pulse waveform. In addition, the presented test controller enables the proper synchronizing of the analogue test cycle. The synchronization between the ATPG, and the ATRC is achieved in both the digital part or analogue part of the implemented testing approach. The digital part implementation is based on the FPGA implementation using the economical chip (Spartan3-200kgate), selected to efficiently perform required functions and suitable capacity to fit the design. Finally, the proposed test strategy in this paper guides us to produce the stand-alone portable ATE for parametric fault detection of analogue circuits based on the FPGA technology.

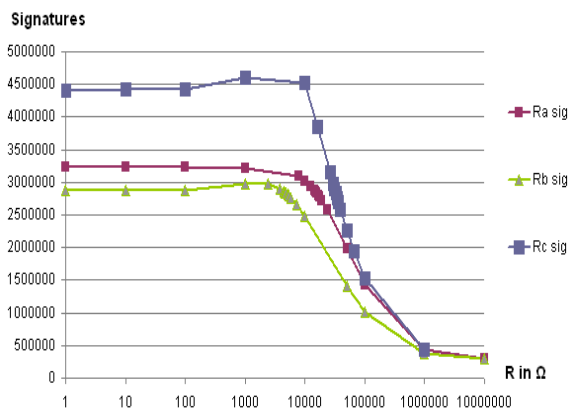

Fig. 16. Measured signature curve of all resistors based on accumulation sum.

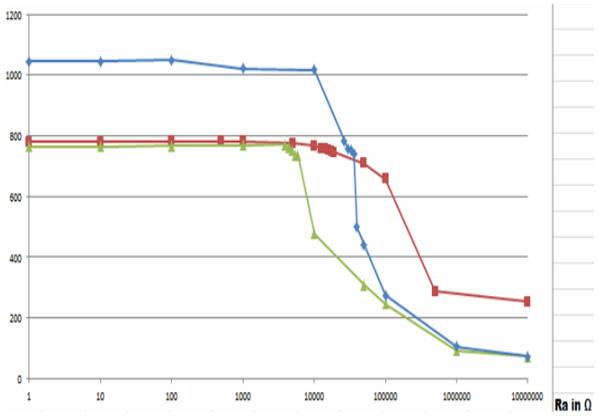

Fig. 17. Measured signature curve of all resistors based on the quotient.

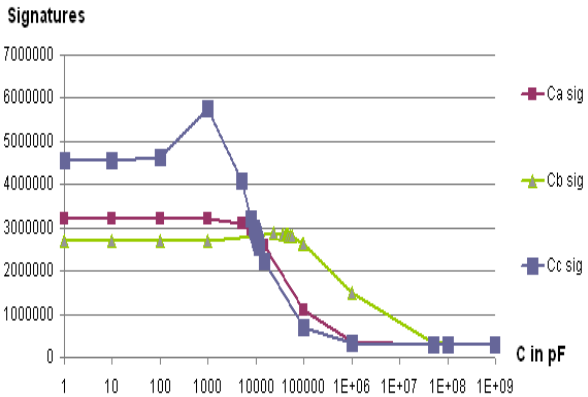

Fig. 18. Measured signature curve of all capacitors based on accumulation sum.

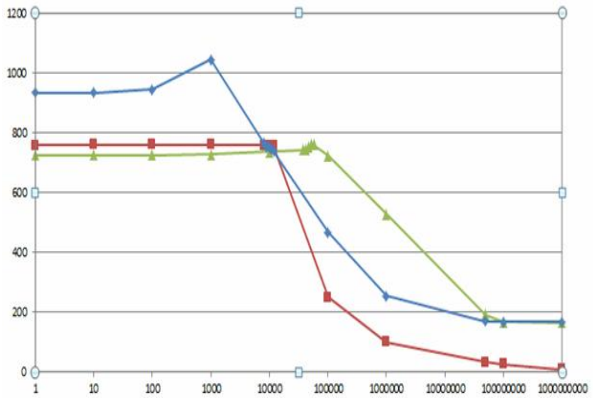

Fig. 19. Measured signature curve of all capacitors based on the quotient.

Table 9. Measured signatures for each resistor and each capacitor variations of the LPF.

Component values			Based on the Simulation		Based on the Hardware		Component values			Based on the Simulation		Based on the Hardware	
			Sig. (Dec.)	Sig. (Nor.)	Sig. (Dec.)	Sig. (Nor.)				Sig. (Dec.)	Sig. (Nor.)	Sig. (Dec.)	Sig. (Nor.)
Ra (Ω)	1	short	3225911	1	23289277	0.995073656	*Ca* (pF)	1	open	3479947	1	23635567	0.994319
	10		3225662	0.999923	23295196	0.995326555		10		3479309	0.999816664	23678102	0.996109
	100		3225598	0.999903	23362681	0.998209965		100		3479071	0.999748272	23707024	0.997326
	1000		3223324	0.999198	23404576	1		1000		3473054	0.998019223	23741814	0.998789
	10000		3022613	0.93698	22832018	0.975536493		8000	-20%	3188221	0.916169413	23770597	1
	12640	-20%	2935062	0.90984	22658709	0.968131574		9000	-10%	3134586	0.900756822	23171033	0.974777
	14220	-10%	2881857	0.893347	22598129	0.965543191		10000	NOM	3081692	0.885557165	22948009	0.965395
	15800	NOM	2828751	0.876884	22482719	0.960612104		11000	+10%	3029491	0.870556649	22773580	0.958057
	17380	+10%	2776546	0.860701	22261136	0.951144597		12000	+20%	2978159	0.85580585	22646257	0.9527
	18960	+20%	2725156	0.844771	22207214	0.948840688		1E+05		1351592	0.388394421	22442954	0.944148
	50000		1986663	0.615846	18500959	0.79048469		1E+06		662481	0.190371003	10350952	0.435452
	100000		1425240	0.44181	9871451	0.4217744		5E+07		510324	0.146647061	7359306	0.309597
	500000		439483	0.136235	5378991	0.229826466		1E+08		301597	0.086667125	5315567	0.223619
	1000000	open	303754	0.094161	5257818	0.224649146		1E+09	short	299472	0.086056483	5247265	0.220746
Rb (Ω)	1	short	3123685	0.96844546	22240701	0.981551994	*Cb* (pF)	1	open	2958159	0.950420469	22469252	0.974184
	10		3124967	0.968842923	22246620	0.981813218		10		2958280	0.950459345	22473419	0.974364
	100		3137149	0.972619745	22314105	0.984791543		100		2959440	0.950832039	22483243	0.97479
	1000		3225463	1	22356000	0.986640501		1000		3068333	0.985818034	22541966	0.977336
	3896	-20%	3151821	0.977168549	22504338	0.993187123		10000		3108634	0.998766255	22814021	0.989132
	4383	-10%	3116929	0.966350877	22658709	1		37600	-20%	3112474	1	23056143	0.999629
	4870	NOM	3081692	0.955426244	22598129	0.997326414		42300	-10%	3098209	0.995416829	23064694	1
	5357	+10%	3047910	0.944952709	22482719	0.992233009		47000	NOM	3081692	0.990110118	23051669	0.999435
	5844	+20%	3011652	0.933711532	22261136	0.982453855		51700	+10%	3063506	0.984267178	23047012	0.999233
	10000		2731306	0.846795018	22207214	0.980074107		56400	+20%	3044323	0.978103913	23035697	0.998743
	50000		1259050	0.39034706	18500959	0.816505433		100000		2864999	0.920489296	20986584	0.909901
	1E+05		694218	0.215230496	8524719	0.376222626		1000000		1757330	0.564608732	11300488	0.489947
	1E+06		557447	0.172826971	6830682	0.301459452		5.00E+07		657306	0.211184415	5461356	0.236784
	1E+07	open	557445	0.172826351	5173136	0.228306741		1.00E+08		496904	0.159649205	4943985	0.214353
								1.00E+09	short	496879	0.159641173	4840680	0.209874
Rc (Ω)	1	short	4674331	0.978191474	25441823	0.975997177	*Cc* (pF)	1	open	4803023	0.918884839	25632439	0.898707
	10		4665782	0.976402436	25976253	0.996498938		10		4803023	0.918884839	25620495	0.89897
	100		4674331	0.978191474	25982172	0.996726002		100		4811692	0.920543339	25849942	0.898551
	1000		4692634	0.98202172	26049687	0.999316007		1000		5227013	1	28513116	0.906598
	10000		4778544	1	26067517	1		8000	-20%	3417008	0.653720968	23774841	1
	26400	-20%	3405417	0.712647409	20564256	0.788884342		9000	-10%	3254501	0.622631128	23313313	0.833821
	29700	-10%	3232763	0.67651632	19639629	0.753413875		10000	NOM	3081692	0.589570372	22782830	0.817635
	33000	NOM	3081692	0.644901878	18453394	0.707907623		11000	+10%	2935710	0.561641993	22600652	0.79903
	36300	+10%	2947809	0.616884348	18071189	0.693245506		12000	+20%	2799576	0.535597673	22337798	0.792641
	39600	+20%	2828060	0.591824623	17879537	0.685893367		1.00E+05		918382	0.1756992	14829193	0.783422
	50000		2523497	0.5280891	14914065	0.572132167		1.00E+06		479163	0.09167052	9997957	0.520083
	1E+05		1768525	0.370097042	11159135	0.428085843		5.00E+07		392662	0.07512168	7693076	0.350644
	1E+06		817781	0.17113602	4893274	0.187715385		1.00E+08		300239	0.05743988	5188663	0.269808
	1E+07	open	650875	0.136207807	4237914	0.162574518		1.00E+09	short	299472	0.057293142	5167123	0.181975

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