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Simulation of Organic Thin Film Transistor at both Device and Circuit Levels

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Abstract: Organic materials and devices are gaining more and more attention in microelectronics. They are dedicated to low cost applications and easy fabrication. Organic thin film transistors (OTFTs) are now making significant inroads into many new large-area applications, considering that they can be fabricated at low temperatures and with high throughput on a wide range of unconventional substrates, such as glass, plastic, fabric, and paper. In this paper an OTFT model is used in cadence, a Verilog-a code is written and used to create an OTFT device. This is done so that OTFT circuits can be simulated before fabrication. First, the model is validated by characterizing the device, showing its FET characteristics. Second, the device is used inside a circuit, and the circuit performance is analyzed. Inverter circuit is implemented using the modelled OTFT device, transfer characteristics, input and output waveforms are drawn using the simulation tool. The transistors used have 10m/20u W/L ratio, the inverter is used at 1 kHz frequency.

Keywords: Organic Thin Film Transistor, Organic Electronics, OTFT, Verilog-A

1. Introduction

Recently there has been remarkable interest on organic electronics because of their unique advantages such as low cost fabrication[1], light weight and mechanical flexibility. The contemporary portable communication and computing devices need light weight, high image quality, thin, and low power flat panel displays. The answer to this need is Organic Thin Film Transistor (OTFT). It is likely to have suitable applications requiring large area coverage, structural flexibility and low cost which was not possible with crystalline silicon . However, the innovative human mind soon searched a novel class of TFTs based on organic or polymeric semiconductor as active layer material that shows amazing possibility for integration on to flexible plastic substrates, thus giving the world an idea of futuristic technology of low cost, thin, printable electronics, rugged, flexible and lightweight displays. Organic semiconductors are actually new class of materials comprising small molecules and polymers with semiconducting properties. To make OTFT, need to have organic semiconductor (OSC), gate dielectric insulator, contact electrodes and substrate [2].

Plastic substrate is used for flexible displays, for that the gate insulator should be organic to reduce the thermal stress induced by the difference in the thermal expansion coefficient between TFT organic semiconductor layer and substrate. Many organic semiconductor materials have been analyzed including Pentacene, Poly (3-octylthiophene) (P3OT), Poly (3-alkylthiophene) (P3AT) and poly (3-hexylthiophene) (P3HT) are the most extensively used organic materials for semiconducting layer, but Pentacene shows the best organic thin film transistor performance. To meet the performance requirements, it is important to fully understand the driving mechanism of OTFTs, which is still under continuous discussion owing to ambiguities of interface energetic and complexities of carrier behavior [3]. Organic thin film transistor fabrication methodology has progressed remarkably in past decade and it appears that OTFT will find use in numerous low-cost, large-area electronic applications such as smart cards, flexible displays, Mobile phones, Price and Inventory tags, Flexible integrated circuits, Sensors and other novel products. The efficient design of complex integrated circuits based on OTFTs requires preliminary characterization and modeling. To this purpose, the availability of accurate analytical models [simulation program for integrated circuits emphasis (SPICE-like)] is particularly attractive. A model is used in this work to create a device symbol in cadence [4], so that a circuit consists of more than one OTFT can be simulated in cadence. In section II, the OTFT device operation is illustrated, and the used model is explained. In section III, the model is used inside cadence by writing its corresponding Verilog-a code and inserting it to create a device symbol. This symbol is characterized and its curves are drawn. Finally, an inverter circuit is designed and simulated.

2. OTFT Device Operation and Its Model in Different Regimes

Organic materials such as P3HT, P3OT or Pentacene acts as p-type semiconductor having holes as majority carriers. When a negative gate voltage is applied, an electric field is formed across the dielectric, causing an accumulation region of holes at the dielectric-semiconductor interface [5]. Applying a voltage to the source-drain terminals allows a current to flow across this accumulation layer between the contacts. Fig. 1 shows the Structure and operation of OTFT.

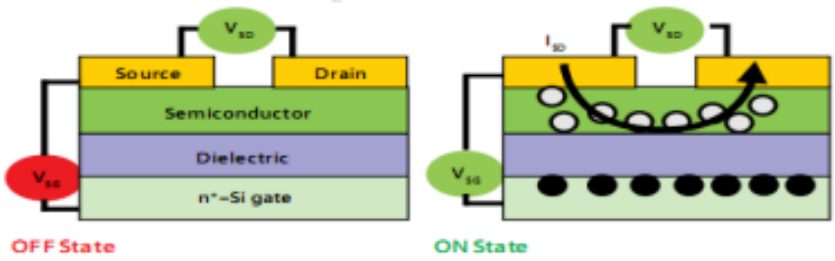

Figure 1 OTFT operation with organic semiconductor layer and metal contact in top contact structure.

A. Linear Regime

Unlike CMOS standard technology, OTFT is only a drift mechanism where the subthreshold regime and linear regime are driven with a unique mechanism and then can be modeled using a single equation. The equation obtained depends on the universal mobility law (UML). In the variable range hopping (VRH) model, the conductivity and thus the mobility of the charge carriers increase with doping. The general equation for the drain to source current in the linear regime is expressed with:

$$I_{d,lin} = \pm \frac{K_3}{(2m+1)(2m+2)} \frac{W}{L} \frac{C_0^{2m+1}}{(2\varepsilon_0 \varepsilon_p kT)^m} \left\{ (V_{gs} - V_t)^{2m+2} - [(V_{gs} - V_t) - V_d]^{2m+2} \right\} \quad (1)$$

B. Saturation Regime

Based on the previous calculations Based on the previous calculation, the current equation in the saturation regime Based on the previous calculation, the current equation in the saturation regime $\{(V_{ds} > (V_{gs} - V_t)\}$ is given by:

$$I_{d,sat} = [\frac{K_3}{(2m+1)(2m+2)} \frac{W}{L} \frac{C_0^{2m+1}}{(2\varepsilon_0 \varepsilon_p kT)^m} (V_{gs} - V_t)^{2m+2}] * [1 + \lambda(V_d - V_{gs} + V_t)] \quad (2)$$

3. OTFT Device Simulation

The Verilog-A language is a high-level language that uses modules to describe the structure and behavior of analog systems and their components. With the analog statements of Verilog-A, you can describe a wide range of conservative systems and signal-flow systems, such as electrical, mechanical, fluid dynamic, and thermodynamic systems Verilog-AMS HDL lets designers of analog and mixed-signal systems and integrated circuits create and use modules which encapsulate high-level behavioral descriptions as well as structural descriptions of systems and components [6]. The behavior of each module can be described mathematically in terms of its ports and external parameters applied to the module. The structure of each component can be described in terms of interconnected sub-components. These descriptions can be used in many disciplines such as electrical, mechanical, fluid dynamics, and thermodynamics. The model equations described in the previous section are now written in Verilog-A, and a device symbol is created in cadence as shown in Fig.2.

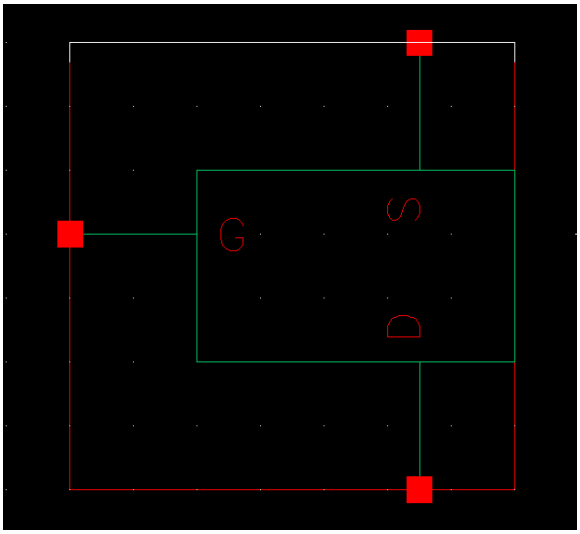

Figure 2 OTFT device symbol created in cadence.

Two primary sets of curves are required for the characterization of the organic transistor: the transfer characteristics (Id vs Vgs) that allow the effective mobility (μ) and the threshold voltage (Vt) to be determined and the output characteristics (Id vs Vds) that provide saturation and general electrical performance information. These two curves are shown in figs. In figure 1, drain current versus drain to source voltage at Vgs of -10 V, and in fig. 2 drain current versus gate to source voltage at Vds of -10 V.

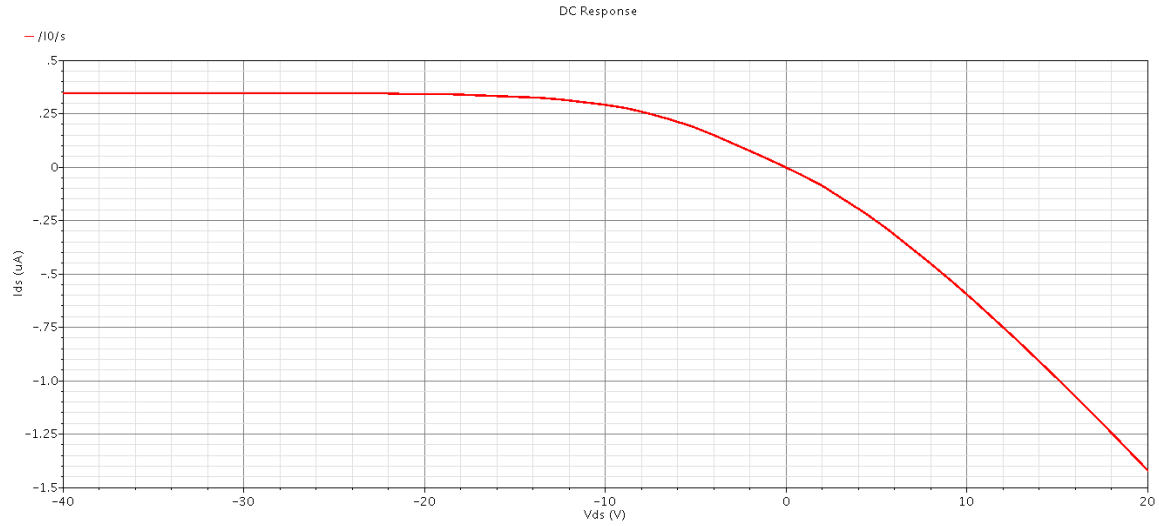

Figure 3 drain current versus drain to source voltage at Vgs of -10 V.

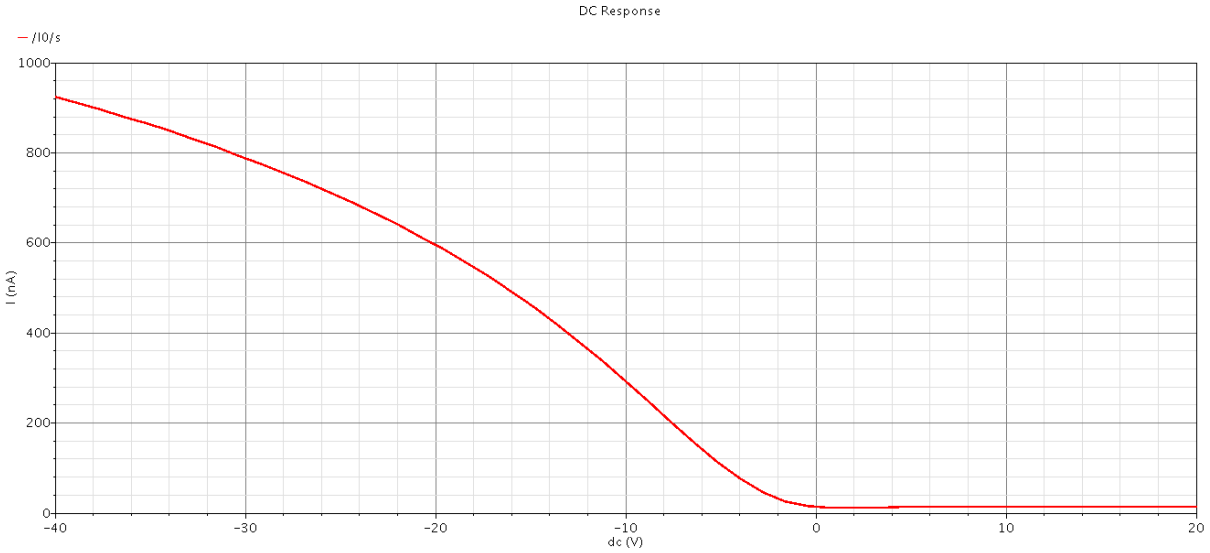

Figure 4 drain current versus gate to source voltage at Vds of -10 V

4. Simulation of OTFT-based Inverter Circuit

Recently, organic inverters have been considered as one of the key elements in organic flexible circuits and have drawn more attention because they are flexible and economic to produce. The simulation of an inverter Fig. 5 using a drain-gate shortcut of the load transistor is done.

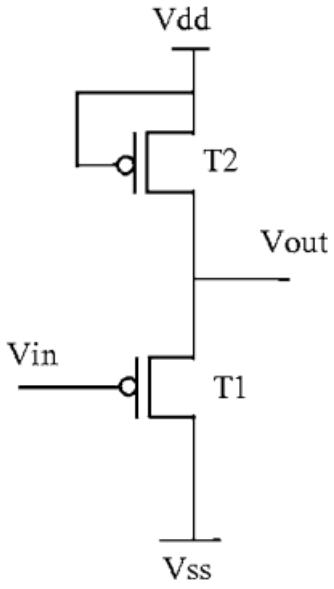

Figure 5 Topology of the p-type OTFT inverter.

The transistor sizes are T1: W/L=20mm/20um and the load transistor T2: W/L=10mm/20um.The inverter is simulated using a Vdd =−20 V, Vss =0 V, and an input pulse ranging between 0 and −20 V with a rise time and fall time of Tr =Tf =100 us and the total period is P = 1 ms. The simulations are shown on Figs. 6, 7 While Fig. 6 shows the input and output voltages for different cycles of inversion, Fig. 7 shows the inverter linearity.

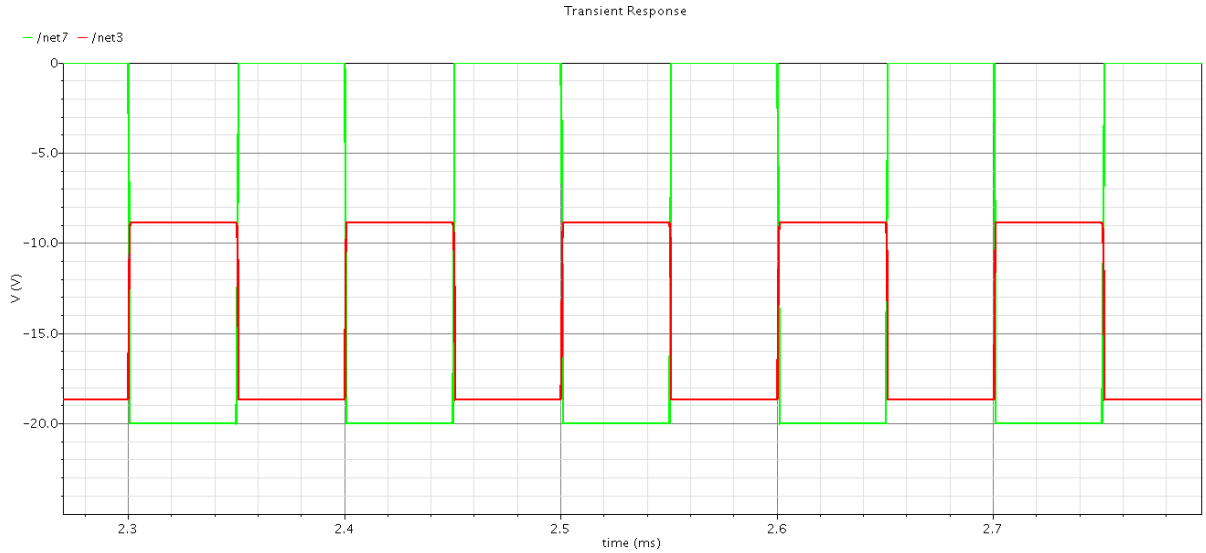

Figure 6 Simulation of a p-type OTFT inverter.

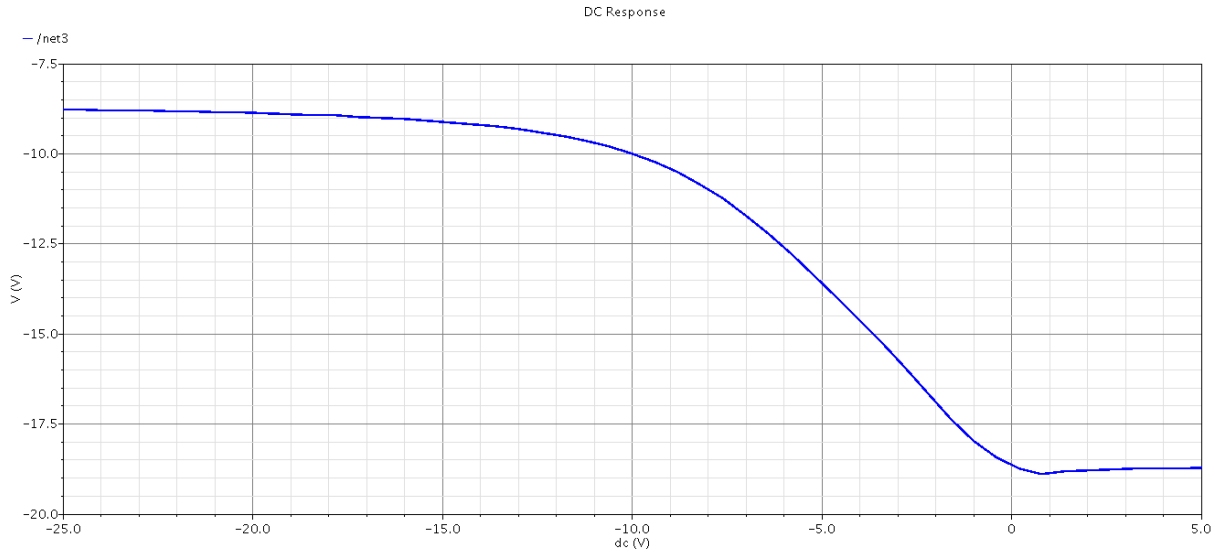

Figure 7 Transfer characteristic of a p-type OTFT inverter.

Conclusion

A universal model for OTFTs was validated by characterizing the device, showing its FET characteristics, then the device was used inside an inverter circuit, transfer characteristics, input and output waveforms were drawn using the simulation tool. The transistors used had 10m/20u and 20m/20u W/L ratio, the inverter was used at 1 kHz frequency with a supply voltage of -20 V. The next big leap will be the further development of advanced devices that will exploit properties unique to organic semiconductors and to prepare multifunctional systems that cannot currently be fabricated from inorganic semiconductors. All technologies require improvements in charge mobility to reduce the drive voltage.

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