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Design of Low Voltage 1st Order 3-Bit Quantizer SR ΔΣ Modulator Using SR Op-Amp

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Abstract: This paper presents a low power (LP) switched resistor (SR) ΔΣ modulator based on 3-bit dynamic quantizer. The proposed design offers lower noise compared to switched capacitor (SC) techniques due to reduction of the number of switches and capacitors. The modulator is designed in a 0.18 µm CMOS technology. The total power consumption is 17.4 mW , and signal to noise ratio (SNR)= 65.8 dB, using, over sampling ratio (OSR) = 64 and 3 V power supply.

Keywords: switched resistor, sigma delta modulator, analog to digital.

1. Introduction

Very large-scale integration (VLSI) CMOS technology developed for digital circuitry is cheaper than analog signal processing especially in wireless transceivers. However, moving from analog to digital signal processing is increased that provide the interfaces between the analog and digital circuits. For example, if it is desired that most of the channel filtering in the receiver be performed by digital filters, the digital filters must be preceded by analog-to-digital converters (ADCs) to digitize not only the desired signal but also the interfering signals to be removed by the digital filters. This creates a potential problem because high-performance data converters often require high-precision analog processing [1].

Recently, ΔΣ modulation becomes suited for high resolution ADC [2]. In addition, oversampling is employed to shape the quantization noise from a coarse quantizer outside the signal band. Delta–sigma modulators form the basis of ADCs [3]. Fig.1 shows the block diagram of a ΔΣ ADC. It consists of two main building blocks ΔΣ modulator and a decimator.

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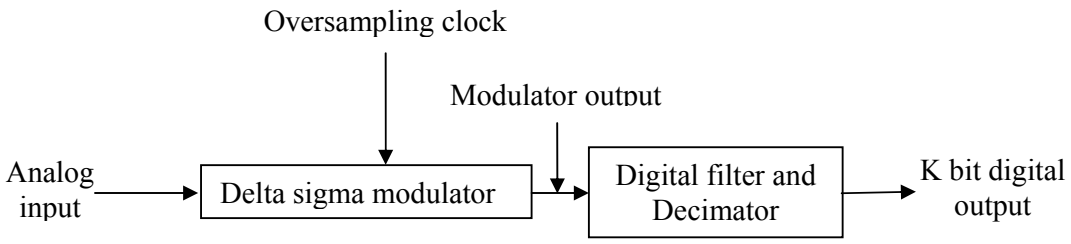

Fig. 1 ΔΣ ADC block diagram

There are more than one architecture for ΔΣ modulator. Each one has its own advantages and disadvantages. The single loop low order architecture has high stability and requires simple circuitry but it requires high OSR. Single loop higher order architecture satisfies large SNR but its drawback is the need of low integrator gain. The Mash structure has the advantages of large SNR for low OSR and grantees stability but its disadvantages are higher complexity of digital part and high sensitivity for circuit imperfections. Multi-bit structure has the advantages of larger SNR for low OSR and better stability but more complex analog and digital circuitry is paid for, in addition the sensitivity of DAC linearity as stated in [3].

In this paper a 1st order switched resistor ΔΣ modulator is represented using 3-bit internal quantizer. The proposed system provides low power consumption, lower circuit complexity, and acceptable SNR for suitable OSR. Section 2 presents the modulator architecture. In section 3, two stages switched op-amp circuit is discussed. In section 4, a 3-bit dynamic flash ADC is discussed as a multi level quantizer. In section 5 switched resistor integrator circuit is discussed. Section 6 illustrates 1st order 3-bit ΔΣ modulator. Section 7 is a conclusion.

2. Modulator Architecture

A block diagram of a basic first order ΔΣ modulator is shown in Fig. 2 [3]. It consists of one integrator and qauantizer in the forward path and a DAC in the feedback path of a single-feedback loop system. If single bit modulator is used, the quantizer is a single comparator and a single bit DAC in feedback is used. On the other side in a multi bit modulator, the quantizer is a Flash ADC and an equivalent number of bits DAC in feedback. Some advantages of using multi bit are lower in-band quantization noise, lower noise due to clock jitter and lower slew rate requirement in the integrator [3].

Although ΔΣ modulators inherently generate sampled output sequences, they can be implemented using continuous- time integrator in place of switched capacitor loop filters [4,5]. Such ΔΣ modulators are referred to as continuous-time ΔΣ modulators. In a continuous time a sample-and-hold operation were added prior to the quantizer, then the theoretical performance of the modulator in the band of interest would be preserved. Continuous time ΔΣ modulators offers lower noise but require larger silicon area In integration compared to switched resistor. While the majority of present-day modulators are implemented using switched capacitor, which has larger noise compated to switched resistor because of larger number of switches and capacitors are used. In prior work a 72 dB SNR and power dissipation of 62 mW in 3.3 v supply voltage using multi bit continuous time architecture is achieved [6]. A 72 dB SNR 81 mW and dissipated power of supply voltage 3.3 v is implemented in switched capacitor 2-2-2 Mash architecture [7].

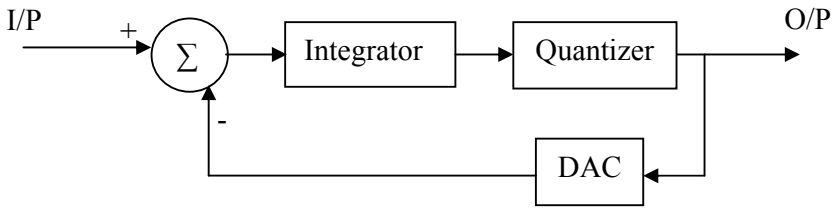

Fig. 2 First order ΔΣ block diagram

This paper presents a ΔΣ modulator using switched resistor instead of switched capacitor and continuous time. Some of the advantages of switched resistor circuits compared to switched capacitor are reducing the number of switches, capacitors, and less number of clock signals. That leads to larger SNR and reducing circuit complexity which leads to occupation of a smaller silicon area in integration and lower power dissipation. More over in switched capacitor technique, circuit topology is changed. Hence in switched resistor, change of circuit topology is not needed. Some advantages of switched resistor compared with continuous time are occupying smaller silicon area in integration and lower power dissipated. Although continuous time provides lower power dissipated than switched capacitor.

In the switched resistor technique, the equivalent resistance Req depends on switch resistance Ron1 and duty cycle D of the clock signal as in equation 1[8].

$$R_{eq} = R_{on1} / D \tag{1}$$

3. Two-Stage Switched op-amp Circuit

Figure 3 illustrates a two stage switched op-amp circuit. The input stage consists of a single p-channel differential pair M4-M5. This differential pair amplifies the differential input signal and rejects the common-mode input voltage. The common-mode input voltage range is a key parameter of the input stage. It is defined as the range of common-mode voltages at which the input stage properly responds to differential input signals. The current mirror formed by M11 and M8 supplies the differential pair with the needed bias current. The W/L ratio of M8 is selected to yield the desired input-stage bias loaded with the current mirror formed by M6 and M7. The second gain stage consists of M9, which is a common-source amplifier actively loaded with the current-source transistor M10. The function of this output stage is to drive a relatively large current into the load. Also the maximum output voltage swing has to be reasonably large. M9 and M10 work as a push-pull output stage. The biasing is implemented with NMOS transistor M12 as shown in Fig. 3 [9, 10, 11]. Capacitor Cc is included to ensure stability when the op-amp is used with feedback. It is called a Miller-feedback compensation capacitor. When used as a comparator, this capacitor is not connected.

The implementation of analog CMOS circuits that operates in the very low power supply voltage range becomes more important nowadays. Most accurate filter circuits are designed using the switched-capacitor technique. The existing design techniques require, however, the on-chip generation of a higher voltage by means of a voltage multiplier [12].

In this paper we achieve a switched op-amp by adding a single switch "transmission gate" instead of compensated resistor. The switch is allocated between differential stage and output stage as in Fig. 3.

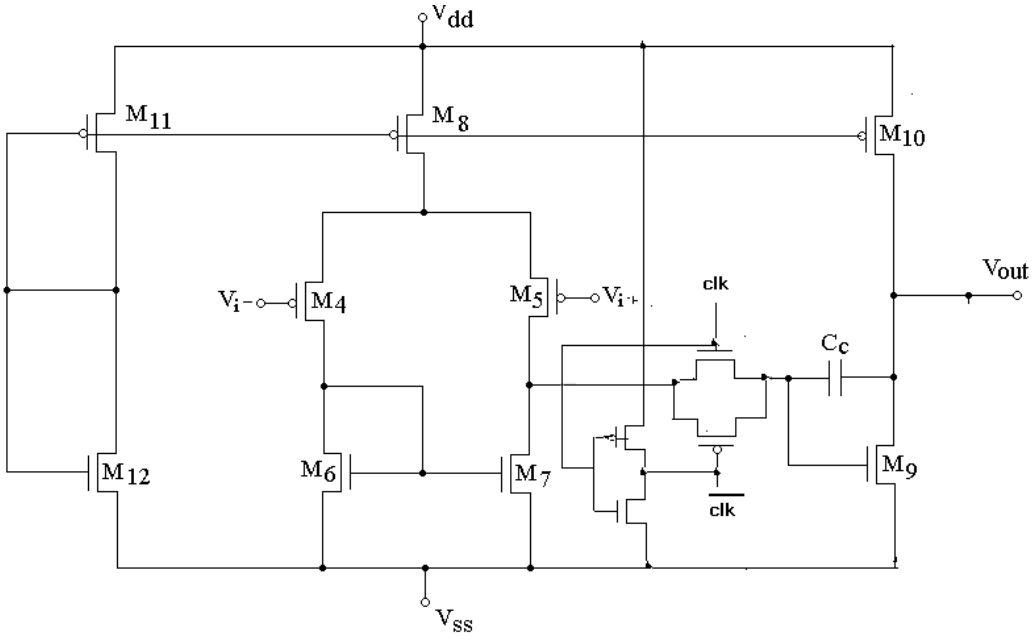

Fig. 3 Two stage switched op-amp circuit

4. 3-Bit Dynamic Flash ADC

Flash ADC, which is the fastest architectures, is shown in Fig. 3. It performs 2^N level quantization using 2^N- 1 dynamic compotators. The reference voltages for the comparators are generated using a resistor ladder, which is connected between the positive vref and the negative -vref reference voltage determining the full-scale signal range. Together the comparators outputs form a 2^N- 1-bit-code, where all the bits below the comparator, whose references is the first to exceed the signal value, are ones, while the its above all zeros. This so-called thermometer code is converted to N-bit binary word with a logic circuit [13].

The thermometer to binary encoder part is a combinational circuit and is implemented using two logic gates, 3 inputs, nor pseudo gate, and inverter as shown in Fig.5.

In the NOR CMOS logic gate circuit, the PMOS transistors act as an active load. In the ordinary NOR CMOS logic gate circuit the number of PMOS transistors is increased by increasing number of inputs. The pseudo NOR CMOS logic gates representing the active load as an only one grounded gate PMOS transistor, independently of the number of inputs. So, if we use ordinary COMS NOR-gate in the previous design more 3 transistors are required for each NOR gate, so the four inputs pseudo CMOS NOR gate is recommended to reduce the total number of transistor. By using 3-bit flash ADC in forward path a 3-bit DAC is required in feedback. The 3-bit R-2R ladder DAC is used. Fig. 6 shows a simulation curves for 3-bit flash ADC connected to DAC applying a sinusoidal input.

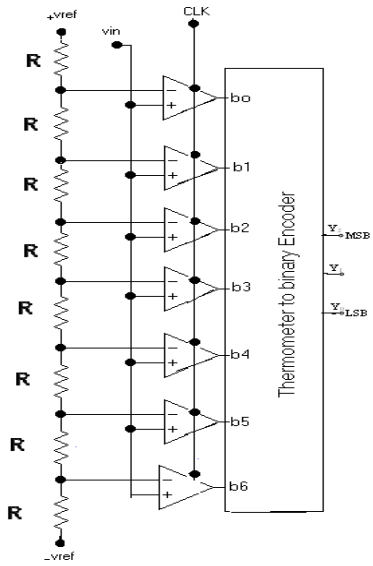

Fig. 4 3bit flash ADC

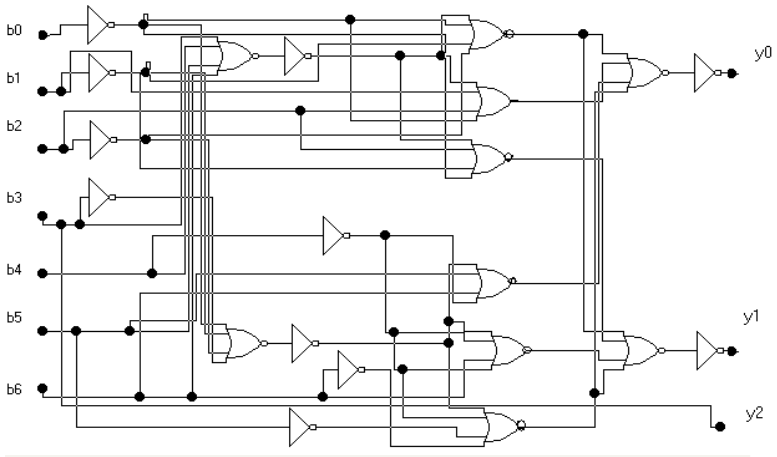

Fig. 5 Encoder circuit

5. Switched Resistor Integrator Circuit

Op-amp RC integrators built with linear resistors and capacitors can achieve very high linearity. By means of a switched resistor, tuning of the RC time-constant is possible via the duty-cycle of the clock controlling the switched resistor [8]. Fig. 7 shows the switched resistor integrator circuit. The equivalent resistance follows as equation 1 but the meaning of Ron1 is equivalent to be the parallel combination of the on-resistance of both NMOS & PMOS transistors. Fig 7 shows the switched resistor integrator square Figure 8 shows the input square wave and the output response.

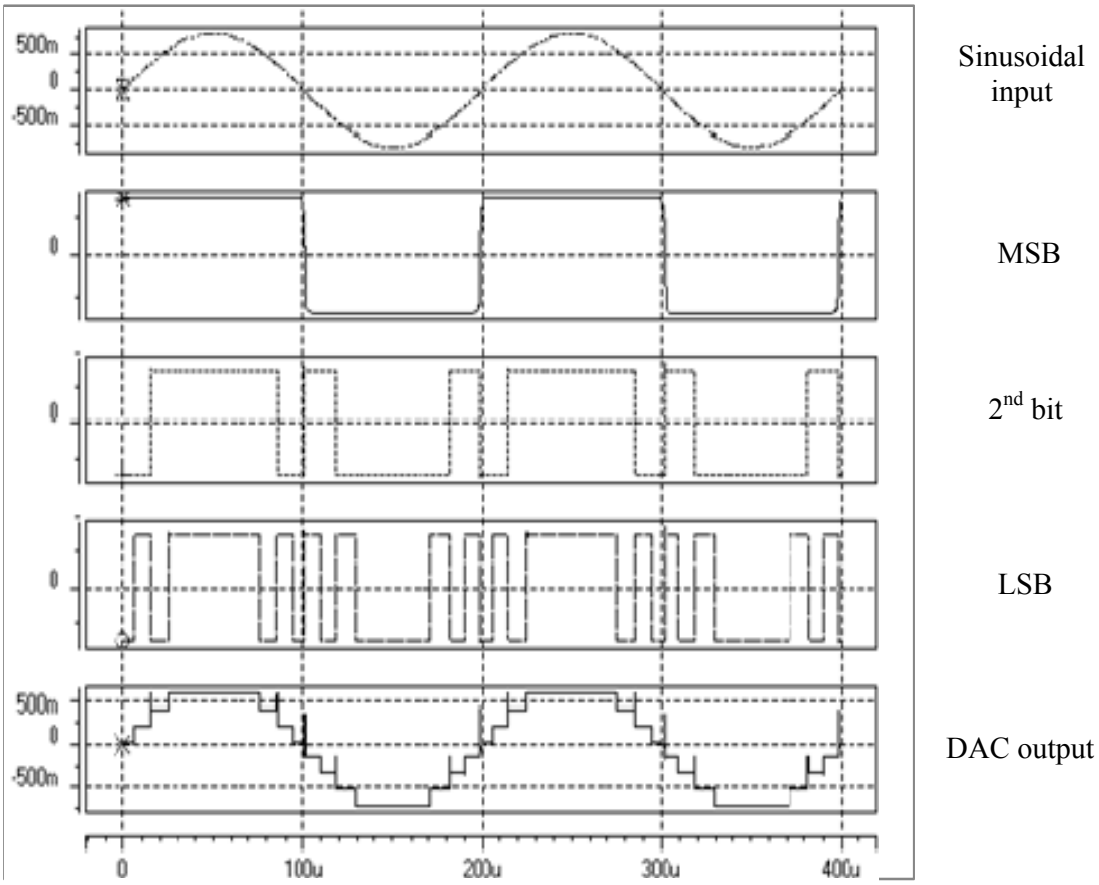

Fig. 6 Flash ADC & DAC simulation curves

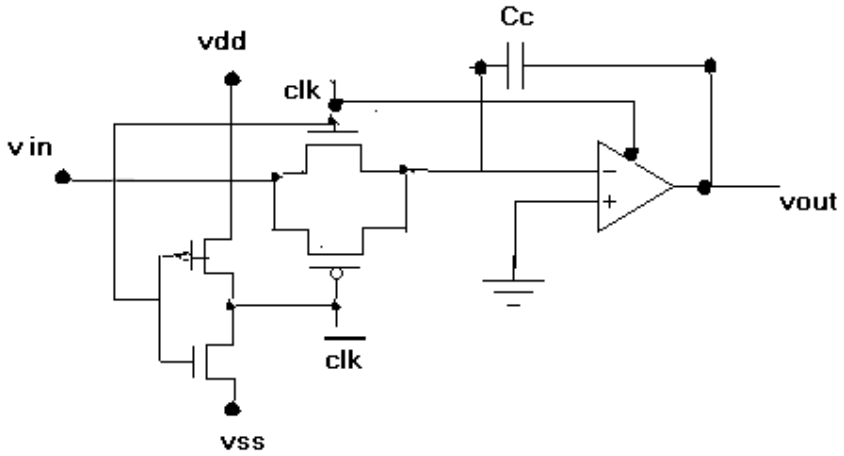

Fig. 7 Switched resistor integrator

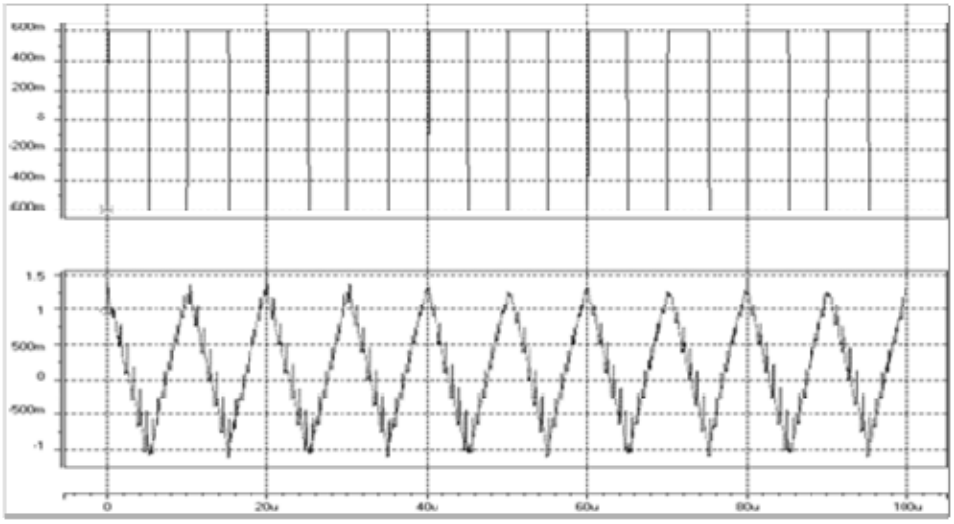

Fig.8 The switched resistor integrator output response

6. ΔΣ Modulator Circuit

If the resolution of the internal quantizer is increased, the output will track the input much closer, since the separation between the output code levels decreased. Fig. 9 shows the circuit of 1st order 3bit ΔΣ modulator and Fig. 10 shows it's response [14].

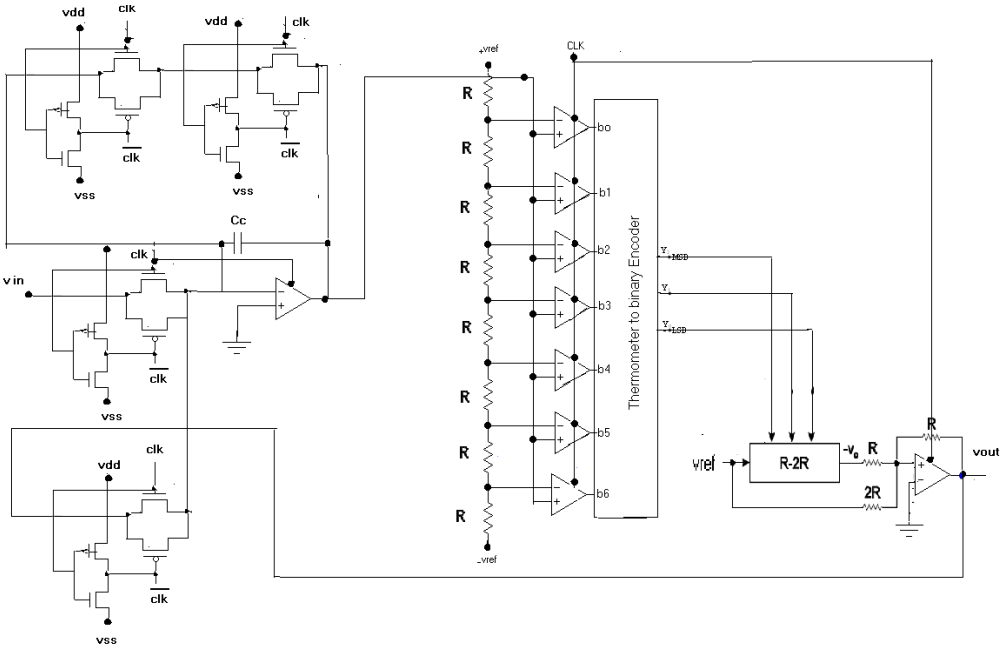

Fig.9 1st order 3bit ΔΣ modulator circuit

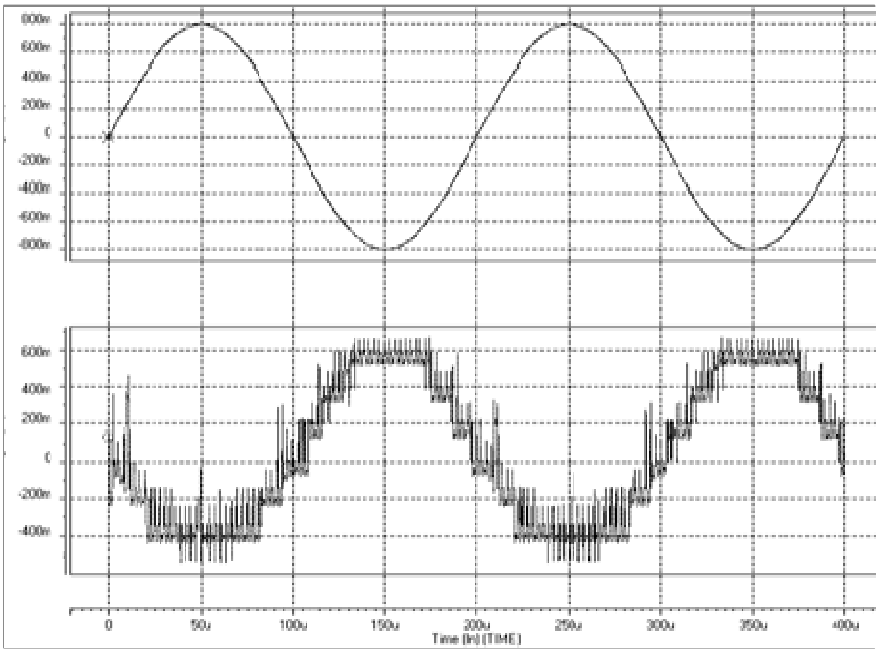

Fig. 10 1st order 3bit ∆∑ modulator circuit response.

Table 1 Resulted System Parameters

Parameter	Value	Unit
Total power dissipation	17.4005	mW
Oversampling ratio	64	-
SNR	65.8	dB
Input signal frequency	5	kHz
Duty cycle	50	%
Technology	0.18	mμ

7. Conclusion

A SR ∆∑ modulator has been designed using 3-bit quantizer and simulated using Hspice. The proposed modulator is designed for low power analog CMOS integrated circuit. The total power consumption of the modulator is 17.4 mW at 3 V supply voltage. Due to using SR technique, the low power dissipation is achieved for acceptable SNR using suitable OSR.

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