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DESIGN AND IMPLEMENTATION OF A DIGITAL RADIO FREQUENCY MEMORY

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ABSTRACT

In this paper the first digital radio frequency memory designed and implemented in Egypt is described. It took two years of dedicated work from the research group to understand the new concepts and techniques, solve many technical problems and perform many design trials until this DRFM system has been built. The design and performance of this DRFM are described in detail and test results are given at the end of the paper.

KEY WORDS

Digital RF memory, DRFM, FIFO, Euro Card, Single Side Band mixer, Compact PCI.

NOMENCLATURE

ADC	*Analog-to-Digital Converter*
DAC	*Digital-to-Analog Converter*
FIFO	*First In, First Out pipeline Memory*
Compact PCI	*a modern standard data interface bus for industrial computer systems.*

INTRODUCTION

Digital radio frequency memory (DRFM) is a technique in which high-speed sampling and digital memory are used for the storage of radio frequency and microwave signals [1]. The ability to store and recall radio and microwave signals has many possible applications. Currently the main application of DRFM technology is the storage and recreation of intercepted radar signals in order to deceive hostile radar systems. Modern electronic countermeasure (ECM) systems use DRFM to sample a radar signal sent by an enemy transmitter, inject a time delay and a frequency shift into the sampled signal, and return a false signal to the enemy receiver. By delaying

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and retransmitting a radar signal that has its frequency shifted, an aircraft can deceive a hostile radar system into tracking a false target or present a large number of false targets to a radar operator [2]. The basic task is to input an RF signal that has been converted to a frequency low enough to be sampled by a high-speed A/D converter (ADC). The sampled signal is stored in a high-speed memory and can be retrieved and converted back to the original signal using a D/A converter (DAC) [3].

The performance of a DRFM system is primarily determined by the system architecture, the sampling frequency and the number of quantization bits. The most important performance criteria are the instantaneous bandwidth, the quantization noise level, the level of spurious signals and the amount of signal distortion [1].

SOME DESIGN ISSUES OF DRFM

1. Frequency Down-Up Conversion vs. Frequency Division-Multiplication

Fig.1 shows the functional diagram of a typical digital radio frequency memory system with frequency conversion, while Fig. 2 shows another configuration of DRFM with frequency division-multiplication. The first configuration needs two mixers and one local oscillator to guarantee coherent reconstruction of the input signal. It reserves the differences among spectral components and needs less time to digitize and re-construct the signal. The second approach promises compact wideband DRFMs but has a number of disadvantages.

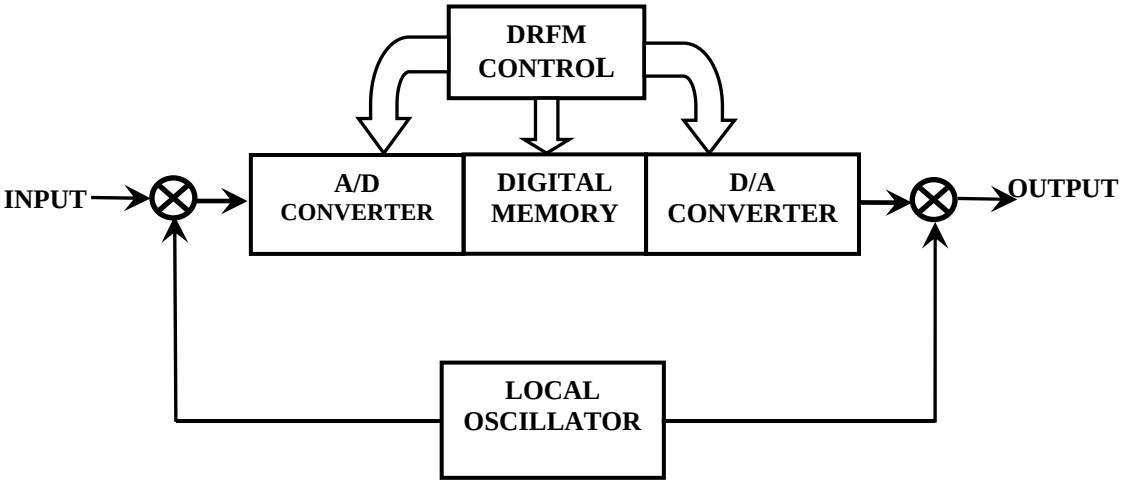

Fig.1. Functional diagram of a frequency translation type DRFM system

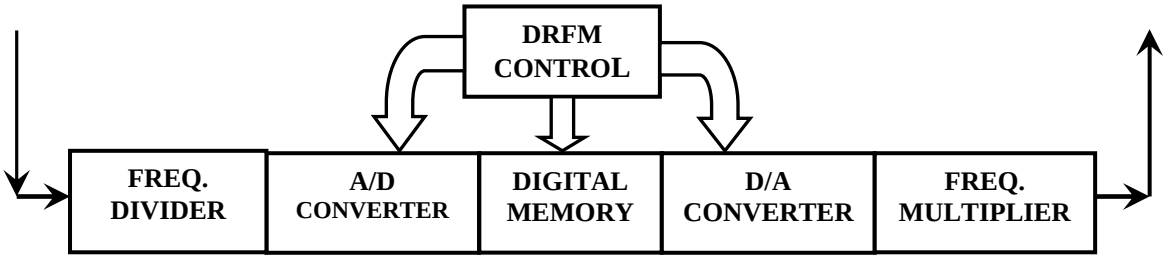

Fig.2. Functional diagram of a frequency division/multiplication type DRFM

When several signals are received simultaneously, a static frequency divider can only divide the largest-power signal. Small signals are mixed with the result and their harmonics generate spurious signals. Frequency accuracy and coherency is likely to be rather poorer than with other architectures [1]. Moreover, a static frequency divider is subject to false triggereing and/or oscillation in absence of input signals [4]. Most of these problems can be avoided by using regenerative frequency dividers which start operation at relatively high microwave frequencies [5].

Both configurations sample the IF signal, stores the samples in a digital memory, extract them at the desired times and re-construct the original signal by D/A conversion and filtering.

2. Amplitude Sampling vs. Phase Sampling

In a phase sampled DRFM system, the detected RF pulse is first down converted to a convenient IF. Amplitude information is removed with a limiting amplifier and quadrature down converted to baseband, generating both in phase and quadrature components. The near-harmonic suppression is improved: the worst-case harmonic for the amplitude technique is the third harmonic while for the phase approach it is the seventh harmonic. The phase digitizing is theoretically independent of signal amplitude, thus eliminating dynamic range problems typically associated with amplitude systems [7]. The performance of a phase sampled DRFM system within a false target jammer is very similar to that of the double-sideband system whilst requiring the storage of approximately half the number of bits. It has the following disadvantages: Digital processing of the stored signal becomes more difficult. In particular the addition of signals must now be carried out in the analogue replay chain. When more than one signal is received simultaneously the smaller signals will be suppressed by up to 6 dB and spurious products will be generated. An additional subsystem is required to ensure that the recreated signal is transmitted at an appropriate level [1]. The advantage of the phase approach over the amplitude approach diminishes as the number of bits increases [7].

FUNCTIONAL DESCRIPTION OF THE EGYPTIAN DRFM

A digital radio frequency memory has been designed and implemented with input multiple down conversion and output single side-band up conversion. The input/output frequency of this DRFM was the standard 21.4 MHz. An input RF signal has to be down-converted to 21.4 MHz before being processed by our DRFM. A scanning super-heterodyne receiver with 20 dB image rejection does this job and stops scanning when an RF signal is detected. The received IF signal is down converted into a new 1.4 MHz IF. An eight-bit A/D converter was used for amplitude sampling, a pipe-line FIFO memory for digital storage of the sampled IF signals and an eight-bit D/A converter and a high performance operational amplifier for signal re-construction. The signal is up-converted by a single-side-band mixer to 21.4 MHz. A specially designed single-side-band filter is used to suppress the residual lower side band of the mixer output. The DRFM was implemented on three standard 160 mm by 100 mm Euoro cards with standard compact PCI interface.

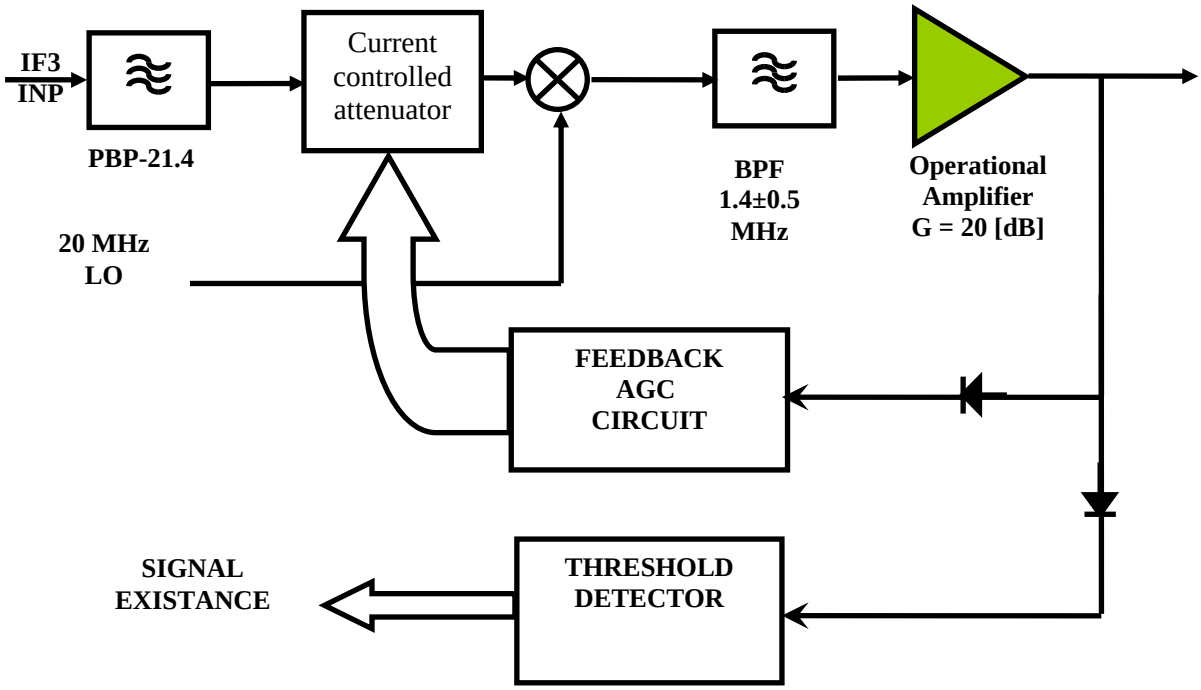

Fig. 3. A Simplified Functional Diagram of the down conversion Board

1. Down conversion of the received signals:

The received signals are down converted to a 1.4 MHz IF frequency; in order to sample their RF information at a feasible rate with minimum possible distortion.
Applying Nyquist criterion for a 1.4 MHz IF; the minimum allowable sampling rate is 2.8 Mega samples per second. At a 10 MSPS sampling rate, we can get at least 7 samples per cycle; which guarantees a reliable time resolution of the RF signal. A closed loop AGC has been designed to guarantee linear operation of the down converter within the system dynamic range. A functional diagram of the down conversion circuit is shown in Fig. 3.

2. A/D conversion of the 1.4 MHz signal:

The DRFM samples the 1.4 MHz IF analog signals at a 10 Msps clock rate. The samples are converted into 8 bit digital data at the same rate. This is done by a fast 8-bit analog-to-digital converer with A/D conversion delay less than 50 ns. Having 256 different levels for voltage quantization we get a reliable RF voltage resolution which guarantees RF storage fidelity.

3. Storage of the samples in th e FIFO memory during reception periods

The DRFM stores the digital samples in an ultra fast FIFO electronic memory during each 50 ns reception period.

4. Extracting the digitally stored signal during the transmission periods

The DRFM extracts the stored digital samples from the FIFO during each 50 ns transmission period and converts them into 1.4 MHz analog signals.

5. Up conversion of the DRFM output:

The DRFM output signal is up converted from the 1.4 MHz IF frequency to the original RF frequency. In order to guarantee the coherency of the transmitted signals with the received ones, the same local oscillators used in the down conversion stages are used in the corresponding up conversion stages.

DETAILED DESCRIPTION OF THE MAIN DRFM BOARD

1. At the arrival of the active low $\overline{MRST}$ TTL signal, the FIFO resets its contents and pointers. The time waveforms of the Master Reset procrss is shown in Fig.4.

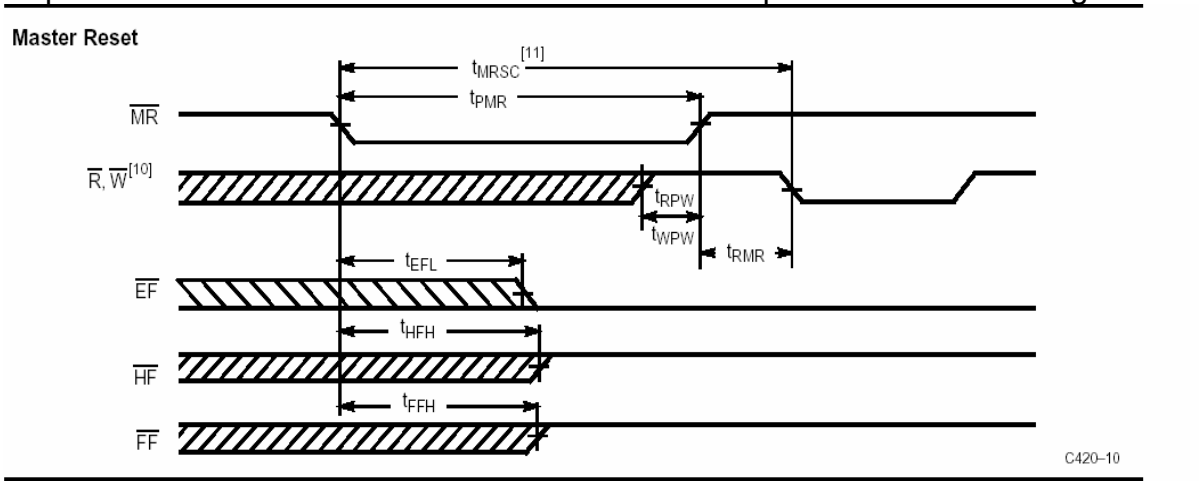

Fig.4. Timing Diagram of the FIFO MASTER RESET

2. the A/D converter samples the input signal at the rising edge of the Rx clock.
3. At the falling edge of the Rx clock, the FIFO gets its active low write enable command ($\overline{WE}$) and stores the 8-bit sampled data in the next memory location. The time waveforms of the WRITE and READ processes are shown in Fig.5.

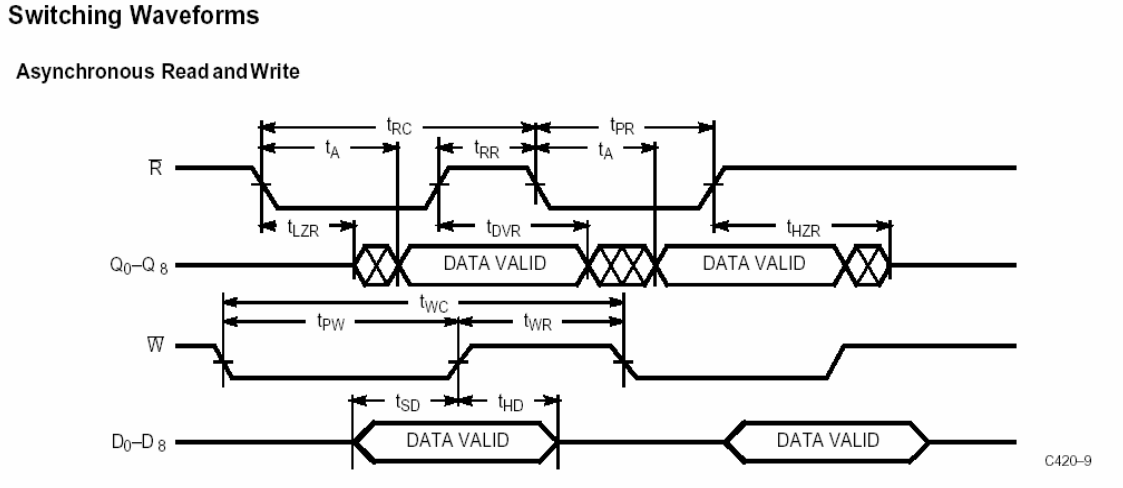

Fig.5.Timing Diagram of the FIFO READ and WRITE

4. The logical diagram of the FIFO is shown in Fig. 6.
5. At the falling edge of the Tx clock, the data is extracted from the memroy location indicated by the READ pointer.

6. At the rising edge of the next Tx clock, the extracted 8-bit data word is converted into an analogue signal by the D/A converter (U1).

7. The balanced A/D converter output is taken from the pins (21 and 22) of U1, through the matching and pre-filtering circuit (composed of R4, R5, R6, R7 and C11) and delivered to the AD711 operational amplifier (U4) where it is amplified and converted into an unbalanced signal (referred to ground). Fig. 7 shows the balanced-to-unbalanced conversion.

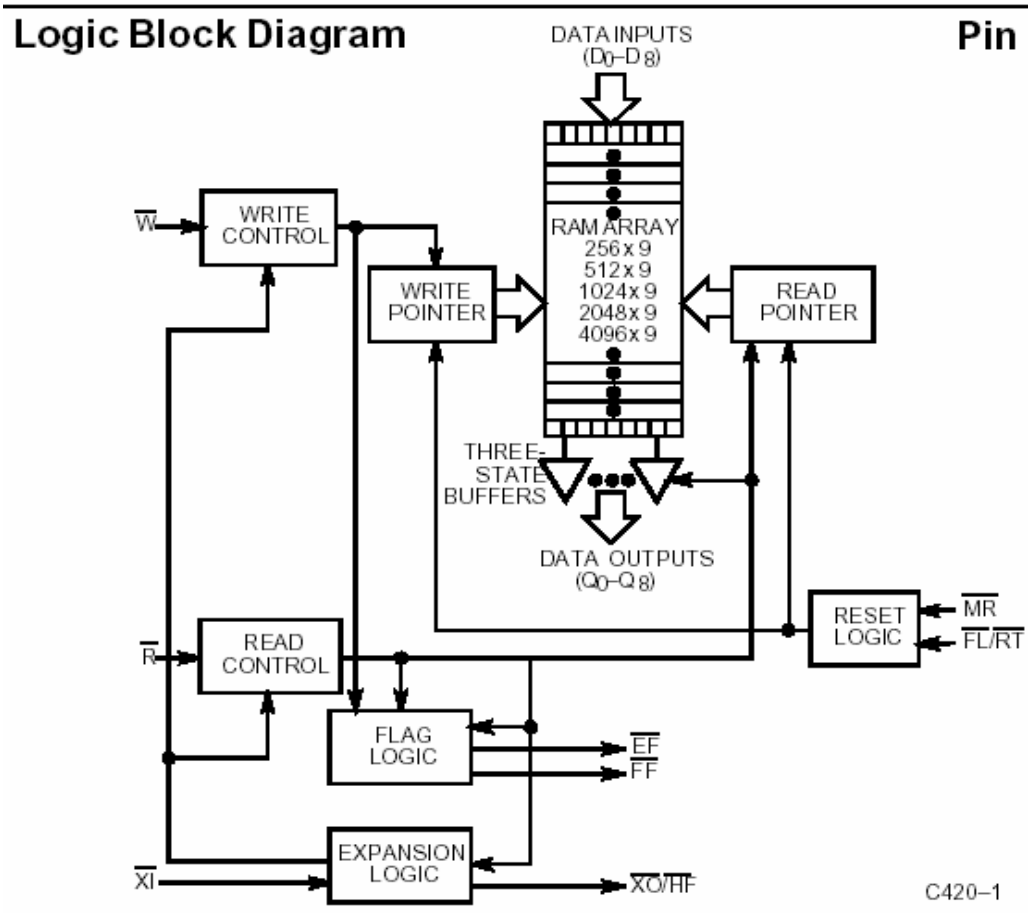

Fig.6. Logical Diagram of the FIFO

8. The output of U4 is the Base Band Up signal (**BBU**). It is the output signal to be up converted into the higher IF frequency.

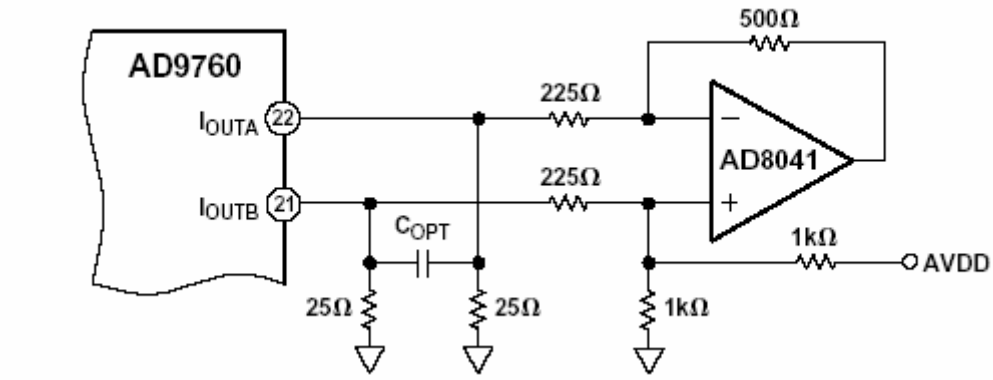

Fig.7. balanced-to-unbalanced conversion at the D/A output

CIRCUIT DESIGN OF THE MAIN DRFM BOARD

Fig. 8 shows the schematic circuit design of the main DRFM board. The ORCAD 9.2 Capture CIS design package was used to design this schematic. Some integrated circuits were found in the ORCAD component library and some have been created by the author and added to the library.

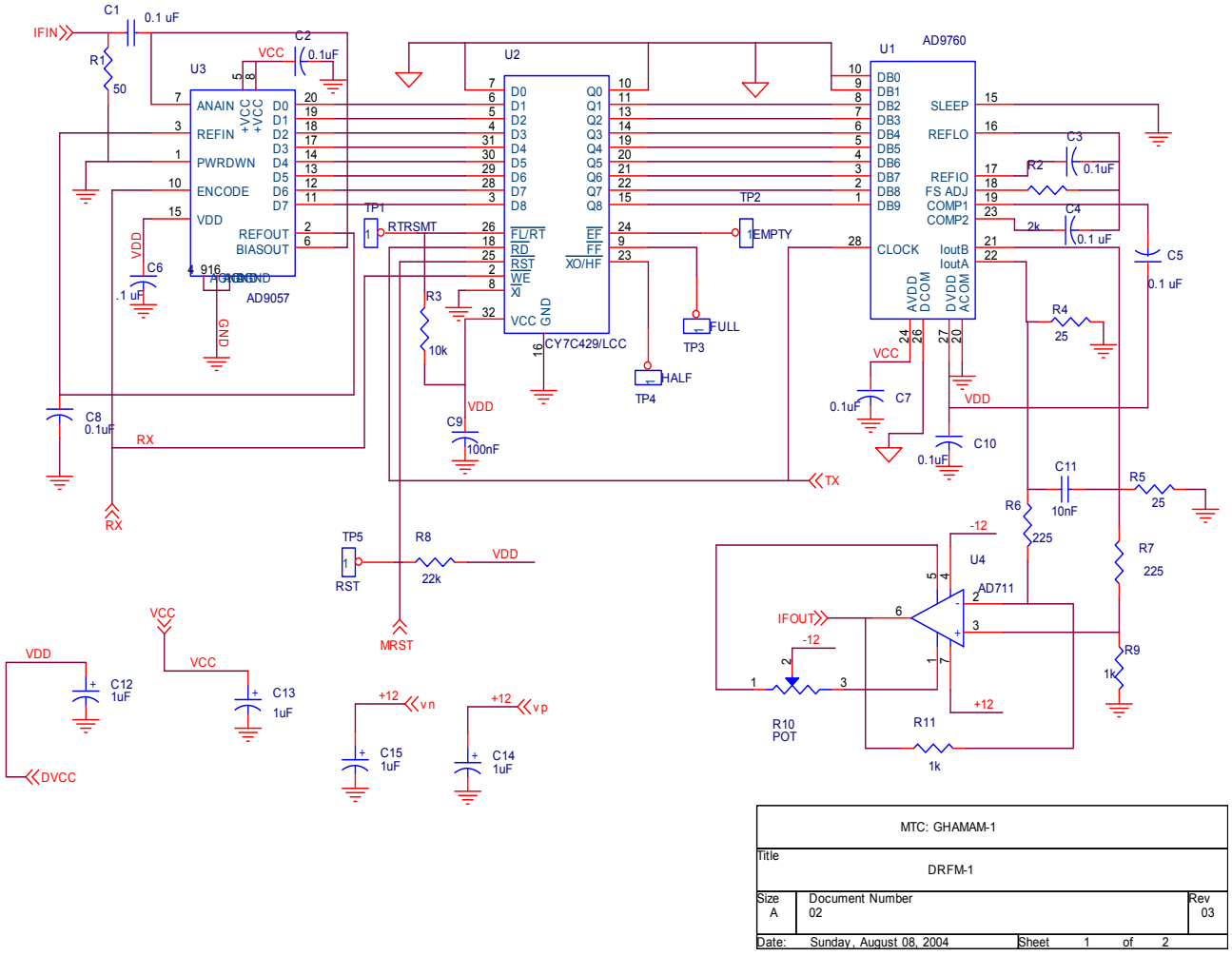

Fig.8. Schematic Design of the Main DRFM Board

IMPLEMENTATION OF THE MAIN DRFM BOARD

Fig. 9 shows a double-layer implementation layout of the DRFM on a standard (100mm by 160 mm) Euoro-Card with Compact PCI interface. The footprints of some integrated circuits were created by the author and added to the footprint library. The dimensions of the Compact PCI multi-pin connector were taken from the official specification of the PICMG international organization, complying with IEEE 1101.1 mechanical standards. This connector is a high density 2mm Pin-and-Socket Connectors (IEC approved and Bellcore qualified) [8]. It is worth noting that the double layer implementation did not conform with the required sampling rate; because of grounding problems. The final successful product was implemented with a 4-layer technology. Separate layers were dedicated for ground and power supply.

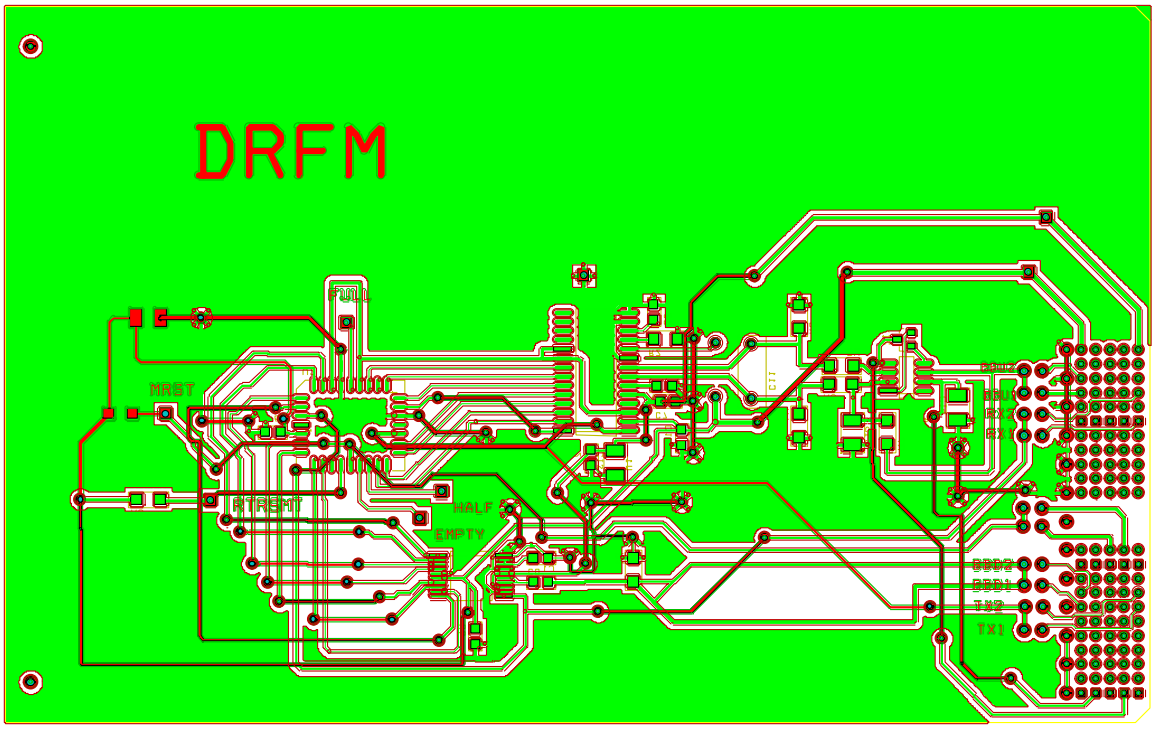

Fig. 9. A preliminary layout of the DRFM board

DRFM BOARD FUNCTIONAL TESTING AND RESULTS

1. A LOW TTL signal was given at the **MRST** control point by connecting the front panel switch to ground. The FIFO flags became as follows:
   FULL = HIGH
   HALF = HIGH
   EMPTY = LOW
2. A 1.4 MHz analogue signal was inserted at the **IFIN** input. It appeared at the connecting point of R1 and C1. It was transferred to the pins (6 and 7) of U3 through the coupling condenser C1.
3. Applying a 100 Hz TTL control signal to the Rx clock point, it was observed that the digital samples appear at the data output pins of U3 (pins 11 to 14 and

17 to 20) and input pins of U2 (pins 3 to 6 and 28 to 31). Testing at these points was carefully done; in order not to cause any accidental short circuit. The FULL flag becomes LOW after 20 seconds; since the capacity of the CY7C429 asynchronous FIFO is 2 Kbytes.

4. With the application of a 100 Hz Tx clock, the FIFO output was observed at the output pins of U2 (pins No 11 to 15, and 19 to 22 of U2). Again, testing at these points was carefully done; in order not to cause any accidental short circuit. It was noticed that the **EMPTY** flag becomes LOW after 20 sec from the start of the 100 Hz Tx clock.

5. Applying a 10 MHz clock to both Rx and Tx control points at the same time; the following was observed:

i. The A/D converter output samples appeared at the U3 output
ii. The FIFO output data appeared at the U2 data output pins
iii. The analogue output was measured at the pins 21 and 22 of U1 and the final output at pin 6 of U4.
iv. A very fast blinking of both the EMPTY and the FULL flags was observed.

UP CONVERTING THE OUTPUT SIGNAL

Fig. 10 shows the functional diagram of the single-side-band up converter board.

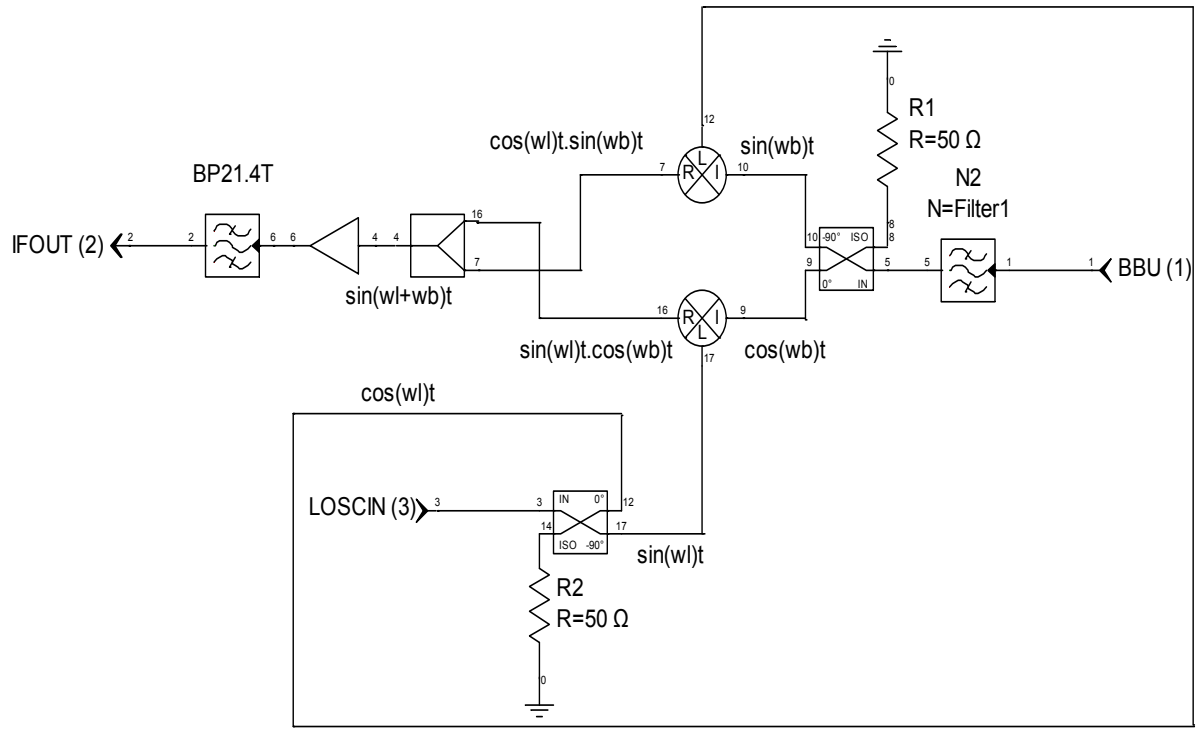

Fig. 10. Functional diagram of the single-side-band up converter board

The re-constructed 1.4 MHz signal is first filtered to get rid of the DRFM quantization noise. Then, a single-side-band frequency conversion is used to up-convert this signal into the original 21.4 MHz IF. It is intended to allow only the desired 21.4 MHz to the up converter output and suppress the un-desired 18.6 MHz mixing output. This is achieved by the use of the following circuits:

A 90º hybrid junction
Two double-balnced mixers

An output power combiner.

The I and Q components of both the local oscillator and the input signals are generated before mixing them to get the upper Single Side Band. Afterwards, a special SSB filter was designed and used to suppress all residual spurs. At the output of the IF amplifier a pure 21.4 MHz was clearly measured.

CONCLUSION

1. The main design issues of digital radio frequency memory have been discussed.
2. A 21.4 MHz DRFM has been designed, implemented and successfully tested by the research team. It was implemented on three standard Euoro Cards, 160mm by 100 mm each, according to the compact PCI technology specifications [8]. They were installed, supplied with necessary voltages and tested in a standard 3U CPCI chassis.
3. The results of system testing conformed to the design requirements. Input signals were down-converted, digitized, stored, re-constructed and up-converted to the original IF frequency with neither distortion nor spurious frequencies.

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REFERENCES

[1] J. S. Roome, Digital Radio Frequency Memory, Electronics & Communication Engineering Journal, August 1990.

[2] D. *C.* Johnston, 'A Dual-port Digital Radio Frequency Memory*' , Msc* thesis, AFIT/GE/ENG/89D-22, School of Engineering, Air Force Institute of Technology (AU), Wright- Patterson AFB, OH, Dec 1989.

[3] K. Gustafsson, 'Implementation of a Digital Radio Frequency Memory in a Xilinx Virtex-4 FPGA', Msc. Thesis, Avdelning Institution, Division of Electronics Systems, Department of Electrical Engineering, Sweden, Dec. 2005.

[4] Hittite Application Note, '*Frequency Divider Operation & Compensation With No Input Signal', 2003.*

[5] Fang, Brunnschweiler, and Ashburn, 'An analytical maximum toggle frequency expression and its application to optimizing high-speed ECL frequency dividers, IEEE Journal of Solid-State Circuits, Volume 25, Issue 4, Aug. 1990.

[6] G. Weber, J. Culp, and M. Robinson, 'DRFM requirements demand innovative technology '*Microwave Journal,* vol. 29. no. 2, pp. 91-104, Feb. 1986.

[7] VU and Hattis, 'A GaAs Phase Digitizing and Summing System for Microwave Signal Storage', IEEE Journal of Solid-State Circuits, Vol. 24. No. 1. Feb. 1989.

[8] PCI Industrial Computers Manufacturers group, 'Revision 2.1 of the CompactPCI specification', Copyright 1995, 1996, 1997 PCI Industrial Computers Manufacturers Group (PICMG).