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MODELING AND SIMULATION OF A NEW VLSI ANALOG CIRCUIT FOR ARTIFICIAL NEURAL NETWORKS APPLICATIONS

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ABSTRACT

This paper presents modeling and simulation for a new VLSI –Artificial Neural Network (ANN) analog circuit designed in 0.34 μm CMOS technology. Differential voltage controlled current source (DVCCS) is used for making synaptic weights and activation functions and capacitors are used for dynamics . Multi output bidirectional neuron current mirror is achieved using super MOSFET which behaves as a single MOS transistor but with nearly zero channel modulation factor λ and intrinsic gain of more than 90 dB. Verification of successful operation of all circuit components were done using HSPICE program. Transfer characteristic of DVCCS with a given bias current which can be seen to have a trance conductance of about 160 μ S with band width reaches 400MHz. .

KEYWORDS: Differential Voltage current control (DVCCS), Super MOSFET , Artificial Neural Network, Analog VLSI Neural network

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I . INTRODUCTION

Artificial Neural networks (ANNs) attempt to behave similarly as brain with its millions of neurons. Both VLSI circuits and biological neurons are of the same class, that is, fundamentally analog. Modeling and circuit design of a small synapse with one D/A per weight can be achieved by a binary weighted current source and then feeding the binary weighted currents into diode connected transistors on the synapse to convert them back tovoltages[1]

On the other hand, the signal processing capabilities has been emphasis upon the synaptic combining of signals via weight matrix summations as opposed to the axon propagation of action potentials. Present analog ANNs consist of synaptic weights, implemented by amplifier gains, summation of the weighted signals, activation functions realized by amplifier nonlinearities , and in many cases dynamics, via capacitors, for smoothly transitioning from an initial state to a desired equilibrium [2].

The work horses of analog VLSI ANNs are the Differential voltage Controlled Current Source (DVCCS) and capacitors. The DVCCS is used for making synaptic weights and activation functions and capacitors are used for dynamics. ADVCCS takes a voltage difference as input, and gives an output current as a function of that difference. DVCCS gains can realize the weights when operating on small signals in a linear region and can also realize saturation nonlinearities when operating on large signals. In both cases the DVCCS output currents can be conveniently summed. Using capacitors in conjunction with DVCC's it is known that any linear circuit can be realized [3] so that any desired filtering of ANN signals is available, as may be needed in special applications such as ANN retinas [4]. Along with the DVCCS and the capacitor it is also convenient to have resistors for conversion of currents to voltage and voltage divisions, as well as for creating and scaling currents (current sources and current mirrors, respectively). All of these devices can basically be constructed of VLSI transistors.

In section II VLSI-ANN Analog Circuit is presented, Modeling and analysis is presented in section III. Simulations results are presented in section IV followed by discussion and conclusions in section V.

II. VLSI-ANN ANALOG CIRCUIT

The two key components in an ANN are the linear weights and the nonlinear activation functions. A weight can be realized by a DVCCS operating in its linear region while a nonlinear activation function can be realized by operating a DVCCS over its full nonlinear range. We consider, current sources, current mirrors, and resistors constructed as diode connected MOS transistors. These are all used for biasing the

transistors, that is, setting the modes of operation of transistors, while the current mirrors and sources are used for various adjustments, as in adapting weights.

A current source can be constructed from a voltage source of voltage V. and current mirrors which allow current in one section of an ANN to determine that in another, perhaps for adjusting weights. The gains are easily set by layout design, being ratios of widths to lengths when the transistors are maintained in saturation. The current mirrors allow current to flow in only one direction. However, by placing a P-mirror on top of an N-mirror we can get a bidirectional current mirror which is convenient for realizing weights.

II. A. DIFFERENTIAL VOLTAGE CURRENT SOURCE

Figure (1) shows the basic configuration of a DVCCS. The bias current, I_{bias} , is steered between I_1 and I_2 by the differential pair consisting of identical transistors P_1 and P_2 with the steering controlled by the voltage difference of the input voltages. The difference of the transistor currents, is designed to be a function of the voltage difference and Ibias, independent of any devices connected, such as loads or the current mirror. To obtain the current output as this difference, the current mirror is used along at the output node so that Iout=- the difference of the transistor currents. The function of Iout versus the voltage difference realized depends upon the MOS transistors and their modes of operation used to form the current difference. In practice there is some loading by whatever is attached in which case three current mirrors are used for isolation and a gain k may be introduced through the upper mirrors so that

$$I_{out} = K\,(I_1 - I_2) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

In some instances it is necessary to convert the output of a DVCCS into a voltage (giving a Differential Voltage Controlled Voltage Source, DVCVS), as when voltage output for an activation function is desired. Such can be accomplished by directing DVCCS output current into a resistor, perhaps made by other DVCCs or an MOS transistor. However one of the best ways to do this is to attach the gates of a CMOS pair, onto the output of the DVCCS. Since the CMOS pair allows no current at its input ,the DVCCS can of course no longer act as a current source but its output voltage is determined by other factors (specifically, the channel length modulation effect through the Early voltage).

Since the DVCCS and the capacitor are sufficient to generate all linear circuits, we can construct many of the components of ANNs using them. A construction of a resistor with resistance on the order of 100 Ohms. This DVCCS resistor has advantage of being variable since gm can be controlled by the bias current which in turn can be controlled by the gate voltage of an MOS transistor realizing the current source.

The two transistors $P_5$and P_6 are used as a current source, under normal circumstances, its drain voltage is larger enough that the drain current Ibias saturated at a value set by the gate voltage V_g. The manner in which Ibias is divided between P_1 and P_2 is a sensitive function of the difference between V_1 and V_2 and is the essence of the operation of the stage

The three current mirrors N_1, N_3 and N_2, N_4 beside P_3 and P_4 are used to generate output current that is proportional to the difference between the two differential drain currents I_1 and I_2 where the current I_1 drain out of P_1 is reflected as an equal current out of P_4 and the current I_2 drawn out of P_2 is reflected as equal current out of N_4. To implement this function we design the circuit in CMOS 0.35 µm technology. All transistors work in saturation mode for the specified output current level. The design procedure starts by adjusting the DC potential level at the gate of the bias current source P6 and at the output at half the supply voltage with both inputs shorted to ground [11].

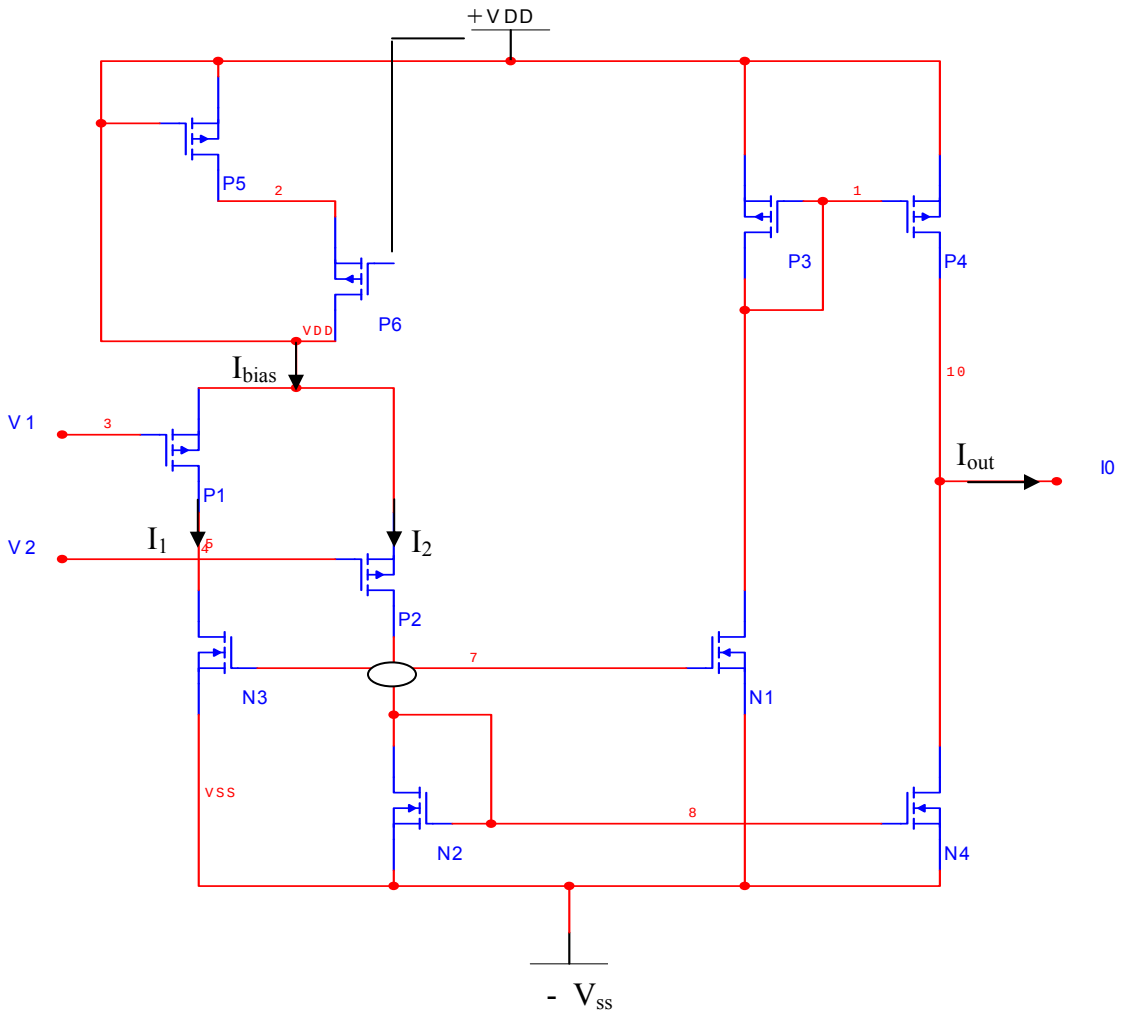

Figure (1): The differential voltage current controlled source (DVCCS)

II. B. SUPER MOSFET

The idea of the super MOS is based on that, the output current I_{ds} of the MOSFET transistor has a great dependence on the effective channel length in the form of the channel length modulation parameter due to short channel MOSFET effects.

The output conductance of the small signal model is also proportional to (1/ lamda) . It can be shown that the drain current in the saturation region increases slightly in a linear manner with VDS. This is physically due to a slight shortening of the channel length as VDS is increased in the saturation region. The channel modulation parameter is the is λ coefficient that represents the linear dependence of I_{DS} on V_{DS}. The effect of drastically reduced in Super NMOS transistors which means that the Super MOS can also be used in a perfect matched current mirror.

The Super MOS behaves like a cascade of MOS transistors having source, gate and drain terminals. Also, the Super NMOS consists of four regular PMOS and eight NMOS. The circuit is self biased and therefore very easy to use in design, it behaves as and intrinsic λ a single MOS transistor but with nearly zero channel modulation factor gain of more than 90 dB. The Super MOS however has an extremely high output impedance due to implementation of the gain-boosting technique. Moreover, it does not require any biasing voltage or current other than one single power supply. Referring to Figure (2), transistor MN1 is the main transistor while MN2 is its cascade. They form the core of the circuit and their sizes determine the current-voltage relationships and the high frequency behavior of the device. The relation between the threshold voltage of the Super MOS and the dimension of the transistor MN3 (W3), in particular we assume all transistors are working in saturation regionwas presented by Alazab and H. F. Ragai in [12].

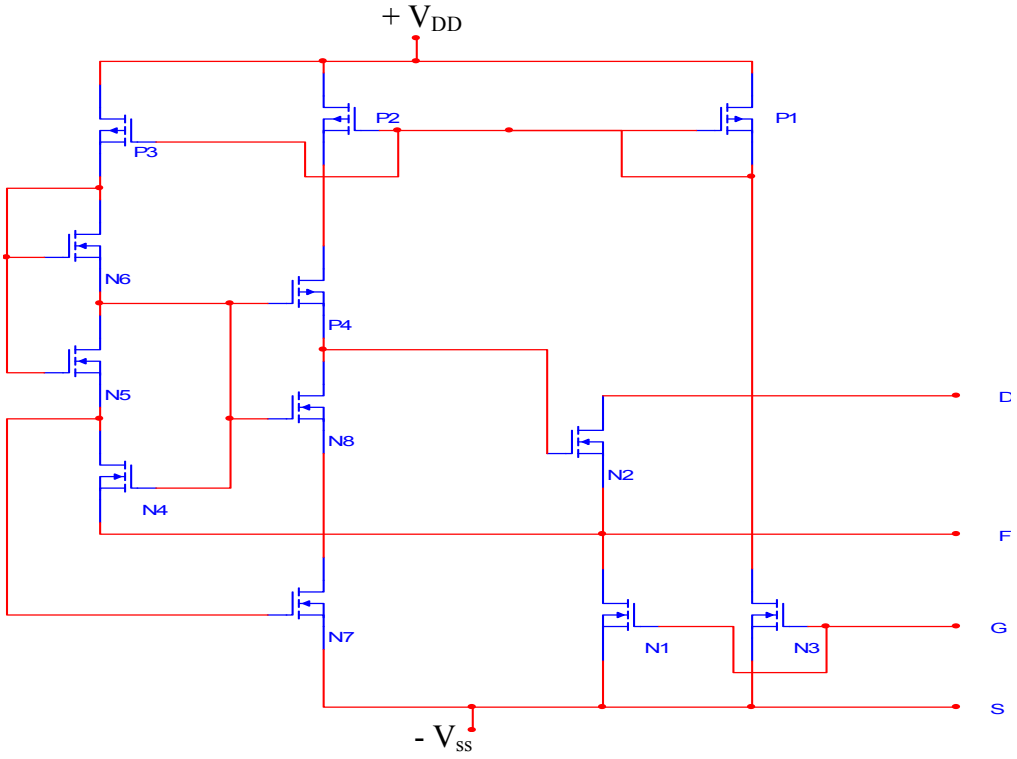

Figure (2) : An N-type super MOSFET

II. C. THE PROPOSED VLSI-ANN ANALOG CIRCUIT

Figure (3) shows an analog circuit suitable for the VLSI realization of the Hopfield continuous time equations which, for the nth neuron of a set N.

$$C\frac{dV_{in}}{dt} + GV_{in} = \sum_{i=1}^{N} g_{mi}\ R_i\, I_{ni} + I_{bias} \quad n = 1,.,N \ldots\ldots\ldots\ldots\ldots\ldots(2)$$

where I_{ni} is the current output of the i^{th} neuron which is fed to the input of the nth neuron,
V_{in} is the nth neuron's state variable,
G is any of the activation functions available
C is the capacitance,
$g_{mi}R_i$ are the synaptic weights,
I_{bias} is the bias input

The weighted inputs from the synapses to the cell body can be thought to correspond to varying amounts of currents linearly summing, at the input node to the left of the activation function DVCC'S the weights are the current gains of DVCC's operating as linear amplifiers with resistor inputs, the resistors being used to convert the neuron output currents to voltages . The bias input I bias is constructed as a constant current source made of a transistor. Using a resistor –capacitor branch connected to this same input node of the activation function amplifer, we obtain the dynamics of the analog circuit. Because each neuron output current in (which can be positive or negative) needs to be sent to each of the other neurons, it needs to be repeated N times, this being accomplished by the bidirectional current mirror in multi-output form . This simply reproduces N copies of the neuron output current in irrespective of what load is presented to it. For adjustments, as may be needed for adaptive ANNs, the g_{mi} can be made as voltage variable by variation of the gain of the associated DVCCS variable bias current.

MOS transistors can be operated such that between the drain and source a resistor is seen whose value depends upon the gate to source voltage, giving a voltage variable resistor useful for adaptation . More commonly the MOS transistor is operated in its saturation mode where instead of a resistor between drain and source a current source is seen, this current source depends on the gate to source voltage in a square law fashion conveniently allowing for quadratic weights. By operating an MOS transistor at very low gate to source voltages, called sub-threshold, exponential behavior is obtained; sub-threshold operation is convenient for low power designs. In all of these the drain current is proportional to the width to length ratio.

Besides the active transistors, capacitors are used to obtain dynamics needed for realization of the ANNs that are described by differential equations. The capacitor are

linear time-invariant (LTI) and satisfy the standard law of the capacitance per unit area of the (gate) oxide used.

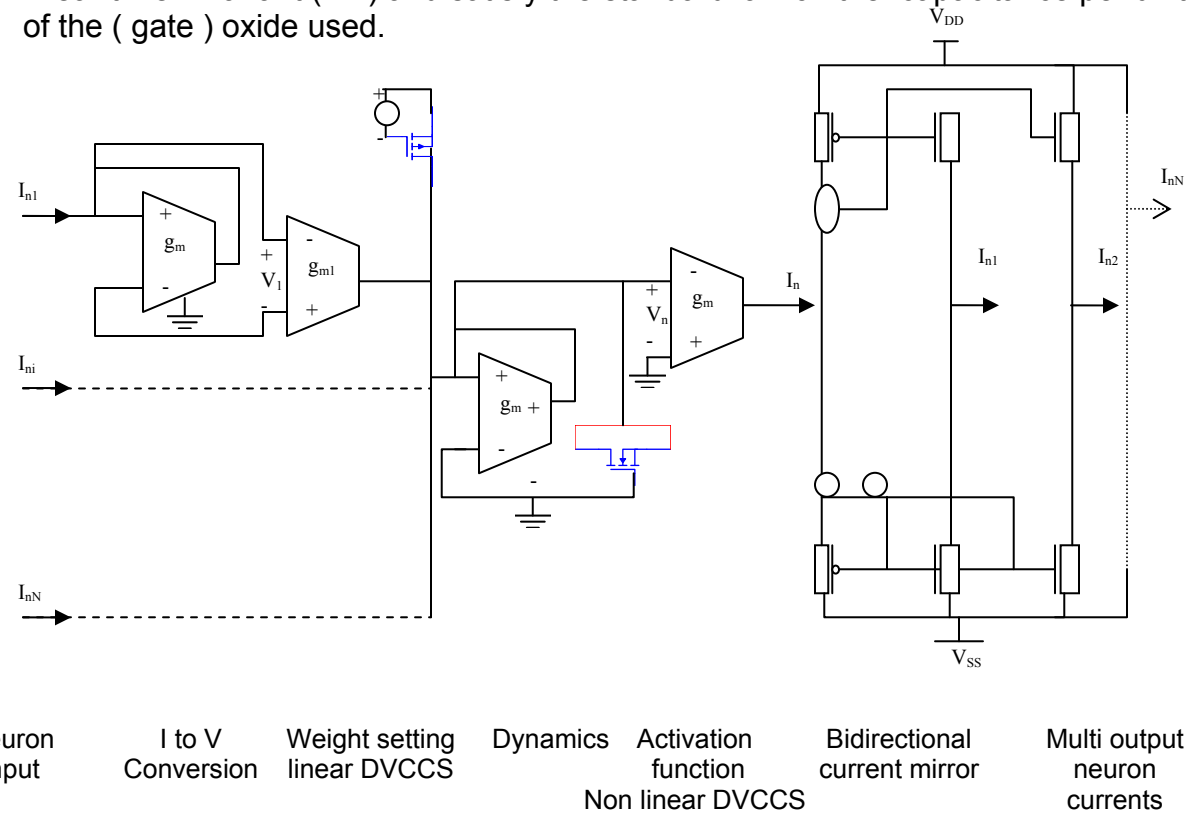

Figure (3): The proposed VLSI realization of the ANN analog circuit

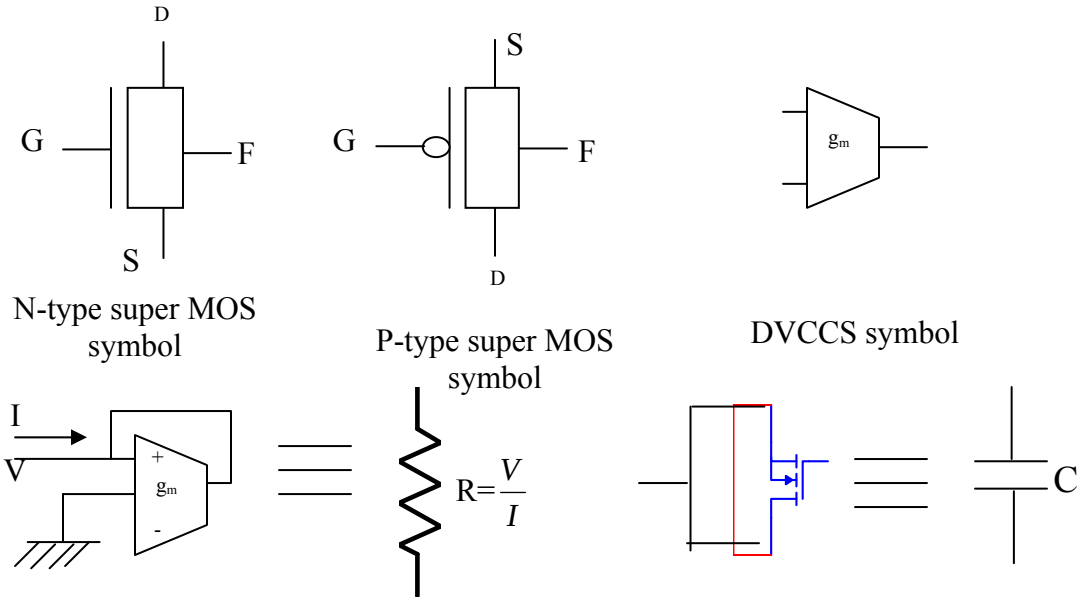

Figure (4) : The equivalent symbols used in the circuit diagrams

The current mirrors allow current to flow only in one direction. However, by placing a P-mirror on top of an N-mirror . we can get a bi-directional current mirror which is convenient for realizing weights . With the steering controlled by the voltage difference of the input voltages, and the current mirrors. We know that the saturation current is:

The trance conductance G of the DVCCS is just the slope of the output current versus the input voltage curve .

$$G=\frac{I_{out}}{V_{in}}=\sqrt{K_p I_{bias}} \quad \text{.....(3)}$$

Notice that the tranceconductace is proportional to the bias I bias, a fact that will become important when the amplifier is used to produce a voltage type output

IV. SIMULATION RESULTS

Figure (4)shows the equivalent symbols used in all circuit diagrams. HSPICE has been used to carry out the different types of analysis . Figure (5) shows the simulated characteristics of a single N-type MOSFET, if the characteristics are extended back into the second quadrant it will meet at the Early voltage which is about 5V (VD = -1/lambda). This effect is important in analog circuits. The simulated characteristics of super MOS has an Early voltage which is several orders of magnitude higher. Also, the super MOS is already saturated at a voltage only slightly above the saturation voltage of one single MOS, indicating a largeR possible output swing. An increase in the output impedance of 300 times Figure (6) gives a transfer characteristics with a given bias current which can be seen to have a transconductance (slope) of about 160 μS.
The AC analysis is shown in figure (7), which gives the same value at low frequency, and is carried out to get the circuit gain and bandwidth which is inherently high in current mode operation.

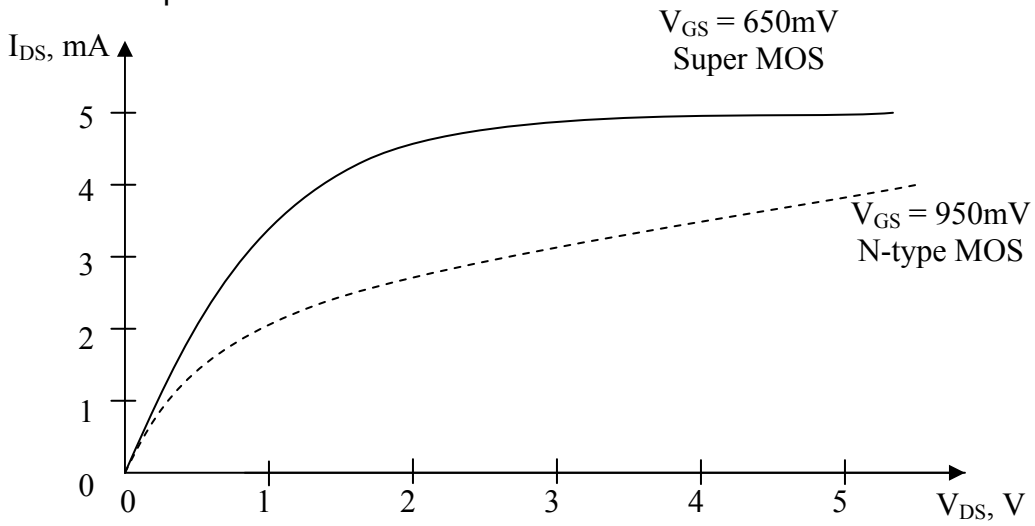

Figure (5): Simulated I_{DS}-V_{DS} characteristics of a single MOS and super MOS (V_{GS} for super MOS is much smaller than V_{GS} for NMOS)

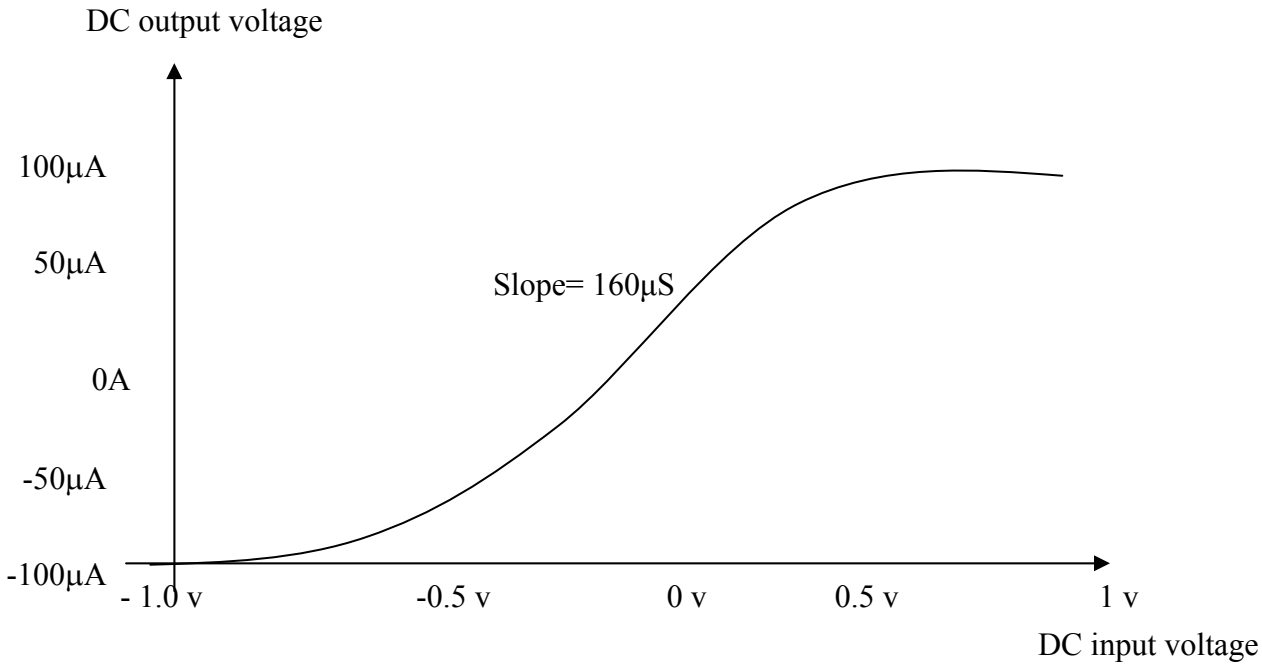

Figure (6): The DVCCS - Transfer function

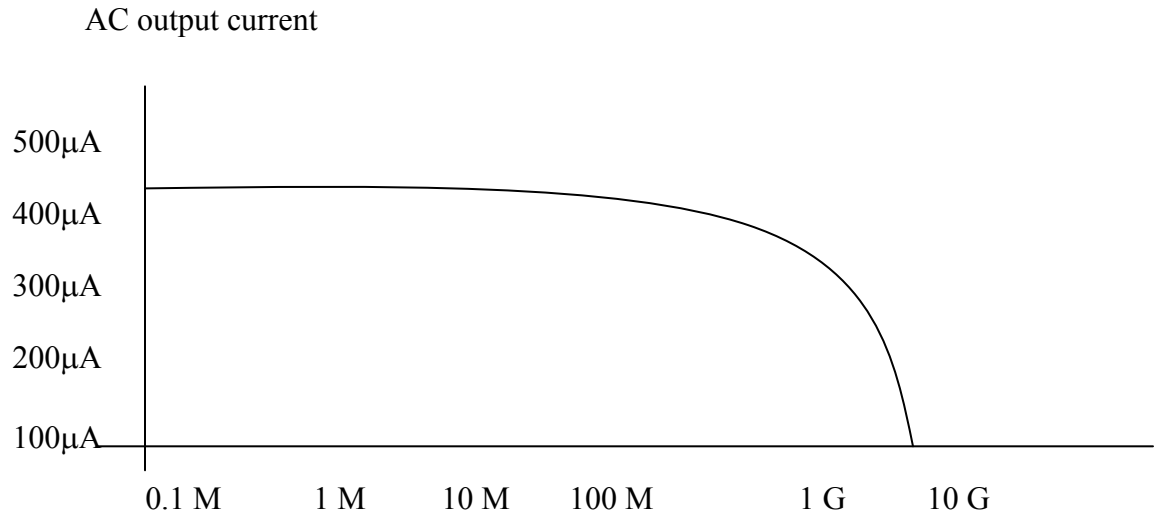

Figure (7) : The DVCCS SIMULATED FREQUENCY RESPONSE

V. CONCLUSIONS

Analog VLSI offers the ANN many advantages of speed and real time processing and the ability to make accurate adjustments for adaptive neural networks. The DVCCS and super MOS current mirrors have a critical tolerance which must be considered. On the other hand, Analog VLSI -Neural Networks represents new technology for a large number of applications involving industrial as well as consumer appliances. This is particularly the case when low power consumption, small size and/or very high speed are required.

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