# A PROPOSED TECHNIQUE FOR FREQUENCY TRANSLATION USING A DIGITAL RADIO FREQUENCY MEMORY

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## ABSTRACT

In this paper a new technique is proposed for frequency translation, based on varying the difference between transmission (ADC) clock frequency and reception (DAC) clock frequency of a digital radio frequency memory. The proposed technique was implemented and tested by the research group and gave satisfactory results.

## KEY WORDS

Frequency translation, carrier suppression, side-band suppression, DRFM.

## NOMENCLATURE

| | |
|---|---|
| $T_J = 2T_{RX} = 2T_{TX}$ | *jamming repetition period of the DRFM* |
| $F_{CR}$ | *the A/D conversion (reception) clock* |
| $F_{CT}$ | *the D/A conversion (transmission) clock* |
| $T_{JS}$ | *jamming strobe duration = total period of continuous jamming* |

## INTRODUCTION

Many modern threats, such as tracking and missile guidance radars apply coherent CW or pulse-Doppler techniques. Even CW search radars and Doppler type radio fuses apply similar techniques. A common feature in all such systems is that the receiver has a very narrow bandwidth; which imposes a stringent condition on any jammer trying to degrade its performance. The permissible tuning error of such a jammer would be too tight to implement. The only practical way is to apply repeater techniques. The

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main function a repeater jammer has to perform for coherent and narrow band jamming generation is frequency translation [1, 10].

Frequency translation is essential to deceive relative speed tracking systems using Doppler frequency-tracking gates. Positive variations of frequency translation values with time lead to velocity gate pull in (VGPI) and negative variation lead to velocity gate pull off (VGPO). Random variation of frequency translation is used to generate narrow band noise jamming.

An ideal frequency translator, given an input signal of a certain frequency, will produce an output signal whose frequency is shifted by some desired amount from that of the input. A maximum of power will be produced at the desired output frequency, and no power will be produced at other, undesired, frequencies [2]. In a practical frequency translator, the output power of the frequency-translated signal is higher than the original frequency residual output by the carrier suppression. It is higher than the unwanted side-band frequency output level by the unwanted side-band suppression. This is schematically shown in Fig. 1.

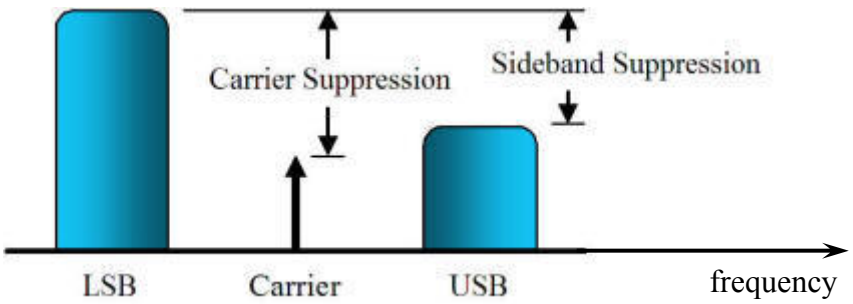


**Fig. 1. Carrier and side-band suppression**

## DEVELOPMENT OF FREQUENCY TRANSLATORS

Early repeater jammers used traveling wave tubes as power amplifiers. They applied a periodic linear time varying voltage on the tube helix to generate a fine controlled translation in the signal frequency. The value of frequency translation was equal to the saw tooth frequency. This technique, called "Serrodyne" [2], was successfully applied in early repeater jammers thirty years ago. Cumming [2] succeeded in 1957 to generate a frequency-translated signal with more than 20 dB carrier suppression. Now the serrodyne principle is used for optical frequency translation [3, 4].

With the development of solid-state systems, it was necessary to implement a compatible technique independent of traveling wave tubes. One of the mostly applied techniques to impose a frequency translation $\Delta\omega$ was the famous quadrature modulator circuit shown in Figure (1). The main idea is to multiply the in-phase signal with $\cos(\Delta\omega t)$ and its quadrature with $\sin(\Delta\omega t)$ and sum the results. The sum will be the frequency translated output. With proper control of amplitudes, more than 35 dB carrier suppression and unwanted side-band

suppression can be achieved. In some references, more than 40 dB suppression was reported [8, 9].

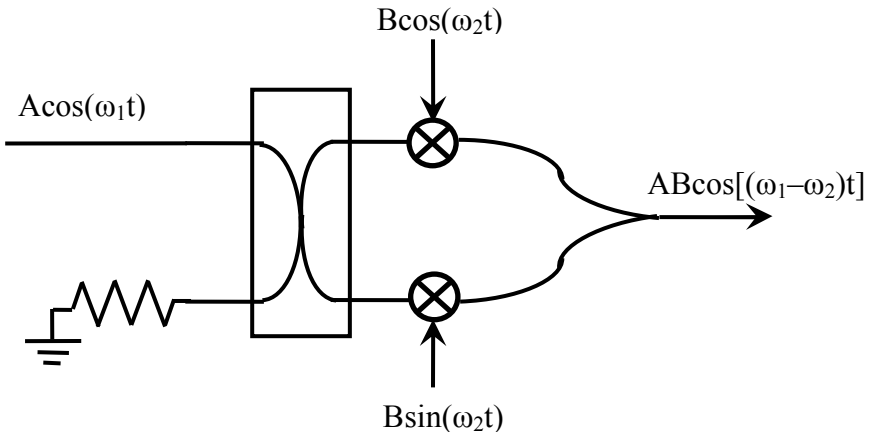


**Fig. 2. Basic Quadrature Modulator Frequency Translator**

In recent years, a big advance occurred in the speeds of A/D and D/A conversion. This led to the application of digital signal processing techniques in modern repeater jammers. Most modern repeater jammers apply digitization techniques to memorize digital samples of the IF signal, from which it is possible to extract the original signal at any time, up convert it to the original RF and generate a coherent jamming output. Any time modulation of the extracted RF signal is possible; which gives a high versatility to such modern jamming systems; the basic unit of which is called the Digital Radio Frequency Memory (DRFM). It is proposed to use a DRFM for frequency translation with theoretically infinite suppression of both carrier and unwanted side band.

## THE IDEA OF THE PROPOSED TECHNIQUE

A DRFM system has been built and tested in the Military Technical College. A detailed explanation of its design and performance is presented in [5]. The above-described Quadrature Modulator technique was applied to translate the frequency of the DRFM output. However, it was noticed the possibility to induce a slight controllable variation in the recovered RF signal with respect to the original one by imposing a slight variation in the DAC clock with respect to the ADC clock. This is the idea of the proposed frequency translation technique which has been studied, designed and implemented by our team.

## DRFM SYSTEM DESCRIPTION

The functional diagram of a typical DRFM system is shown in Fig.3.

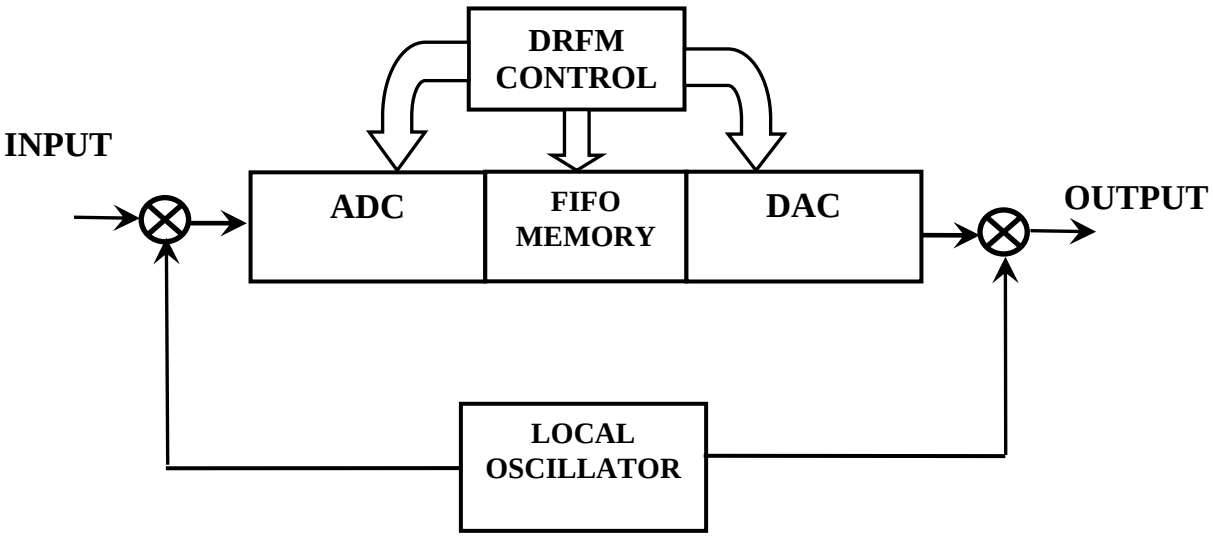


**Fig. 3. DRFM Functional Diagram**

The input RF signal is down-converted by mixing with a certain local frequency $f_L$. The resulting IF signal is filtered with a band-pass filter to reject high order spurs. An analog-to-digital converter is used to get digital samples of the resulting IF signal. The digitization clock frequency is selected such that the highest spectral component of the signal is lower than half the clock frequency [5]. The samples are stored in a First-In-First-Out (FIFO) type memory. The memory size has to be large enough to support the storage of a number of samples equal to the product of the sampling rate by the time frame to be memorized. An Rx/Tx rectangular waveform controls the DRFM operation. The A/D conversion and WRITE processes are done, during Rx periods, at the ADC clock rate $f_{cr}$. The READ and D/A conversion processes are done, during Tx periods, at the DAC clock rate $f_{ct}$. The output of the FIFO memory is taken to a digital-to-analog converter to extract the original IF signal. The D/A converter output is up-converted by mixing with the same LO signal used for down conversion; to guarantee coherence of the output jamming signal.

The number of samples stored during an Rx period is given by:

$$N_s = f_{CR} * T_{RX} = f_{CR} * T_J/2 \qquad (1)$$

## DIGITAL FREQUENCY TRANSLATION

Using the same clock for A/D and D/A conversion we would get exactly the same original frequency.

$$RF_{OUT} = IF_{OUT} + F_L = IF_{IN} + F_L = RF_{IN} \qquad (2)$$

If, however, a certain variation $\Delta f$ is imposed on the D/A clock with respect to the A/D clock; the digital samples are taken from the FIFO memory at a rate higher than that with which they were stored. Consequently, the output

analogue signal of the D/A converter will be regenerated at a rate higher than that of the original A/D converter input. The resulting output IF will be:

$$IF_{out} = IF_{in} + \Delta f \quad (3)$$

*Where* $\Delta f = [F_{CT} - F_{CR}] * (IF/F_c)_{av}$ (4)

$(IF/F_c)_{av}$ *= average ratio between the IF and clock frequencies*

The output RF frequency will be

$$RF_{OUT} = IF_{OUT} + F_L = IF_{IN} + \Delta f + F_L = RF_{IN} + \Delta f \quad (5)$$

If the value of $\Delta$f is varied with time, it is possible to generate any time variation of the output frequency translation.

## GENERATION OF FREQUENCY TRANSLATION PROGRAM

It is possible to generate the law of variation in different ways. Linear or nonlinear increase or decrease with time are all possible. However, the synchronization of the ADC and DAC clocks is a critical process that must be carefully done. Two controllable clock generators can be used, one with a constant control voltage to generate a constant-frequency clock for the ADC and the FIFO WRITE commands. The other has a time varying control voltage to generate a variable-frequency clock for FIFO READ and the DAC commands. To get very small values of $\Delta$f starting from zero, a single clock generator with switched control voltages has to be used to generate both clocks. A waveform generator integrated circuit type MAX038 (U1) was used to generate those clocks as shown in Fig. 4.

It is worth noting that with positive *Δf*, the DRFM extracts all the FIFO memory contents during the Tx period and the FIFO EMPTY flag becomes true before the end of the Tx period. On the other hand, if *Δf* is negative, the number of samples remaining in the FIFO at the end of the first Tx period can be estimated as:

$$N_1 = (F_{CR} - F_{CT}) * (T_J/2) \quad (6)$$

The flag FIFO FULL becomes true after a number of Rx/Tx cycles given by

$$N_C = N_{MAX} / N_1 \quad (7)$$

*where* $N_{MAX}$ *is the FIFO capacity.*

The system designer has to consider that the FIFO should not be saturated during the jamming strobe width; i.e.

$$T_{JS} < N_C * T_J \quad (8)$$

## CIRCUIT DESIGN

In the waveform generator IC, the two waveform control bits (pins 3 and 4) are set at [00] for rectangular output waveform. A fast comparator IC (AD8561) is used as a zero-crossing comparator to shape the symmetrical output of the waveform generator in the TTL format. During the transmission time periods, the waveform generator gets zero voltage at the frequency control input port. Its output frequency is given by the following equations:

$$f_0[MHz] = \frac{I_{in}[\mu A]}{C_{osc}[pF]}$$

*where*

$$I_{in} = \frac{V_{ref}}{R_{in}} \qquad (9)$$

The reference voltage $V_{ref}$ of the MAX038 waveform generator IC = 2.5 [v]. So, $R_2$ = 5 [KΩ] and $C_4$ = 50 [pF] were selected, to get an output clock frequency = 10.04 [MHz]. In order to translate the output frequency with respect to the input frequency; the DAC clock frequency was incremented linearly with time. The linear sweep starts at the beginning of the jamming period, controlled by a jamming strobe pulse. The linear variation is done by a Miller Integrator [the LM124 operational amplifier with feedback capacitance C3 = 100 nF]. With an input rectangular pulse, generated from the jamming strobe, the miller integrator generates a linear sawtooth output voltage. The transistor (Q1) is used to discharge the FeedBack condenser at the end of every jamming strobe as shown in Fig. 5. The coupling circuit [C1, R5 and D1] is used to open the transistor (Q1) at the rising end of the negative jamming strobe pulse. The operational amplifier (U2B) is used as a voltage follower to isolate the load (Q2) from the source (U2C).

The transistor Q2 is used to ON-OFF modulate the control voltage, such that it is zero during Rx periods and enabled during the Tx periods. This transistor is controlled by the Tx/Rx control input gated by the jamming strobe (U3A).

The waveform generator IC (U1) gets a zero frequency control voltage and generates a constant frequency during the receiving periods. The same waveform generator gets a linearly increasing frequency control voltage and generates a sweeping output frequency during the Tx periods. The three gates (U3B, C and D) are used as a digital switch to guarantee that the clock with linearly increasing frequency goes to the Tx1 output while the clock with fixed frequency goes to the Rx output.

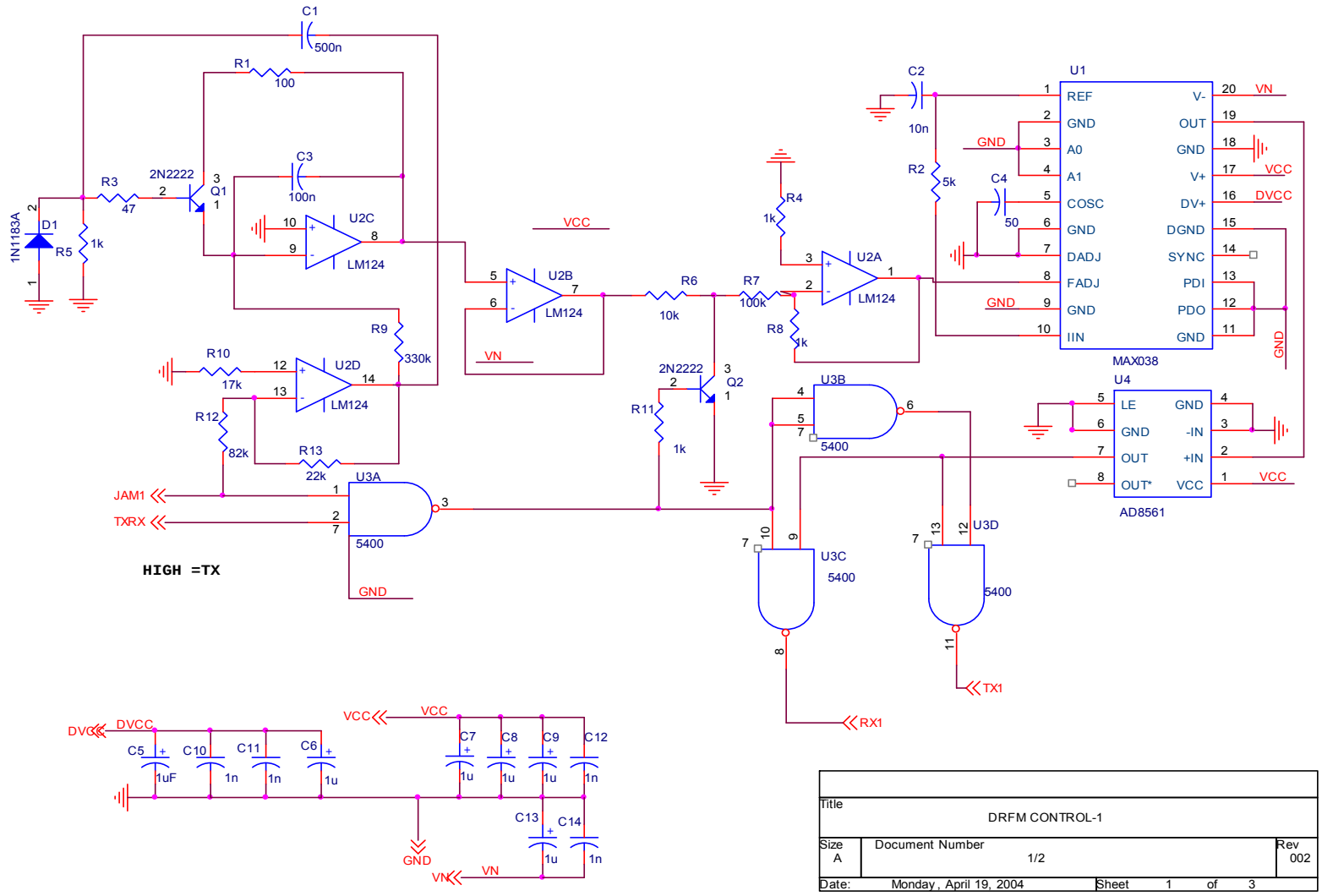


**Fig.4. Local Oscillator Control Circuit**

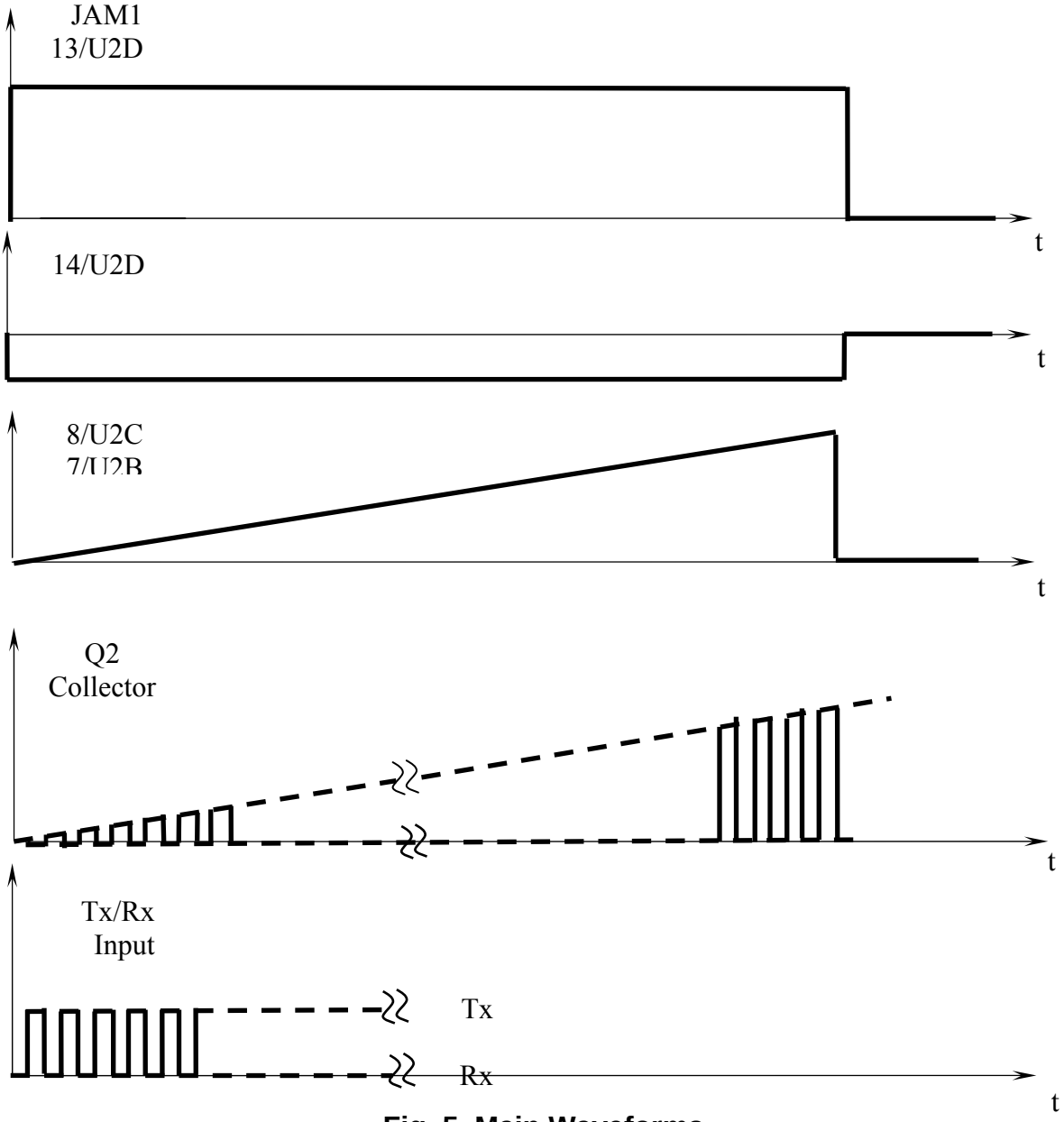


**Fig. 5. Main Waveforms**

## IMPLEMENTATION

The board layout is shown in Figure 6. The Compact PCI standard was applied in the board design and manufacture. The Compact PCI is one of the most advanced technologies for system implementation [10].

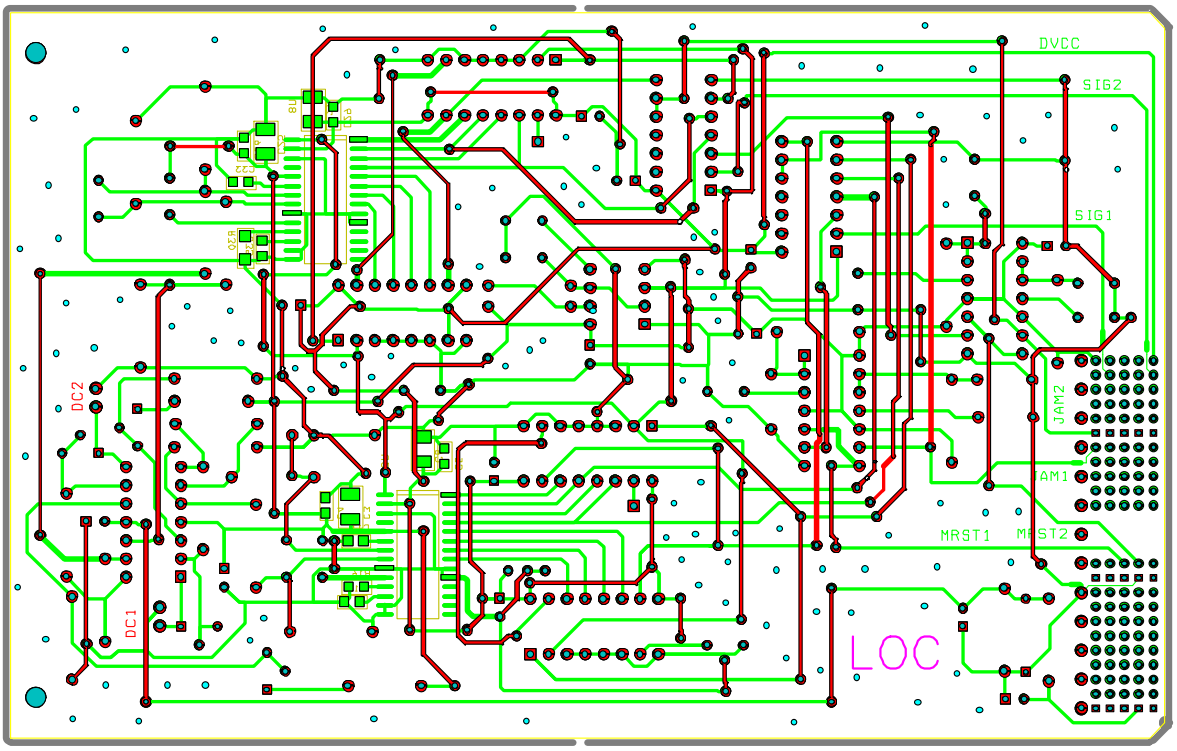


**Fig. 6. Compact PCI Board Layout of the Local Oscillator Control Circuit**

## MEASURED PERFORMANCE PARAMETERS

As described above, the following main parameters have been verified:

- The Rx clock is a TTL periodic signal a fixed 10 [MHz].
- The Tx clock is a TTL periodic signal a rate starting form 10 [MHz] at the beginning of the jamming strobe, and ending with 10 + 0.005 [MHz] at its end.
- The output of the DRFM signal started at the input frequency and gradually swept in frequency with respect to the input by an increment $\Delta f_s$ (t).
- For a 1.4 [MHz] IF signal at the input ADC of the DRFM, the increment $\Delta f_s(t)$ started from zero at the beginning of the jamming strobe and arrived at 0.5 [KHz] at its end.
- No residual carrier frequency was seen at the output.
- No residual lower side-band frequency was seen at the output.

## CONCLUSION

A fine linearly increasing frequency variation has been imposed on the received frequency without any spurs at the output. This variation started from zero and increased up to the desired frequency shift. The fine control on the output frequency enables the user to apply successful velocity gate stealing on coherent radar signals. This frequency translation technique has been implemented by the linear increase of the D/A clock of a digital radio frequency memory (DRFM) while the A/D clock remained constant.

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