

A Single-switch Non-isolated High Gain DC/DC Converter for PV Applications

Arafa S. Mansour¹, Eman M. Sarhan^{2*}, Awad E. El-Sabbe¹, and Dina S. M. Osheba¹

¹Electrical Engineering Department, Faculty of Engineering, Menoufia University, Shebin El-Kom (32511), Egypt.

²Master of Science Candidate
(Corresponding author: esarhan9@gmail.com)

ABSTRACT

In this paper a single switch non-isolated high voltage gain DC/DC converter based on the conventional converter and a switched inductor is introduced. The operation and analysis of the converter in the continuous conduction mode (CCM) and discontinuous conduction mode (DCM), and voltage gain equation derivation are also presented. Also, design of the converter parameters (inductors and capacitor) is given. The proposed converter achieves continuous input current that suitable for PV applications. Also, it is characterized by simplicity of installation and eases of operation which decreases the power losses and gives high overall efficiency. A prototype is made in laboratory to validate the effectiveness of the proposed converter. The proposed converter operation is tested experimentally with static and dynamic load. Also, the performance of the proposed converter is examined with an open loop and closed loop controllers. In addition, a comparison between the proposed converter and other recent converters is also introduced to confirm the merits of this converter.

Keywords: High gain; CCM/DCM; DC/DC converter; switched inductor; PV applications.

1. Introduction

The use of renewable energy source as photovoltaic (PV) cell has been playing a very effective role lately due to the many advantages that it enjoys, such as it is clean and inexpensive energy which makes it widely used in existing networks. But the output voltage of these energies has high fluctuations and a low value. So, to adjust the voltage at the output and convert it to high voltage level, the high gain DC/DC converter is very important to use in these applications [1]. The step-up DC/DC converter can operate in continuous current mode (CCM) and discontinuous current mode (DCM). The CCM is widely popular due to load independent voltage gain, lower current ripple, and better efficiency [2].

To increase the output voltage level, conventional boost converter should increase the switch duty cycle value, and this causes increasing diode reverse recovery issue. Besides, it also limits the voltage gain and increases voltage stress on semiconductor devices (switches and diodes), causing low efficiency. So, conventional boost converters are not proper for high power ranges [3].

There are suitable step-up DC/DC converters that able to overcome the drawbacks of classical boost

converters. These converters can provide high voltage levels with high efficiency at output side suitable for renewable energy applications [4].

Many topologies have been introduced for this purpose [5-17] such as 1) using coupled inductor, 2) using voltage multiplier, 3) using switched capacitor, 4) using cascaded techniques, and 5) switched inductor.

Coupled inductor chooses to use in high gain by increasing inductor turns ratio. But it has the following problems: large input current ripple and high switch voltage spikes because of stored energy of leakage inductance. So, clamp circuit must be used to limit this energy. However, this clamp circuit increases the conduction losses [5-8].

In reference [5] a topology based on coupled inductor is presented with passive clamp circuit and intermediate energy storage capacitor used to increase the output voltage level. But this circuit suffers from using a lot of components that increase the losses and the cost of the system.

References [6-8] presented converters consist of coupled inductors with voltage multiplier (VM) used to multiply the voltage gain. These converters provide high voltage gain with low input current

ripple. However, the VM cells in DC/DC converters that contain coupled inductor decrease the nominal value of power semiconductors as a result of using the clamping circuit that recycles the stored energy of leakage inductance which increases the losses and reduces the overall efficiency.

Reference [9] described topology consists of a switched inductor with double switches to get high gain voltage value. However, using two switches increases the circuit components and thus raises the cost of the system.

References [10, 11] presented proposed converters used a conventional cascaded boost topology based on coupled inductor and diode-capacitor cell that used to suppress the switch voltage spikes resulting from leakage inductance stored energy by recycling this energy to the output side. On the other hand, using diode-capacitor cell as clamping circuit affect the system efficiency due to switching losses of this clamp circuit.

Converters based on the switched-capacitor principle is studied in references [12, 13]. A high voltage gain is achieved, and the switches voltage stresses is reduced. However, the number of components is large, and the output diode voltage stress is high.

Reference [14] described converter uses switched capacitor and a coupled inductor, where the voltage boosted by increasing the turns ratio of the coupled inductor and switched capacitor stage. This converter suffers from high transient current that has degrading effect on both efficiency and power density.

An interleaved DC/DC converter with small input current ripple for large power ranges is discussed in reference [15]. Also, a high step-up interleaved boost converter with switched-capacitors and switched-inductors is studied in [16]. To these circuits operate correctly, the duty cycles of switches should be greater than 0.5, but this led to high power losses and low efficiency.

A converter based on conventional boost and sepic converters is introduced in [17]. A high voltage gain and low current stresses are obtained. However, large number of components is used and in turn increases the cost and the size of the system.

Reference [18] introduced high step-up extendable hybrid DC/DC converter based on two-phase interleaved boost converter and switched capacitor. But this converter did not suitable for high power applications due to high-level of the transient current related to switched capacitor.

The isolated converter topologies such as fly back, forward and push-pull may provide high voltage gain by increasing the transformer turns ratio [19], but this increases the total cost, the weight, and reduces the efficiency.

In this paper, a proposed single-switch DC/DC

converter with switched inductor is presented. The converter operation modes, analysis in CCM and DCM, and designing of circuit parameters are also introduced. A prototype of proposed converter is built in the laboratory and the experimental results with static and dynamic loads are captured. A comparison with other recent topologies is also introduced.

The remainder of the paper is arranged as follows: *Section 2* describes the converter structure, the operation modes, the voltage gain equation derivation in CCM and DCM, and parameters' design methodology. Experimental results are presented in *Section 3*. Also, the comparison study of the proposed converter with other recent converters is shown in *Section 3*. The conclusion is informed in *Section 4*.

2. Converter Description and Operation Modes

As shown in Figure (1), the proposed converter consists of one power switch, one capacitor, two inductors, and four diodes. Inductors L_1 and L_2 are the same. Considering the following assumptions while analyzing the proposed converter: semiconductor components models are ideal, the capacitor voltage stays constant and has small ripple, and the converter operates in the steady state period.

2.1 CCM Operation

The proposed converter operates in two modes for CCM operation. The operation modes and the key waveforms of the proposed converter in CCM are shown in Figures (2 and 3), respectively.

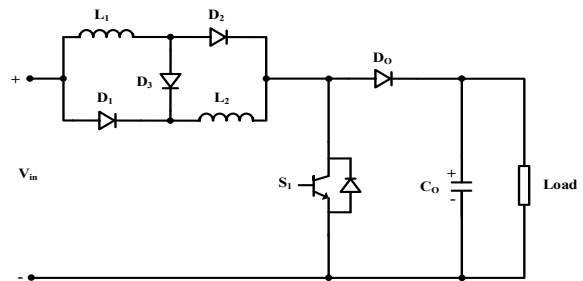
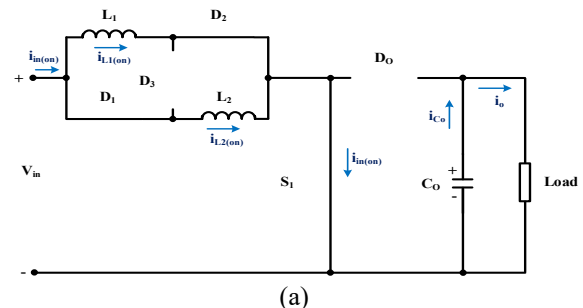


Figure 1- The proposed converter topology



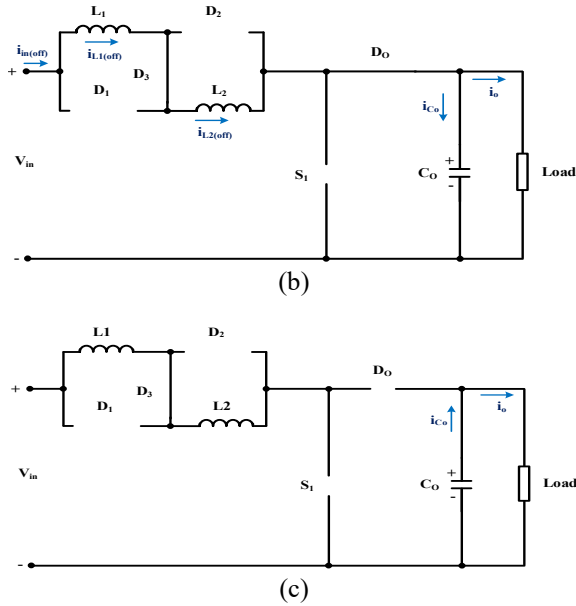


Figure 2- The operation modes of the proposed converter (a) Mode 1, (b) Mode 2, and (c) Mode 3.

2.1.1 Mode 1 (0 – DTs):

In this mode, as shown in Figure (2a), the switch S₁ is in ON condition, the diodes D₁ and D₂ are conducting, and the diodes D₃ and D_o are reverse-biased. The inductors L₁ and L₂ are connected in parallel and charged by the input voltage. The inductors currents increased, and the energy is stored in the inductors. During this mode, the load is fed by the stored energy in the capacitor C_o.

The voltage equations of this mode can be written as follows (assumption: L₁ = L₂ = L)

$$V_{L1} = V_{L2} = V_L \tag{1}$$

$$V_{L(on)} - V_{in} = 0 \tag{2}$$

The current equations related to this mode:

$$i_{L1(on)} + i_{L2(on)} = i_{in(on)} \tag{3}$$

$$i_o = i_{co} \tag{4}$$

2.1.2 Mode 2 (DT_s – T_s):

In this mode, as shown in Figure (2b), the switch S₁ is in OFF condition, diodes D₁ and D₂ are reverse biased, and diodes D₃ and D_o are conducting. The inductors L₁ and L₂ are connected in series and discharge their energy into the capacitor C_o and the load.

The voltage equations of this mode can be written as follows:

$$V_o - V_{in} + 2 V_{L(off)} = 0 \tag{5}$$

The current equations in this mode:

$$i_{L1(off)} = i_{L2(off)} = i_{in(off)} \tag{6}$$

$$i_{L1(off)} = i_{L2(off)} = i_{co} + i_o \tag{7}$$

2.1.3 Voltage Gain Derivation in CCM

The voltage gain derivation is implemented by inductors volt-second balance method as observes.

$$D (V_{L(on)}) + (1 - D) (V_{L(off)}) = 0 \tag{8}$$

Substituting the values of V_{L(on)} and V_{L(off)} from equations (2) and (5), respectively.

$$V_{L(on)} = V_{in} \tag{9}$$

$$V_{L(off)} = 0.5 (V_{in} - V_o) \tag{10}$$

Substituting from equations (2) and (5) into equations (10), the mathematical equation of the voltage gain in CCM is given by:

$$M = \frac{V_o}{V_{in}} = \frac{1+D}{1-D} \tag{11}$$

The maximum switch voltage stress derived from the equation as,

$$V_{sw} = V_{in} - 2 V_{L(off)} \tag{12}$$

By substituting from equation (8) into equation (5) and solving for finding V_{L(off)}, one gets;

$$V_{L(off)} = -\frac{D}{1-D} V_{in} \tag{13}$$

Subsequently the switch voltage stress becomes;

$$V_{sw} = \frac{1+D}{1-D} V_{in} \tag{14}$$

2.2 DCM Operation

The proposed converter operates in three modes for DCM operation. The operation modes and the key waveforms of the proposed converter in DCM are shown in Figures (2 and 4), respectively.

2.2.1 Mode 1 (0 – DT_s): This mode is similar to Mode 1 in CCM, as shown in Figure (2a).

2.2.2 Mode 2 (DT_s – t₁): This mode is similar to Mode 2 in CCM, as shown in Figure (2b).

2.2.3 Mode 3 (t₁ – T_s):

In this mode, as shown in Figure 2c, the switch S₁ still in OFF condition. D₁ and D₂ are still reverse biased, diode D₃ is still forward bias, while D_o is non-conducting. No current follows in the inductors L₁ and L₂. The load is fed by the stored energy in the capacitor C_o.

The steady state voltage equation for this mode is:

$$V_o = V_{Co} \tag{15}$$

The current equation for this mode in this mode:

$$i_o = i_{co} \tag{16}$$

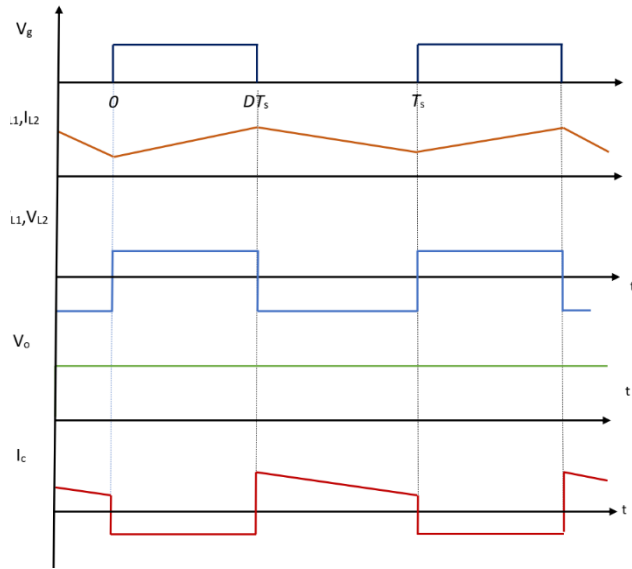


Figure 3- The typical key waveforms of the proposed converter in CCM

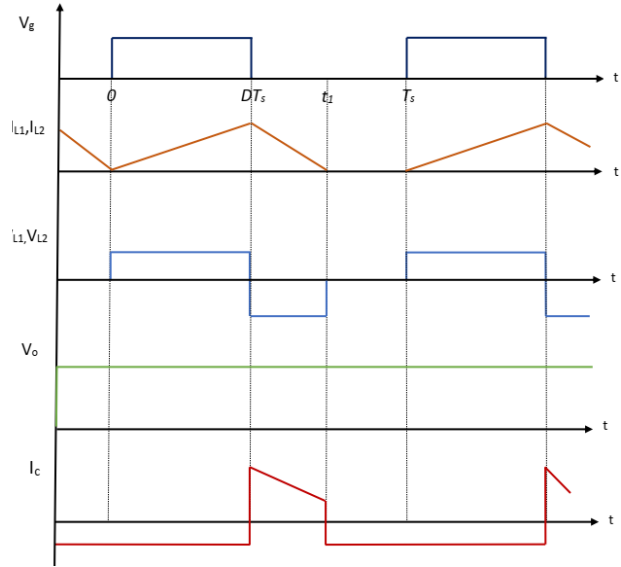


Figure 4- The typical key waveforms of the proposed converter in DCM

2.2.4 Voltage Gain Derivation in DCM

The voltage gain derivation is implemented by inductors volt-second balance method.

$$D (V_{L(on)}) + 0.5 (1 - D) (V_{L(off)}) = 0 \quad (17)$$

Substituting the value of $V_{L(on)}$ and $V_{L(off)}$ from equations (2) and (5), respectively.

$$V_{L(on)} = V_{in} \quad (18)$$

$$V_{L(off)} = 0.5 (V_{in} - V_o) \quad (19)$$

Where the DCM condition operates only in half period of the OFF condition. The mathematical equation of the voltage gain becomes:

$$M = \frac{V_o}{V_{in}} = \frac{1+3D}{1-D} \quad (20)$$

The maximum switch voltage stress can be obtained from the equation;

$$V_{sw} = V_o = \frac{1+3D}{1-D} V_{in} \quad (21)$$

2.3 Design Methodology

Inductors and capacitor design depend on their currents and voltages.

2.3.1 Inductor Design

From the key waveforms and operation modes, the inductor can be estimated by equation:

$$V_L = L di/dt \quad (22)$$

By integrating equation (22), the inductor value can be calculated as in (23).

$$L = (V_L * D T) / (\Delta I_L) \quad (23)$$

Where ΔI_L is the inductor ripple current allowed. It's value equal to 20 to 40 percent of the output current according to IEEE standard.

At on state of the switch $V_L = V_{in}$, and the inductor value can be found according to equation (24);

$$L = (V_{in} * D) / (f_s * \Delta I_L) \quad (24)$$

Where f_s is the switching frequency.

2.3.2 Capacitor Design

The capacitor value can be found by:

$$I_o = C_o dv/dt \quad (25)$$

By integrating equation (25), the minimum output capacitor value (C_o) value can be determined by equation (26).

$$C_o = (I_o * D) / (f_s * \Delta V_o) \quad (26)$$

Where the output voltage ripple value as in equation (27).

$$\Delta V_o = 3.8\% \text{ to } 5\% \text{ of } V_o \quad (27)$$

3. Experimental Results

To validate the proposed converter efficacy, a hardware prototype is carried out in the laboratory. The results are captured using the oscilloscope and DSP 1104 during open-loop and closed-loop control, respectively. The circuit parameters are given in Table (1). The effectiveness of the proposed converter is tested under open-loop and closed-loop control. Experimental results are introduced as the

following scenarios: 1) open loop performance (CCM/DCM), 2) closed loop performance (static load/dynamic load).

Table 1- Circuit parameters

| Open-loop Control (CCM/DCM) | | | Closed-loop Control | |
|-------------------------------|--|--------------|---|-------------|
| Parameter | | Value | Parameter | Value |
| Input Voltage (V_{in}) | | 24 V | Inductances (L_1, L_2) | 10mH |
| Load (R) | | 550 Ω | Capacitance (C_o) | 330 μ F |
| Capacitance (C_o) | | 330 μ F | Static Load | |
| Duty ratio (D) | | 0.6 | Proportional gain (K_P) | 100 |
| Switching frequency (f_s) | | 1 KHz | Integral gain (K_i) | 200 |
| CCM | | | Dynamic Load (Separately excited dc motor) | |
| Output Voltage (V_o) | | 93 V | Rated armature current (I_a) | 1 A |
| Inductances (L_1, L_2) | | 25 mH | Rated armature voltage (V_a) | 50 V |
| DCM | | | Rated field voltage (V_F) | 50 V |
| Output Voltage (V_o) | | 162 V | Proportional gain (K_P) | 98.6 |
| Inductances (L_1, L_2) | | 10 mH | Integral gain (K_i) | 215 |

3.1 During Open-loop Control

3.1.1 CCM Performance

Figure 5 shows the waveforms of the input and output voltages. As shown the input voltage value is equal 24 V, and the output voltage value is equal about 93 V that represents 3.8 times of input voltage. Figure 6 displays the waveform of input current that ensures the continuity of the current for the proposed circuit. Figure 7 shows the waveforms of inductor voltage and current and validates the proposed circuit operation in CCM.

The waveforms of gate-emitter and switch voltages are shown Figure 8. It indicated from Figure 8 that the proposed circuit operates at 0.6 duty ratio. Also, the switch voltage stress is not exceeding the output voltage that validates the theoretical analysis.

To confirm the validity of the voltage equation, Figure 9 is introduced. It compares between the voltage gain taken experimentally and derived theoretically at different duty ratios. It is clear that there is a high convergence between the obtained results.

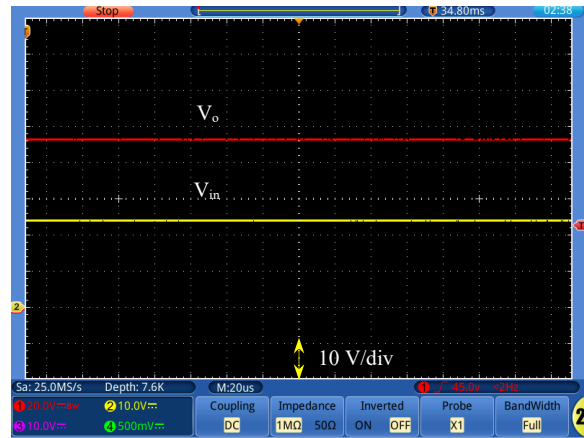


Figure 5- Waveforms of input and output voltages in CCM



Figure 6- Waveform of input current in CCM

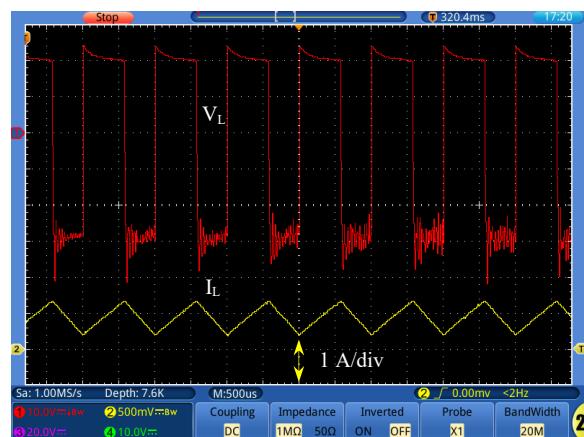


Figure 7- Waveforms of inductor voltage and current in CCM

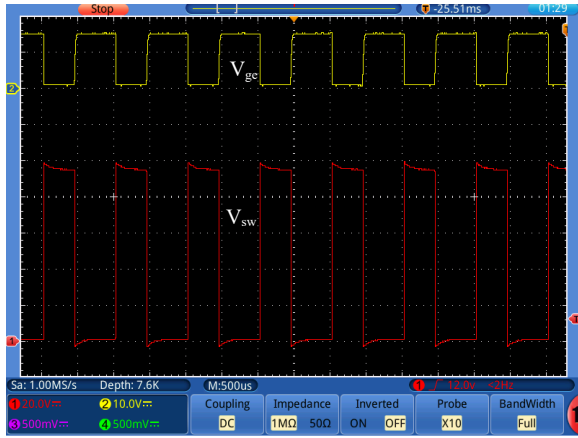


Figure 8- Waveforms of gate-emitter and switch voltages in CCM

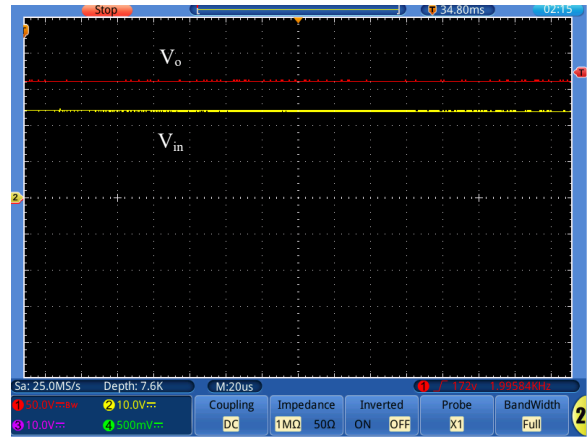


Figure 10- Waveforms of input and output voltages in DCM

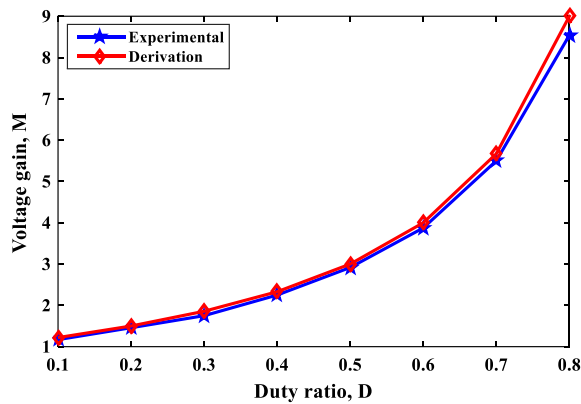


Figure 9- Voltage gain versus duty ratio in CCM

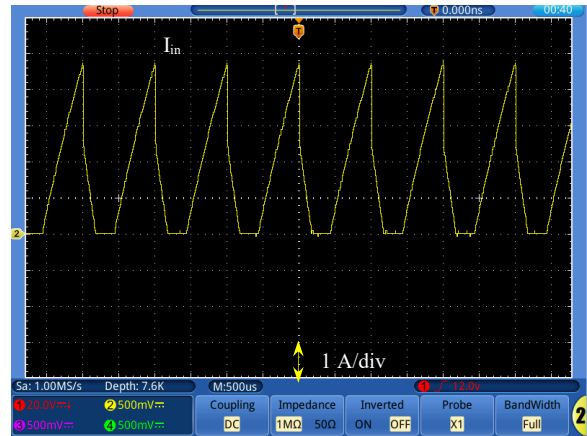


Figure 11- Waveform of input current in DCM

3.1.2 DCM Performance

The experimental results of the proposed converter in DCM operation are presented in Figures (10-14).

The waveforms of input and output voltages are shown in Figure 10. The output voltage value is equal 162 V that represents 6.75 times of input voltage. The discontinuous input current waveform is shown in Figure 11.

The waveforms of inductor voltage and current are shown in Figure 12. The inductor current is discontinuous that proves the operation of the proposed circuit in DCM.

Figure 13 shows the waveforms of gate-emitter and switch voltages, respectively. It's clear from Figure 13 that the average voltage across the switch is less than the output voltage that means low stress across the switch.

The relation of voltage gain versus duty ratio in DCM is shown in Figure 14. It also shows the convergence of the results and the validity of the derived equation.

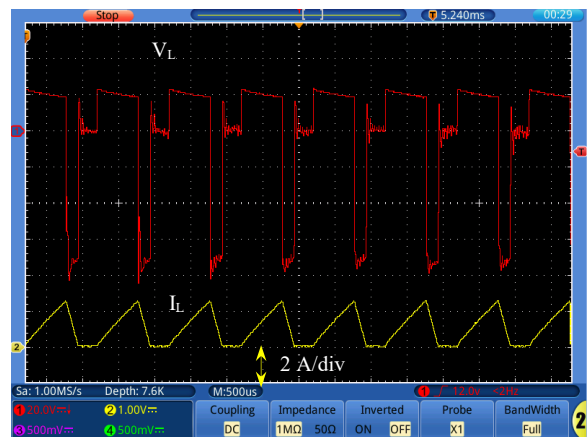


Figure 12- Waveforms of inductor voltage and current in DCM

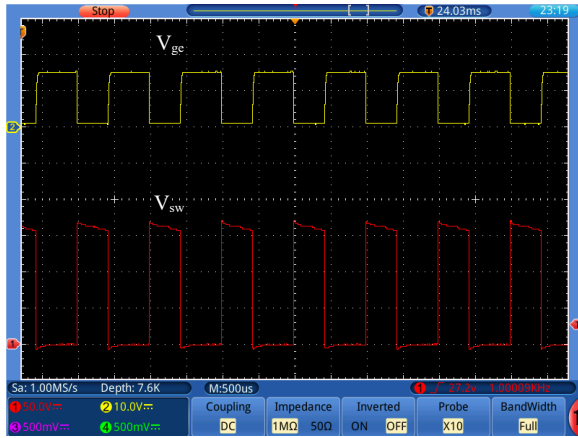


Figure 13- Waveforms of gate-emitter and switch voltages in DCM

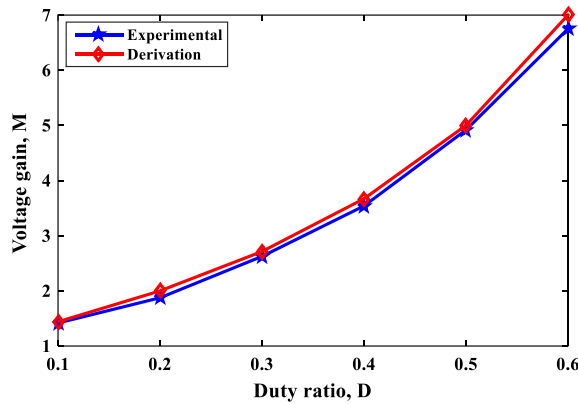


Figure 14- Voltage gain versus duty ratio in DCM

3.2. Closed Loop Analysis

3.2.1 Static Load

The proposed converter is tested under closed loop control with static load (resistive load). The converter performance is studied under changing of load, input voltage, and reference voltage as shown in Figures 15-17, respectively.

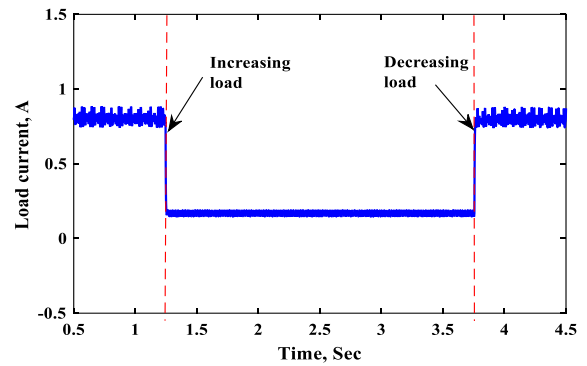
The waveforms of reference and output voltages, and load current during changing of the load are shown in Figure 15. With the reference voltage equal to 50 V, two load changing are introduced. At the instant $t = 1.248 \text{ sec}$, the load resistance increased from about 25% of the rated load to the rated value. So, the load current decreased by the same ratio. At the instant $t = 3.75748 \text{ sec}$, the load resistance decreased from the rated load to about 25% of the rated value again.

The waveforms of input voltage, and reference and output voltages during changing of the input voltage are shown in Figure 16. With reference voltage equal to 50 V, the input voltage is increased from 22 V to 35 V then some time the input voltage is reduced to 22 V again.

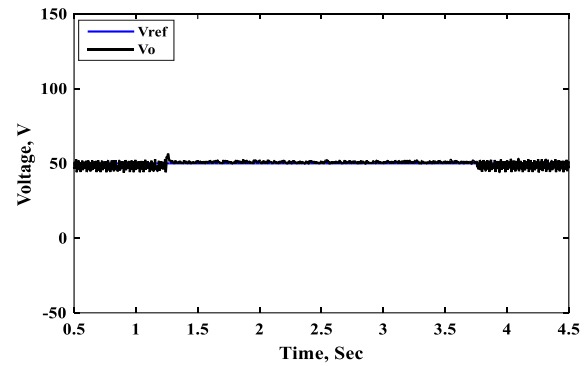
The waveforms of reference and output voltages during changing of the reference voltage are shown

in Figure 17. At the instant $t = 1.266 \text{ sec}$, the reference voltage decreased from 100 V to 70 V then at the instant $t = 2.67 \text{ sec}$, the reference voltage increased to 100 V again.

As evidenced by the experimental results in Figures 15-17, even with these rapid and strong variations in load, input voltage, and reference voltage, the output voltage still constant and robustness against these variations.

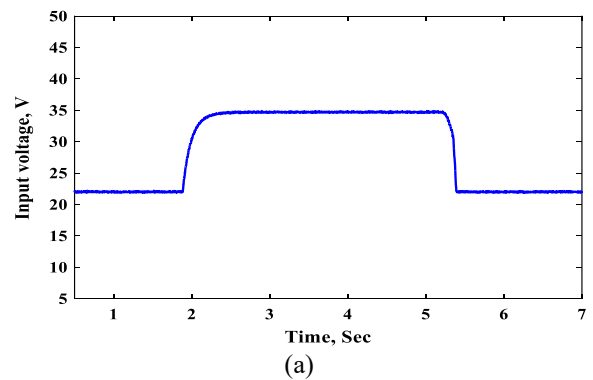


(a)



(b)

Figure 15- Waveforms of (a) load current, and (b) reference and output voltages during the load changing.



(a)

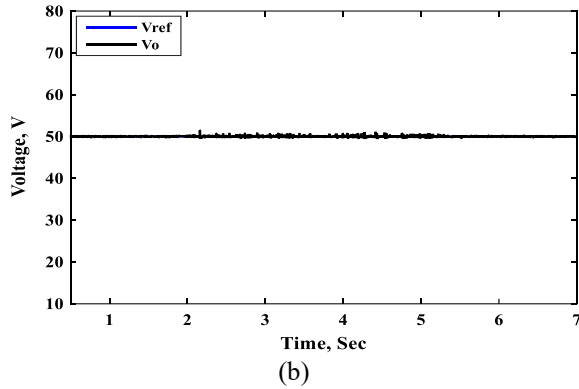


Figure 16- Waveforms of (a) input voltage, and (b) reference and output voltages during the input voltage changing.

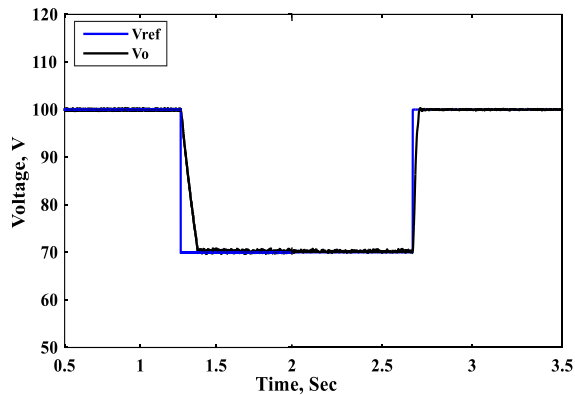


Figure 17- Waveforms of reference and output voltages during the reference voltage changing.

3.2.2 Dynamic Load

The performance of the proposed converter is also tested when it supplied a separately excited dc motor under armature voltage control. The field winding of the motor is supplied from a constant dc supply with 25 V. The armature winding is supplied from the proposed converter.

To show the effectiveness of the proposed converter to drive the motor effectively, the results shown in Figure 18 are presented. With a load torque equal to 50% of the motor torque, the motor operates at armature voltage equal 35 V and speed equal to 1300 rpm. At the instant $t = 2.3 \text{ sec}$, a step change in the reference armature voltage from 35 V to 40 V is introduced so, the motor speed responds to this change and increases to 1500 rpm. Then when a step change in the reference armature voltage from 40 V to 35 V is introduced at the instant $t = 5.92 \text{ sec}$, the motor speed responds to this change and decreases to 1300 rpm.

Also, with the reference armature voltage equal to 45 V, a motor load torque step changing from no-load to 40% of the motor torque is introduced at the instant

$t = 3.37 \text{ sec}$ in Figure 19. As result, the motor speed decreases from 2200 rpm to 1800 rpm while the armature voltage still follows the reference voltage.

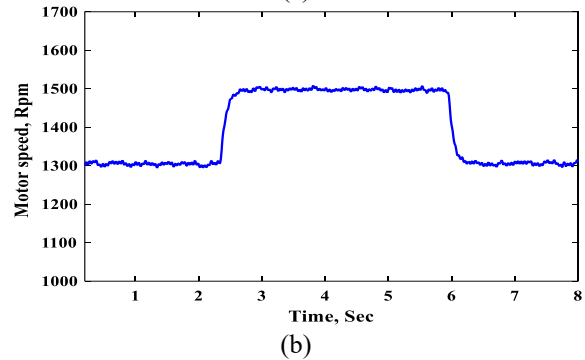
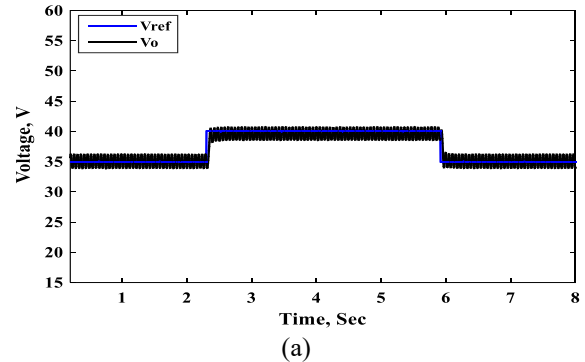


Figure 18- Waveforms of (a) reference and output voltages, and (b) motor speed during the reference armature voltage changing.

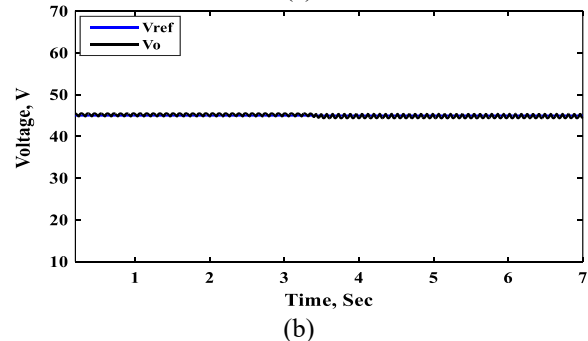
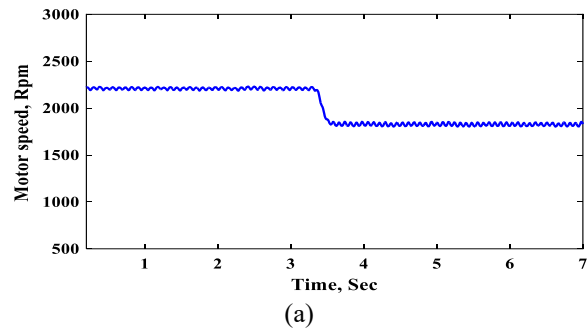


Figure 19- Waveforms of (a) motor speed, and (b) reference and output voltages during the motor load torque changing.

Table 2- Comparing the proposed converters with other recent topologies

| Converter Type | Conventional boost | Conv. [5] | Conv. [8] | Conv. [10] | Conv. [17] | Proposed |
|---|--------------------|-------------------------------|-------------------------------|-----------------------------------|---------------------|---|
| No. of switches | 1 | 1 | 2 | 1 | 2 | 1 |
| No. of inductors | 1 | 2 | 4 | 3 | 3 | 2 |
| No. of capacitors | 1 | 3 | 4 | 4 | 3 | 1 |
| No. of diodes | 1 | 3 | 2 | 5 | 2 | 4 |
| Voltage gain equation | $\frac{1}{1-D}$ | $\frac{2}{1-D}$ $n=1, k=1$ | $\frac{1}{1-D}$ $n=1, k=1$ | $\frac{2(1+D)}{(1-D)^2}$ $n=1$ | $\frac{D}{(1-D)^2}$ | in DCM $\frac{1+3D}{1-D}$ in CCM $\frac{1+D}{1-D}$ |
| Switch voltage stress | V_o | $0.5 V_o$ | V_o | $0.5V_o/(1+D)$ | V_o/D | V_o |
| Output diode (D_o) voltage stress | V_o | $0.5 V_o$ | V_o | $V_o/(1+D)$ | V_o/D | V_o |
| Output capacitor (C_o) voltage stress | V_o | V_o | V_o | V_o | V_o | V_o |

n and k are the turns ratio, and the coupling coefficient of the coupled inductor, respectively.

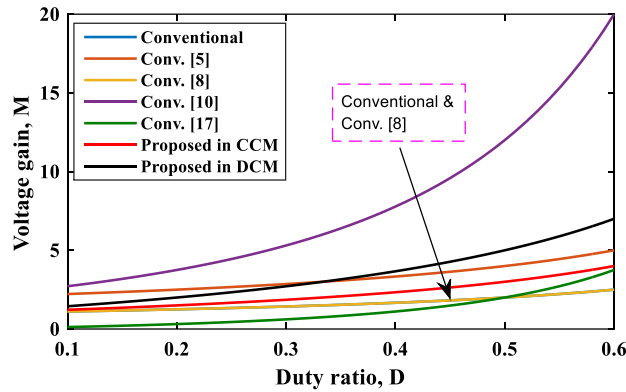


Figure 20- Voltage gain versus duty ratio.

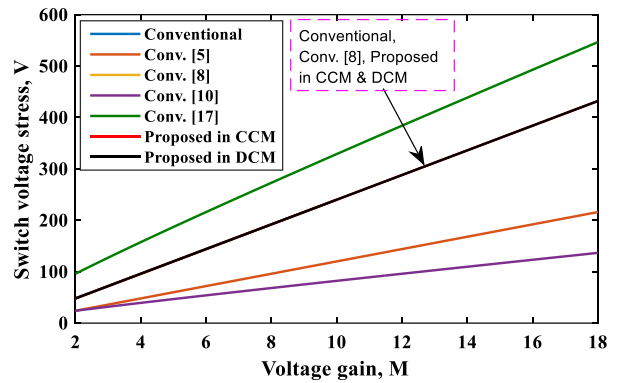


Figure 21- Maximum switch voltage stress versus voltage gain at $V_{in} = 24$ V.

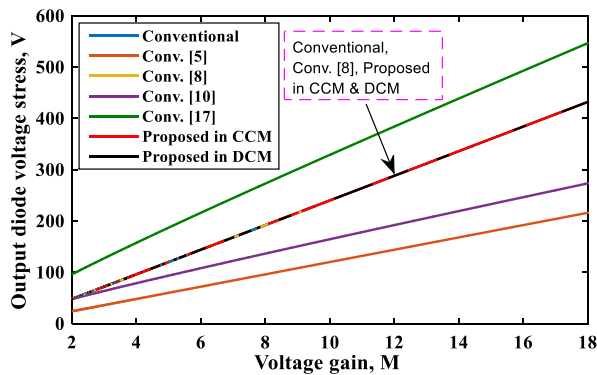


Figure 22- Maximum output diode voltage stress versus voltage gain at $V_{in} = 24$ V.

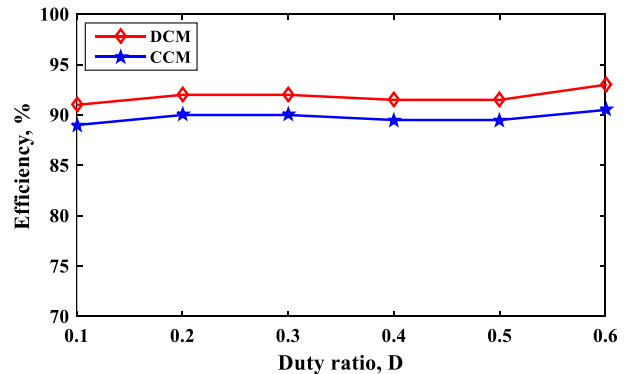


Figure 23- Efficiency of the proposed converter versus duty ratio.

3.3 Comparative Analysis

In this section the proposed converter compared with other recent converters in terms of number of switches, number of inductors, number of capacitors, number of diodes, voltage gain equation, and switch and output diode voltage stresses as in Table (2).

As described in Table 2, the proposed converter has the least components count compared to the other converters in [5], [8], [10] and [17]. Also, for the modest duty ratios the proposed converter has the larger gain compared with the conventional, conv. [5], conv. [8], and conv. [17] except conv. [10] that has the largest voltage gain as shown in Figure 20. However, conv. [10] needs high output capacitor value that increases the volume and cost of the converter.

The maximum voltage stresses across power switches of the converters are compared as shown in Figure 21. The maximum switch voltage stresses of the conventional, conv. [8], and proposed are equal. The maximum switch voltage stresses of the proposed is lower than conv. [17], but it higher than conv. [5] and conv. [10]. The maximum output diode voltage stresses of the converters are displayed in Figure 22. Conv. [17] has the highest value, while conv. [5] has the lowest value. The maximum output diode voltage stress of the proposed converter is equal to the conventional and conv. [8]. Based on these comparisons, the proposed converter has good performance.

3.4 Converter Efficiency

The converter efficiency is measured at different duty ratios and the result is shown in Figure 23. The efficiency is higher when the converter operates in DCM. The maximum efficiency that the converter reaches is 93 % at $D = 0.6$.

4. Conclusions

In this manuscript, a proposed DC/DC converter with high voltage gain has been introduced. The operation modes of proposed converter in the CCM and DCM have been analyzed and discussed. Also, the voltage gain equation has been derived in both the CCM and DCM. A prototype has been built in the laboratory to emphasize the proposed converter effectiveness. The proposed converter has been tested under open loop and closed loop performance, and the experimental results are captured. The performance of the proposed converter has been compared with other recent converters and it was found that it has good performance. Finally, the proposed converter can be used in renewable energy applications.

5. References

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