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MODELING THE AGC OF A HOMING MISSILE RECEIVER AS AN AID FOR ECM EVALUATION

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ABSTRACT

In this paper a proposed mathematical model is formulated and analyzed for the automatic gain control subsystem of a hostile radar homing missile receiver. The model is intended for evaluating an angular deception jamming technique called "AGC DECEPTION". The analysis of this technique needs a real-time laboratory model that responds to external excitations in exactly the same way as the original AGC subsystem does. The author has designed, realized and tested an analogue circuit model; upon which the proposed jamming technique can be applied and optimized for maximum effectiveness. This paper is interested only in the modelling process and the extent to which the author's model; drawn in Fig. 9, resembles the original missile AGC subsystem. With the proposed simulation technique every RF or video signal parameter is represented as a DC variable voltage that can be easily measured in real time on an oscilloscope.

NOMENCLATURE

A_{av_i} = *average input amplitude [v]*
$\alpha(t)$ = *instantaneous angle between target direction and antenna boresight*
$F\{\alpha(t)\}$ = *the AM function due to the antenna directional characteristics.*
ω_{IF} = *Intermediate angular frequency of the missile receiver.*
v_o = *output DC voltage*
G_{IF} = *Intermediate frequency amplifier gain*
K_d = *detector voltage sensitivity*
G_v = *the video amplifier gain*
e_d = *the AGC delay voltage [v]*

INTRODUCTION: TYPICAL AGC CHARACTERISTICS

The AGC deception technique consists in a periodic ON-OFF switching of the jamming signal at such rates that the hostile receiver is either cut-off or saturated

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most of the time. Our goal is to design and evaluate a real-time analogue model to be used for optimizing the On and OFF periods of this deception technique.

Fig.1-A shows a simplified functional diagram of the missile receiver AGC. The following equations describe the steady-state system operation. The video output voltage is given by :-

$$v_O = A_{avi} \cdot F\{\alpha(t)\} \cdot G_{IF} \cdot K_d \cdot G_v \qquad (1)$$

where

$$G_{IF} = G_{max} \text{ [dB]} \quad \text{for } v_O \le e_d$$

$$= G_{max} - B.(\bar{v}_O - e_d) \quad \text{for } \bar{v}_O \ge e_d \qquad (2)$$

B = *a proportionality constant of the gain regulation characteristic.*

e_r = *a reference voltage; selected such that :*

$$G_{IF} = G_O - B.(\bar{v}_O - e_r) \quad \text{for } \bar{v}_O \ge e_d$$

$10\log(e_r/e_d) \approx$ *half the output dynamic range* (3)

G_O = *the nominal IF gain at the centre of the gain regulation characteristic*

Fig.1-B shows the steady state dependence of G_{IF}[dB] on the average DC output voltage which is allowed to vary within a very small range (±1 [dB] in this example) due to the AGC action. **Fig.1-C** shows the regulated input-output characteristic of the AGC system. It is the relation between the steady state average output voltage v_{avo} [v] and the average input amplitude logarithm [20log(A_{avi})] [dB]. In the same figure the saturation level of the output voltage {$v_{sat} \approx 3e_d$} and the cut-off level v_{co} are depicted. The video amplifier is saturated at IF amplitudes $> v_{sat}/(k_d.G_v)$. The envelope detector; due to its detection threshold, can not sense any IF amplitude lower than $v_{co}/(k_dG_v)$. **Fig.1-D** shows the dependence of G_{IF} on the average input voltage; which is the feed back loop characteristic.

In these figures we concentrate on four important points of the regulation characteristics :

Point A where the average output voltage = 0 corresponding to a zero average input amplitude [20log(A_i/A_d)$\rightarrow -\infty$]. The system gain is set to its maximum value.

Point B where the average output equals the delay voltage e_d. The gain is still equal to G_{max}. Note that the region AB of the characteristics represents the locus of equal gain points.

Point C; the centre of the regulation characteristic, where the IF gain equals G_o and the average output equals the reference voltage $e_r \cong 1.22\ e_d$. Given a 90 [dB] input dynamic range; the ratio $20\log(A_i/A_d) \cong 45$ [dB] for this point.

Point D: the end of the AGC dynamic range, where $20\log(A_i/A_d)$ = the full receiver dynamic range [90db in this example] and the IF gain = $G_{\min}$.

ANALOG CIRCUIT SIMULATION OF THE AGC SYSTEM.

An analogue circuit model has been specified, designed and implemented to predict exactly the complete transient and steady state behaviour of the AGC loop in different cases. The model has been intended for:

a. measuring some characteristics which are difficult to calculate
b. studying the system behaviour with different input waveforms
c. verifying the theoretically derived formulae for jamming effectiveness
d. optimizing time parameters of the proposed jamming technique.

AGC Model Specification :-

My study of a typical missile receiver resulted in the following AGC specifications:-
- The characteristic impedance of all RF stages is 50 [Ohms].
- The input signal varies between -120 and -30 [dBm].
- The mixer conversion loss is 7 [dB]; leading to a -127 to -37 [dBm] IF input level.
- The corresponding regulated IF output varies between -17 and -15 [dBm].
- The IF saturation level is 9 [dB] above the central regulated level, and the minimum detectable level is 4.8 [dB] below the central regulated level.
- The maximum IF gain is 110 [dB] and its minimum value is 22 [dB].
- The IF gain regulation characteristic can be approximated by the following formula:

G = 110 [dB] *for input power <-120 [dBm]*

$G = G_o + B.v_c$ *for input power >-120 [dBm]* (4)

where

G_o = 63.68 [dB]

B = 126.44 [dB/v]

V_C = $e_r - \overline{v_O}$

- *The AGC time constant* τ_{AGC} = *200 [m.sec.]; resulting in a feed back filter half-power point* $\omega_h \cong$ *5 [rad/sec].*
- The AGC reference voltage $e_r \approx 3[v]$

Choice of the Circuit Model :-

The AGC loop of interest can be represented by 4 main blocks :-

1. The AGC amplifier; having an input regulated dynamic range of 90 [dB] and a corresponding 2 [dB] output dynamic range. Fig.2 shows the IF gain vs the control voltage characteristic of this amplifier.

2. A single block with a certain gain, a certain saturation level and a certain detection threshold to represent all the circuits following the IF amplifier including the

detector.

- The IF voltage level corresponding to -16 [dBm] is 50 [mv]. The input IF amplitude causing saturation is 141.6 [mv] and the minimum detectable IF level is 28.6 [mv].
- For any IF amplitude < 28.6 [mv] the output DC = 0.
- For any IF amplitude > 141.6 [mv]; the output DC will be = 8.49 [mv].

Fig.3 shows the input-output characteristic of this block.

3. A Low Pass Filter, having the same frequency response of the original FB filter.

4. A unity gain differential amplifier to compare the output voltage (v_o) with the reference value (e_r)and produce the gain control voltage (v_c).

Simulation of the AGC IF Amplifier :-

Referring to the regulation characteristic of this amplifier; we notice that it has a minor nonlinearity. The slope $\partial G_{IF}/\partial v_c$ decreases slightly from 133.3 [dB/v] at the beginning of the dynamic range to 120 [dB/v] at its end. It has been approximated to the following formula:

$$G\,[dB] \cong \begin{cases} 110 & \text{for small values of } v_c \\ 126.44\,(0.504 + v_c) & \text{for higher values of } v_c \end{cases} \qquad (5)$$

which has been simulated by the simple circuit of **Fig. 4;** including a limiter set at +11 [v]. It is evident that the IF amplifier gain has been simulated by a DC voltage that can be measured and plotted.

For 50 Ohm input impedance ; it can be shown that the average input IF signal level [dBm] is :

$$S_{I_{av}} = 10\log\left(\frac{A_{av_i}^2}{2 * 50\Omega}\right) + 30 = 20\log A_{av_i} + 10 \ [dBm] \qquad (6)$$

from which $A_o = v_m * 10^{\left(\frac{S_I + G_{IF} - 10}{20}\right)}$ (7)

If we introduce an input voltage $v_M = F\{\alpha(t)\}$ to the input of a 6 [dB] gain logarithmic amplifier, sum its output to the sum of $0.1\left(S_{I_{av}} + G_{IF}\right) = 2\log(A_{av_O})$ and introduce the sum to the input of an anti-log amplifier; the AGC amplifier can be simulated by the circuit shown in **Fig.5**.

Simulation of the Linear Amplifier-Detector Block :-

The characteristic of this block; shown in **Fig.3** has been simulated with the circuit shown in **Fig.6.** The comparator is used to simulate the cut-off for signals under the detection thtreshold, while the saturation is simulated with the two FB diodes.

Simulation of the Feedback Filter :-

It is a single time constant (200 [ms]) low-pass filter. An additional band-reject effect for specific frequencies has also been simulated in the realized model (not shown in this paper for lack of space).

The Complete AGC Analog Simulator :-

The complete circuit diagram that has been designed and implemented by the author is shown in **Fig.9**.

VERIFICATION OF THE CIRCUIT OPERATION

Measurement of the IF Amplifier Simulator :-

These measurements have been done with open FB loop. The following steps have been followed:
a. The anti-log gain factor has been adjusted to the value 0.2975 by varying R13.
b. The log-anti-log circuits of Fig.5 are measured with the simulated input signal level fixed at -10 [dBm]. The results; shown in **Fig.7** demonstrate the agreement of measured and calculated responses.

Measurement of the Linear Amplifier-Detector Simulator :-

With the FB loop open; a variable DC voltage was introduced at the analog switch input and the output variation was measured. The measured characteristic coincided to the calculated one.

Measurement of the Closed Loop Characteristics :-

The results of these measurements have shown a complete agreement with the mathematical model. An example of the results is shown in **Fig.8.**

CONCLUSION

1. The detailed steady-state and transient performance of the homing missile receiver AGC subsystem has been qualitatively and quantitatively described by an exact mathematical/graphical model.

2.The complete AGC model has been successfully simulated by an analog circuit

3. Every important parameter of the AGC characteristics; including the IF gain, the input signal level and the detector output; has been explicitly represented by a

measurable DC voltage; which is a big advantage of this simulation method.

4. There is a reliable correspondence between the circuit model and the original AGC subsystem; which gives result to the agreement of the circuit response to different input excitations with that expected from the original subsystem of the hostile missile.
5. This leads to reliable measurements of transient response to be taken from the circuit model when subjected to certain jamming excitations; in order to optimize the parameters of that jamming technique for maximum possible degradation of the missile AGC.

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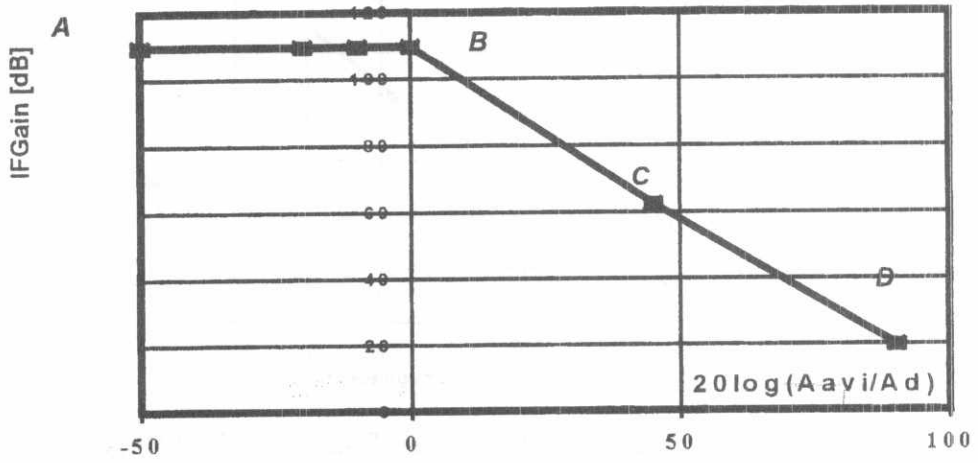

Fig.1-B. IF Gain as a function of Input Amplitude

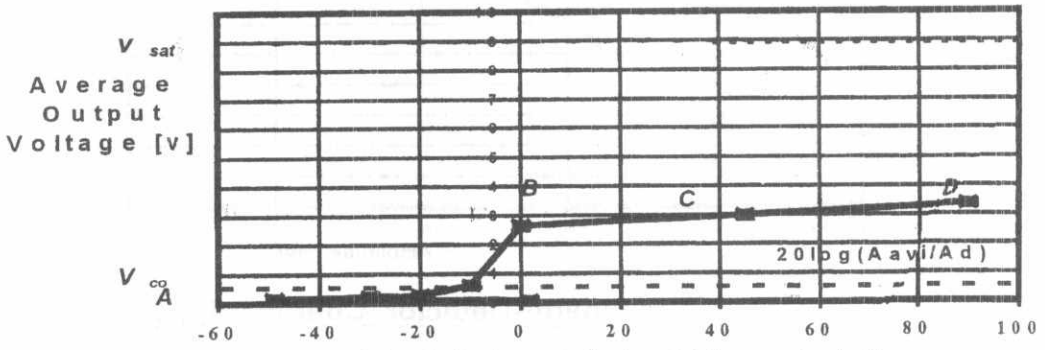

Fig.1-C. Input-Output Characteristic

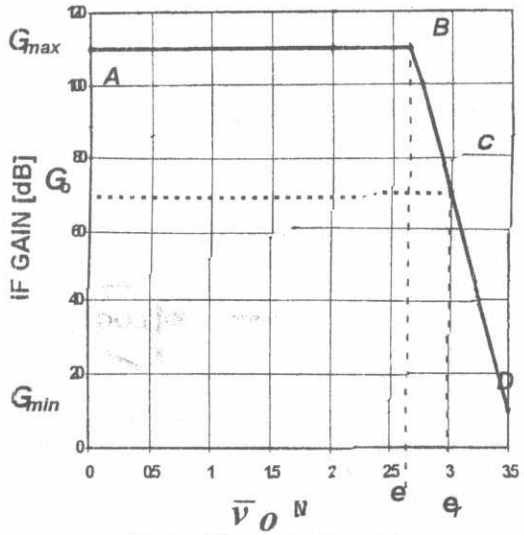

Fig.1-D. Gain Regulation Characteristic

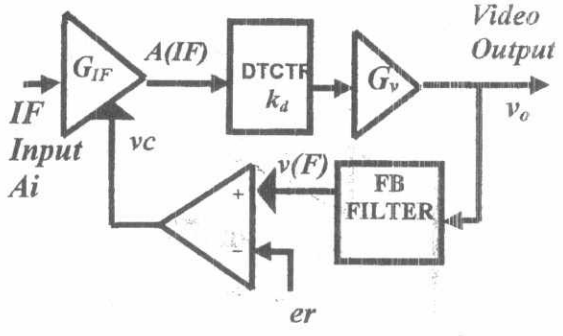

Fig.1-A. Simplified Block Diagram

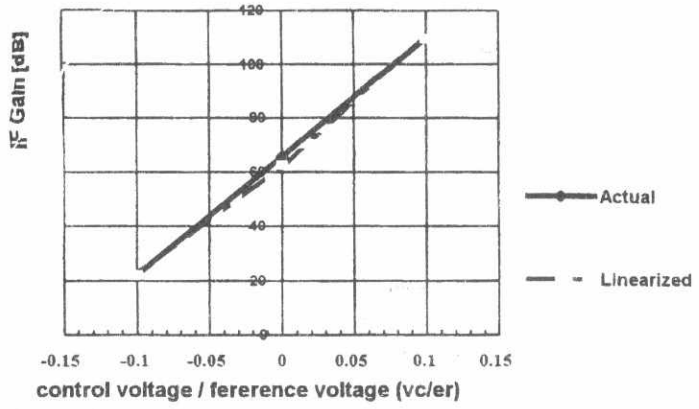

Fig.2. IF Amplifier Control Characteristic

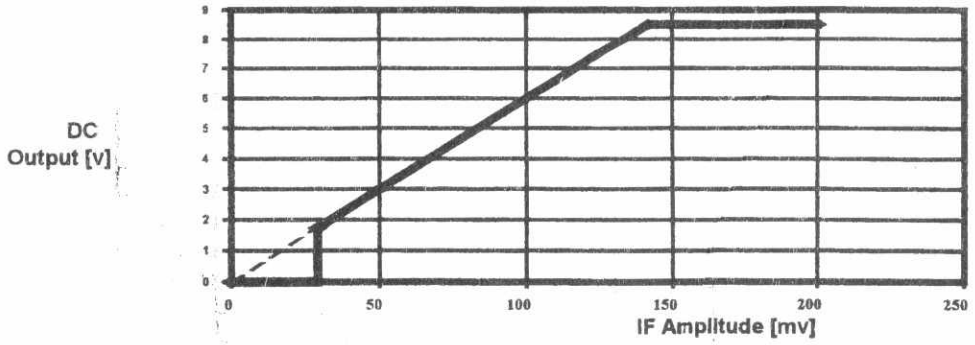

Fig.3. Amplifier-Limiter-Detector Characteristic

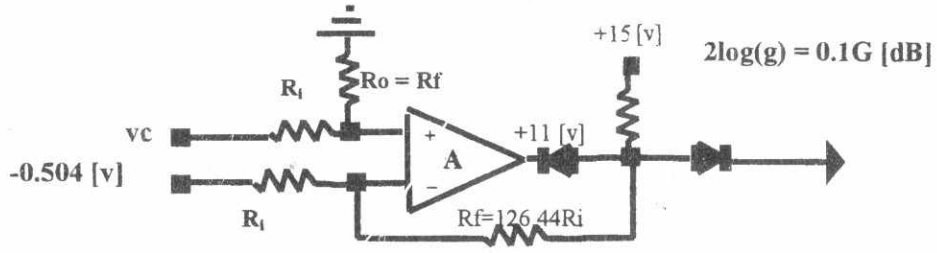

Fig.4 IF Gain Function Simulator

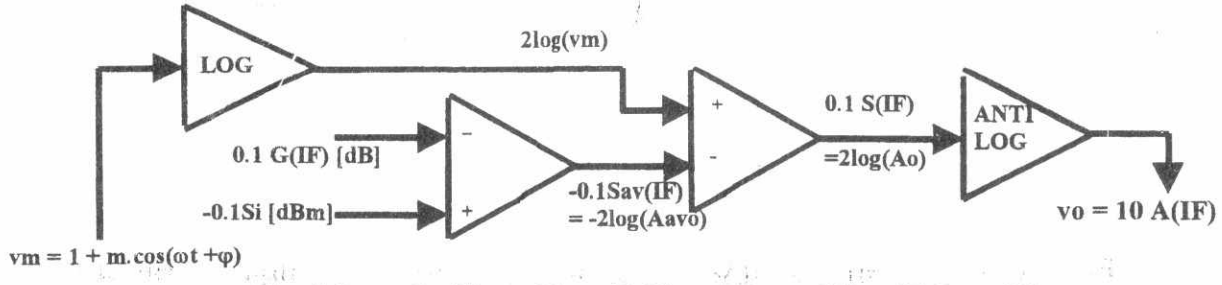

Fig.5 Log-AntiLog Circuit Simulator of the IF Amplifier

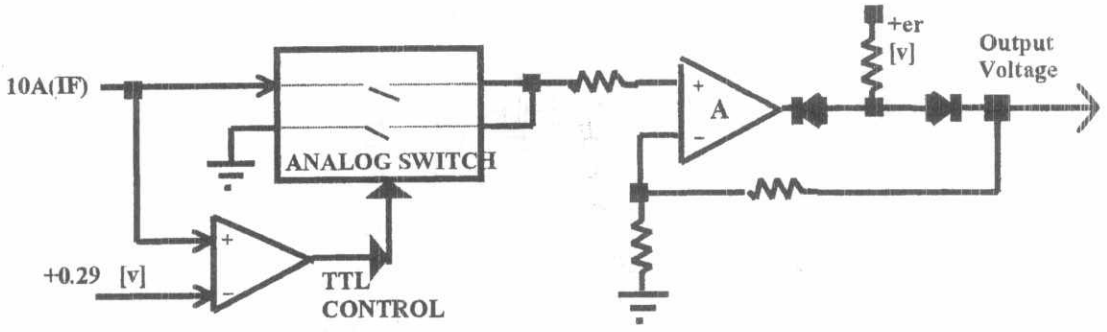

Fig.6. Simulation of the Linear Amplifier-Limiter-Detector Block

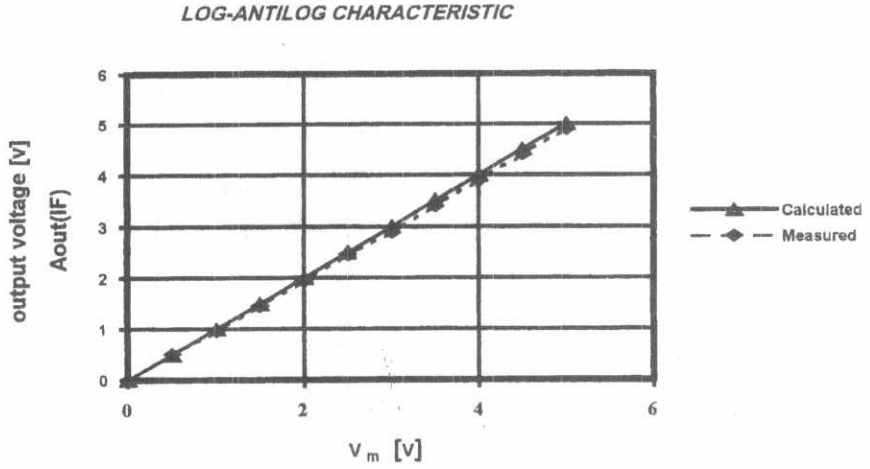

Fig.7. Measured Log-Antilog Characteristic

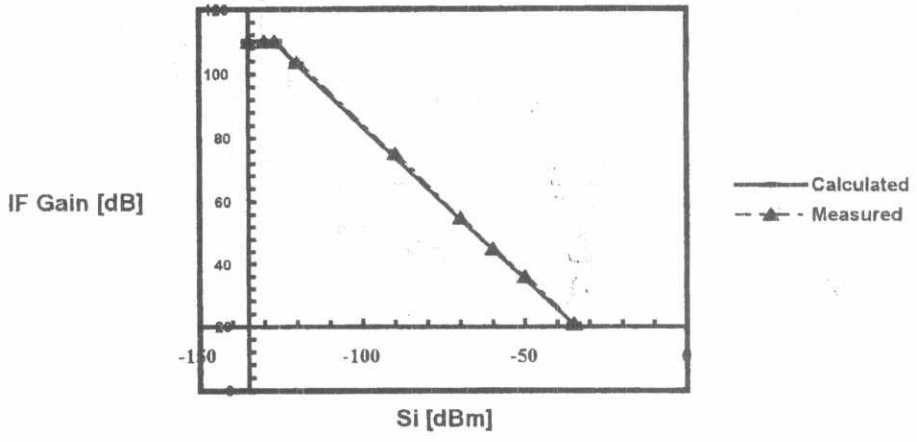

Fig.8. Measured IF Amplifier Control Characteristic

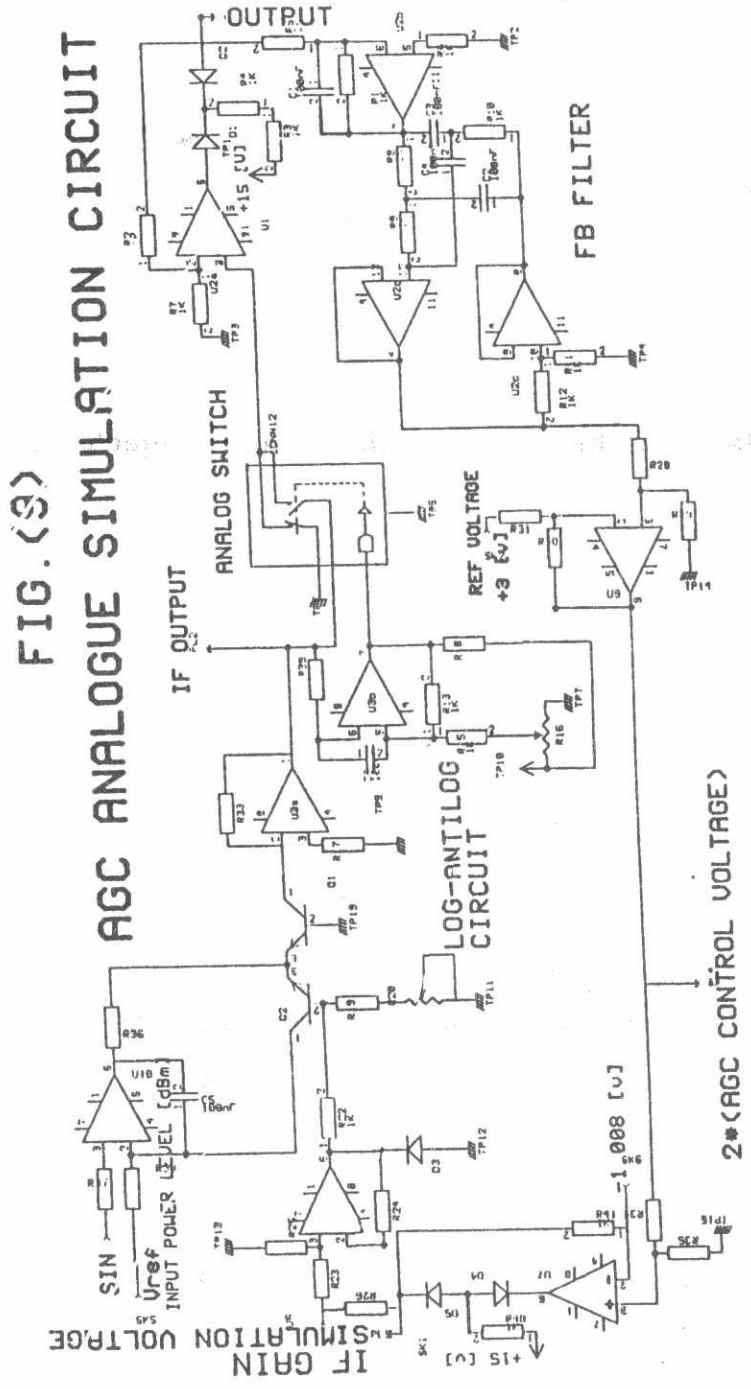

FIG.(3)
AGC ANALOGUE SIMULATION CIRCUIT