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CHOPPERED DC MOTOR DRIVE
USING MOS AND BIPOLAR POWER TRANSISTORS

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ABSTRACT

A four quadrant DC chopper circuit is presented applying a combination of MOS and bipolar power transistors as the main power elements. This circuit uses two MOS switches to take all required high frequency (up to 100 KHz) switching in the four quadrant operation. Two bipolar transistors are used in the return path of current as fast contactors to select the required quadrant of operation. Using of this scheme greatly reduces cost than the case of using four MOS switches. Moreover separate fast recovery diodes can be used as freewheeling diodes instead of relatively slower integral body-drain diode of the power MOSFET which cause restrictions on ON state switching speed.

In the following work, the detailes of design of power circuit to feed a 20 A- 18V separately excited DC motor is given. Analytical dependence of overall efficiency on operating frequency and battery voltage is discussed. Results show that frequency has a little effect so that a 100 kHz frequency seems to be practically possible with this configuration. Under such high frequency the armature leakage reactance alone is sufficient to draw smooth continuous current to give good motor operating characteristics.

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I- INTRODUCTION

Developments in the technology of power semiconductor devices speed up progress in the branch of electrical motor drives. Until few years ago thyristors had been used approximately in all motor drives over a wide range of power ratings but today their applications are restricted to high power low frequency drives where other devices cannot be used on account of their lower power ratings. Power transistors depending upon their better switching characteristics and absence of commutating circuitry gradually replaces thyristors in medium and low power application, such as battery operated vehicles and UPS where high operating frequency is used and overall efficiency is critical. At present power transistors (darlington) are produced with ratings more than 100 A and 500 V (collector to emitter sustained voltage) as a single package. Typical switching times from 1 to 3 micro seconds.

An exciting new power semiconductor device recently introduced is the power MOSFET. This offers the advantages of; very high gain, very fast switching speed (typical switching time below 0.2 us), and very rugged performance. Thermal and electrical instabilities experienced with bipolar transistor are absent in this device.

II- SWITCHING STRATEGIES FOR FOUR QUADRANT CHOPPERS

In general DC to DC converters must be designed for fast response and negligible dead band during transition from motoring to regenerative brake modes. The circuit diagram of an ideal four quadrant chopper system is shown in Fig.1. The DC input source must be able to supply and accept power /2/.

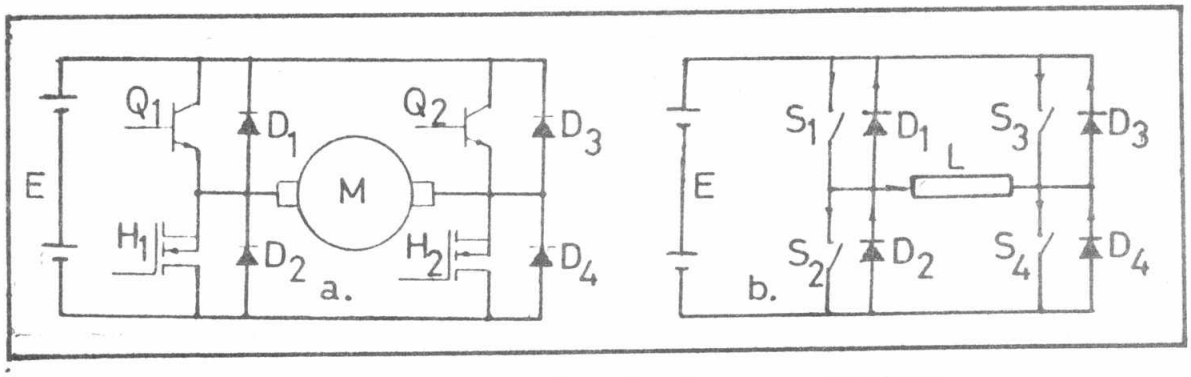

Fig.1 Four quadrant chopper system

Several switching strategies are in use; the simplest one is called the bipolar switching strategy. With this strategy, the changeover of the average value of the output voltage from positive to negative or vice versa is smooth. This is done simply by variation of the time ratio. However,the input current ripple and the output voltage ripple are large. Also number of switching per cycle is four and this increases switching losses.

A second switching strategy called unipolar reduces number of switching per cycle. The switching sequence depends on the required mode of motor operation. This strategy is the one used in cases of thyristorized and transistorized four quadrant choppers to give lesser number of ON/OFF switching per cycle and to reduce the output voltage ripple and input current ripple.

Another strategy called modified unipolar aims at symmetrical utilization of switches is described in /2/. However all these strategies necessitate that the four switches must be of the same switching speed since each one is subjected to high frequency ON/OFF switching in a certain mode of operation of the circuit.

The suggested scheme (Fig.1) introduces some modifications to unipolar strategy such that all high frequency switching duties in different modes of operation are carried upon by two MOS power switches. Thus two low cost bipolar power transistors (Q1 and Q2) can be used for the remaining two switches. This greatly reduces cost since price of bipolar power transistor is nearly one tenth of that MOS power transistor of the same ratings. Another advantage of this scheme is that only two diodes (D1,D3) of the four diodes are subjected to reverse recovery conditions during operation, these diodes are discrete component not integral part of the transistors so fast recovery diodes can be used. This enable MOS power transistor to apply its full switching speed with further reduction in switching losses. The relatively slower integral reverse diodes of MOS transistors are not subjected to reverse recovery conditions. In the suggested scheme S1 and S3 are bipolar power transistors while S2 and S4 are MOS power transistors. Diodes D1 and D3 are epitaxial fast recovery diodes while diodes D2 and D4 are body integral reverse diode of the MOS power transistor.

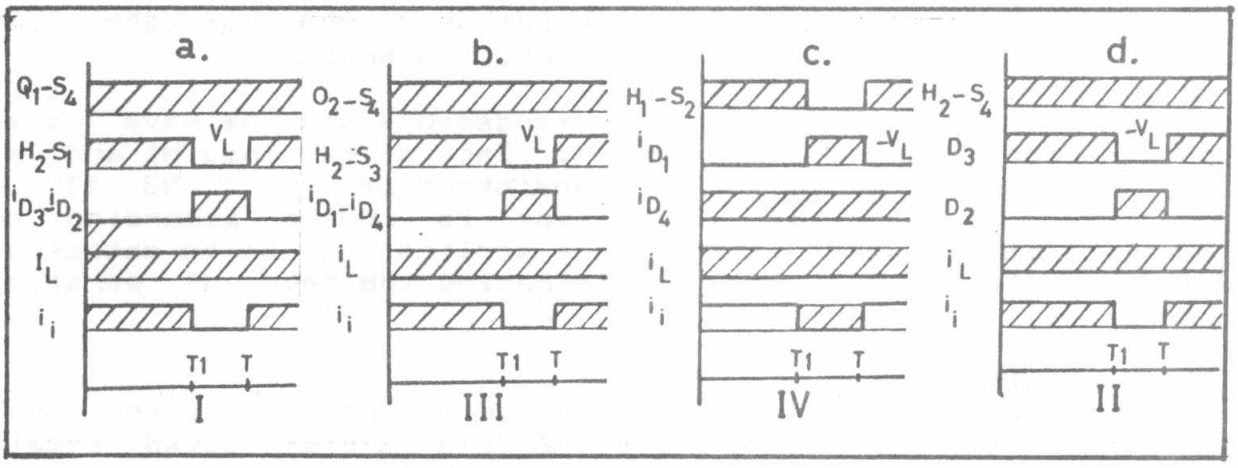

Fig.2 Switching Arrangments

Referring to Fig2., the sequence of operation is as follows;

1) Quadrant I/(a) (motoring) : S1 is driven permanently ON while S4 is driven by the high frequency ON/OFF signals of control circuit. During OFF period of S4 current

freewheels through D3 in the loop S1->motor->D3.

2) Quadrant IV/(c) (regenerative break): S2 is driven by the ON/OFF control signals while all other switches are in OFF state. During ON period of S2, the motor e.m.f drive current in the closed loop consisting of; motor->S2->D4 and this converts a part of the kinetic energy of the rotor into electromagnetic energy stored in the leakage reactance of armature. During OFF period of S2, the current is transferred through D1 to the battery delivering the energy previously stored in armature reactance to the battery. Repetition of ON/OFF transforms rotor kinetic energy back to the battery and brake the motor.
3) Quadrant III/(b): the same as in first quadrant with S3, S2, D1 replacing S1, S4, D3 respectively.
4) Quadrant II/(d): the same as in Q.IV with S4, D3 replacing S2, D1.

III- DESIGN OF POWER CIRCUIT

1- Selection of Switches

A - MOSFETs

MOS switches H1 and H2 are subjected to similar operating conditions. H1 closes for a period T1 during each cycle of time T seconds in first quadrant where;

$$D = T1/T \qquad (1)$$

D is the duty cycle of chopper which may vary between zero and unity according to the control signal. This necessitates that H1 and H2 must have continuous current rating equals the full load motor current with sufficient safety margin for over load operation. In our case these switches are designed to have maximum continuous current rating of 30 A. In OFF state the switch will be subjected to full supply voltage (24 V), so the OFF state drain to source voltage rating of the transistor must be higher than that expected in circuit operation.

Figure 2 shows the switching arrangements and the wave forms for the represented drive system. Each of switches H1 and H2 is made up of three HEXFET transistors of type (RS 130) connected in parallel. This type is chosen according to availability in local market. This application can be satisfied with single SIPMOS device eliminating the need of parallel operation.

Steady State Sharing of Current

During the period outside of the switching transition, the current in the parallel group of HEXFETs is distributed itself in the individual devices in inverse proportion to their ON state resistance. The device with the lowest resistance will carry the highest current. This leads to greater temperature rise in this device and consequently its resistance rises more than other devices. This fact means that good steady state sharing of current is expected although initial ON resistance

may be mismatched.

Dynamic Sharing of Current Under Switching Condition

It is necessary to take positive steps to ensure that the current is distributed properly between the group of devices connected in parallel under switching conditions. In summary the following points must be carefully considered /5/.

1- Threshold voltages should be matched withen determined limits.
2- Inductances that are common to gate and source circuits of the individual devices must be carefully matched.
3- Gates must be decoupled with individual resistors, and the output impedance of the drive circuit must be low in comparison.

B - Power Transistors

Each one of switches S1(Q1) and S3(Q2) is to be made of a single NPN power transistor to avoid problems associated with paralleling of such devices. S1 and S3 operate in continuous current mode, so each one should have a continuous current rating equal to the maximum expected load. The device BUX 98A satisfies the imposed current requirements.

C - Diodes

Concerning freewheeling diodes D1 and D3 (Fig.2 and Fig.3) the most critical ratings are those associated with reverse recovery conditions. In the suggested scheme the motor current is continuous, so when S2 is OFF, armature current freewheels through D1. When S2 closes again it must carry instantaneously a current $I = I_L + I_{RM}$. This current may exceed pulsed current rating of S2. Furthermore if switching speed of S2 is to high, cessations of the reverse recovery current of the diode induces destructive overvoltages with stray circuit inductance. This necessitates using of fast recovery diodes for D1 and D3. Each one of diodes D1 and D3 is made up of two parallel connected epitaxial fast recovery diodes of type BVY 32.

Assuming that S1 is applying its full switching speed, then the rate of decaying of the diode current is determined externally by the stray circuit inductance (about .5 uH) and the battery voltage (24 V), then;

$$dI/dt = E/L_s = 48 \quad A/\mu S \tag{2}$$

An expression for the last part given in /4/ as,

$$I_{RM} = (2\, Q_{RR}\, dI/dt)^{1/2} = 1.7 \quad A \tag{3}$$

This value of peak reverse current imposes no harmful duties on S2 since its pulsed current rating is higher than 76 A.

2- Total Power Dissipation and Efficiency

Power dissipation in S2 or S4 will be of three types namely; switching power losses(P_s), conduction power losses (P_{CH}) and

off state power losses which will be negligible in present application du to low operating voltage.

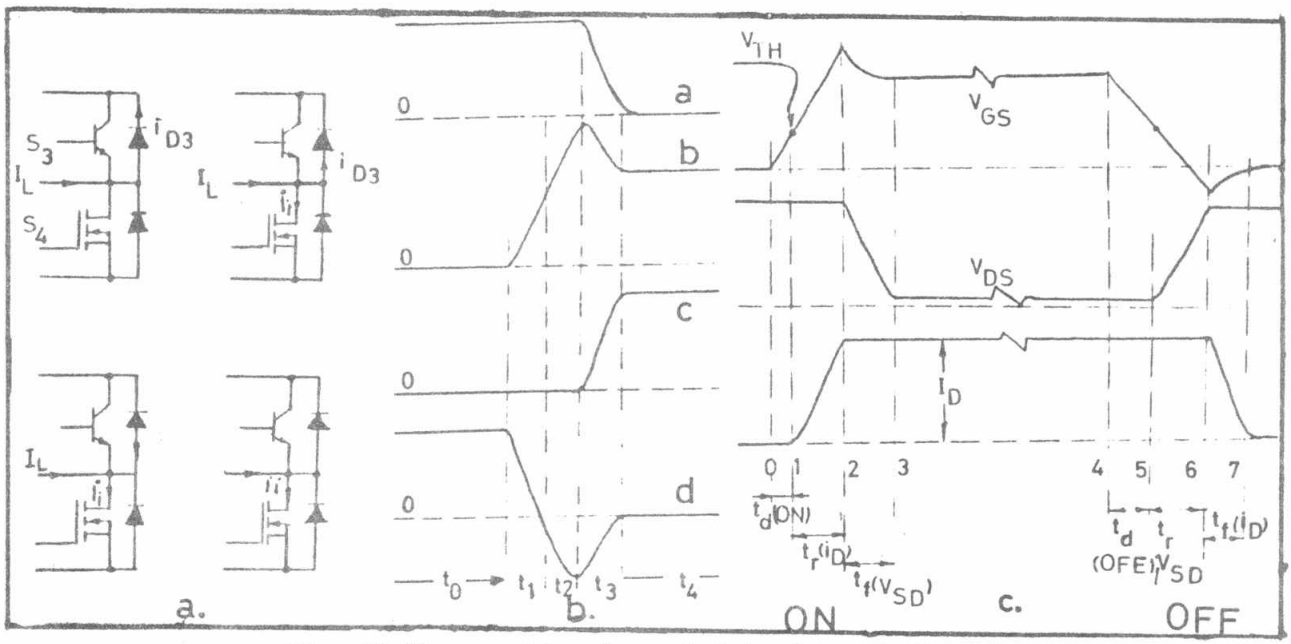

Fig.3 Theoretical and idealized Waveforms

Figure 3.c shows the idealized switching wave forms of the used type of MOSFETs with clamped inductive load of continuous current. Referring to the shown wave forms, switching losses can be expressed as ;

$$P_S = .5\ I_D\ V_D[t_r(i_D)+t_f(v_D+t_r(v_D)+t_f(i_D)]$$

$$P_S = 3.4 \times I_D \times V_D\ f \times 10^{-7} \qquad (4)$$

Assuming that MOSFET internal temperature is the maximum allowable value (150 C°) then the ON resistance will be .315 Ohm. The conduction power is;

$$P_{CH} = I_D^2 \times D \times R_{DS\ T} \qquad (5)$$

Then the total power per switch will be;

$$P_H = 3\ P_S + 3\ P_{CH}$$

Since the bipolar transistors Q1 and Q2 operate in continuous current mode, then there will not be any switching power losses and the total losses will be conduction losses due to collector and base currents, then ;

$$P_Q = V_{CEsat} \cdot I_C + V_{BE} \cdot I_{BF} \qquad (6)$$

Power losses in diode D1 or D2 will be of two types; forward conduction power losses P_{DC} and reverse recovery power losses. An expression for the last part P_{DS} is given in /4/ as,

$$P_{DS} = .5\ I_{RM}^2\ L_S\ f \qquad (7)$$

The stray loop inductance L_s has an order of magnitude of 0.5 uH. Then P_{DS} =.0723 W at 100 kHz and can be safely neglected. Then power losses in diodes is purely conductive;

$$P_{DC} = (1-D)\ I_L\ V_F = 0.85(1-D)\ I_L \qquad (8)$$

Power losses in motoring mode, which is the normal mode of operation- is higher than regenerative brake mode, so that losses and efficiency in this particular mode are the measure of circuit quality

$$P_{Loss} = P(HEXFETs) + P(power\ transistor) + P(diode) \qquad (9)$$

$$P_{Loss} = 3.4\times10^{-7} E I_L f + 2.35\ I_L + .105\ DI_L - .85\ DI_L + 12.5 \qquad (10)$$

Where duty cycle D depends on the input battery voltage ,load voltage and voltage drop in series elements,

$$D = V_L / [E-(1/3\ I_L\ R_{DST} + 1.5)] \qquad (11)$$

Finally efficiency of the circuit is given by ;

$$n = I_L\ V_L\ /(I_L\ V_L + P_{Loss}) \qquad (12)$$

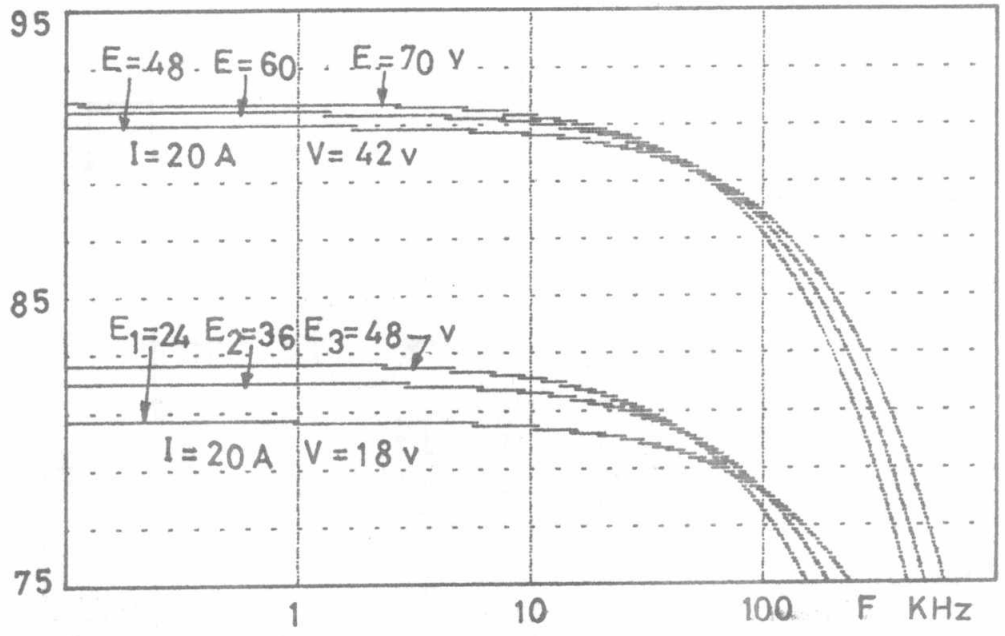

Fig.4 Efficiency and switching frequency

From the above equations it is clear that efficiency depends on I_L, V_L , E and switching frequency. Curves in Fig.4 give efficiency at different input and output voltages against operating frequency. At the particular load conditions considered here efficiency in general is below 85θ. This is an expected figure at this low voltage application, but the circuit can be operated at load voltages up to 48 V with efficiency higher than 95θ.

IV-DRIVE CIRCUITS AND DEVICES PROTECTION

1- HEXFETs Drive Circuit

HEXFETs are subjected to high frequency fast switching duties, so positive steps must be taken to clamp any expected overvoltage transients in both gate and drain circuits. This is of a vital importance since these devices are so sensitive to overvoltages that any transient voltage greater than 20V in gate circuit causes device failure whatever its duration is short. As shown in Fig.6 the following arrangements are present;

1- A 16V zener diode connected directly between gate and source leads is used for gate protection against transient overvoltage.
2- Clamping of expected overvoltages in drain circuit by using single 56V/1W zener diode.
3- A snubber circuit between drain and source is used to reduce OFF switching losses in HEXFET and to damp out any high frequency oscillations.
4- The gate drive circuit is designed to have low output impedance to reduce switching losses and assure good transient sharing of current between parallel connected HEXFETs.

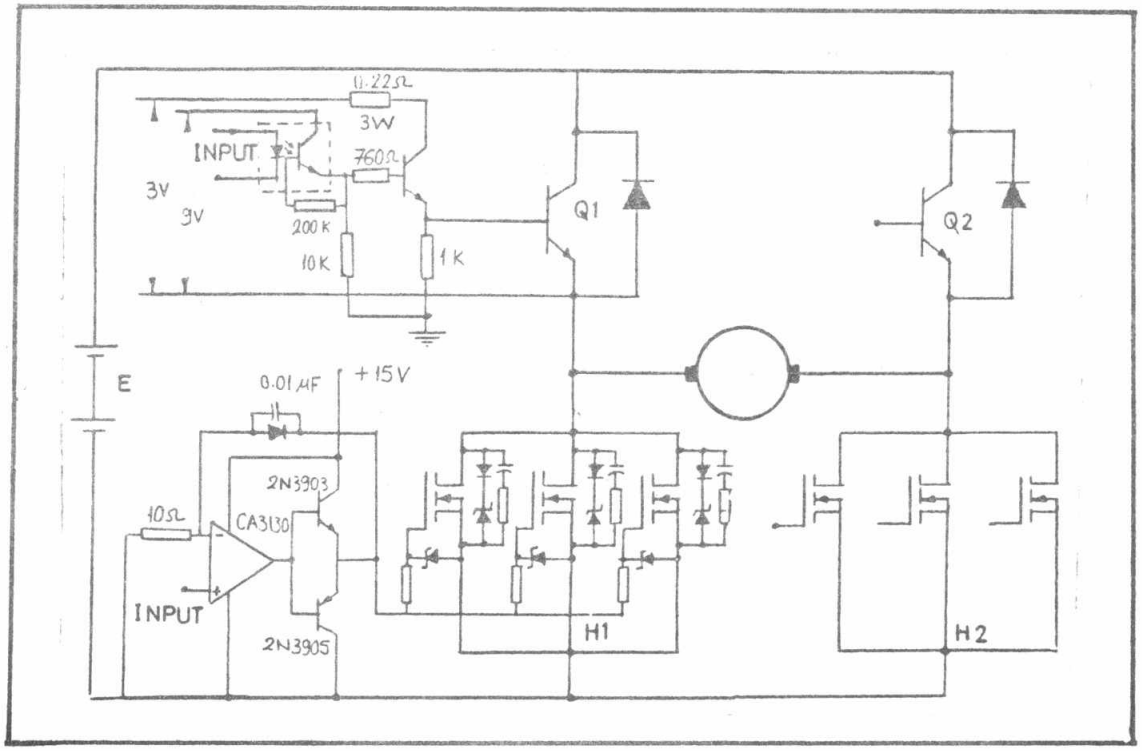

Fig.5 The Drive Circuit

2- Power Transistors

Power transistors are not subjected to high frequency switching. They are subjected to switching only when the mode

condition means that the transistor base drive circuit can be as simple as that used for DC operating condition.
As shown in Fig.5 a transistor optocoupler is used introduce the required isolation between control circuit and drive circuit. The transistor Q is a power darlington transistor used to drive Q1 directly from the optocoupler output. Voltages required for drive circuit are obtained from a switching power supply energized from the main DC supply.

V-BASIC MICROPROCESSOR CONTROL

This drive imposes difficult and variable duties on the control circuit including;

1- Power switches required variable gating schemes according to the mode of operation of drive.
2- Two control loops -speed loop and current loop- with their associated input measurements and compensating controllers must be considered.
3- An arrangement must be present to prevent simultaneous switching ON of switches on the same arm. Otherwise short circuit is expected.

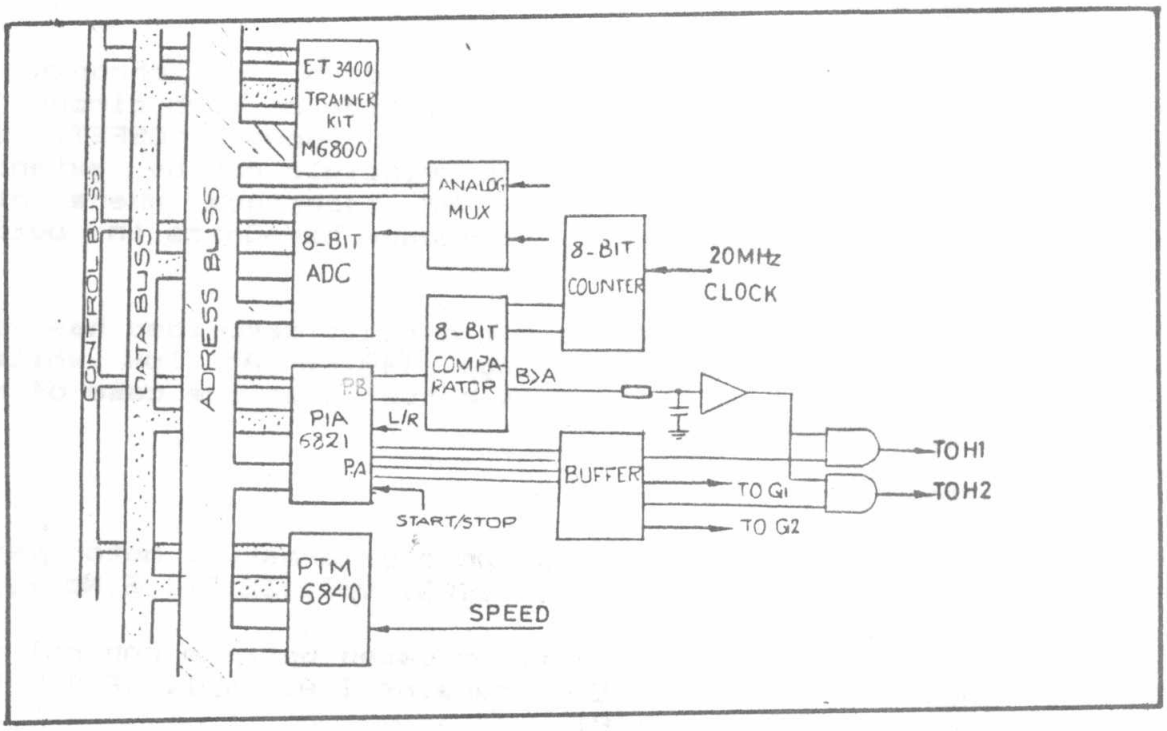

Fig.6 Microprocessor implimentation

The basic microprocessor system shown in Fig.6 , consists mainly of the following;
-The microprocessor trainer ET 3400 A consisting mainly of M 6802 MPU chip, ROM (2k) containing monitor program, 1/2 k byte RAM for temporary storage and the I/O accessories extending storage capability and giving facility of storing programs on a tape recorder for subsequent usage. As shown in Fig.6 the following hardware are added :

1- The peripheral interface adaptor (PIA) M6821P, of which port B is used as an output port to drive an 8-bit magnitude comparator. Port A gates the four power switches (S1,S2,S3 π S4), PA0 is used to monitor start/stop switch and PA7 is used to monitor Left/Right switch.
2- The ZN 448 ADC is used to feed the MPU with signals expressing armature current (I_L) and reference speed. The ADC is fed through two channels analog multiplexer.
3- The timer module PTM 6840 is used with optical speed encoder to measure motor speed.
4- PWM technique is implemented by comparing the digital value of the pulse width written by the MPU in port B of PIA with the output of a free running 8-bit counter taken its clock input from 26 MHz crystal oscillator. The PWM output signal is taken from B>A output terminal of the magnitude comparator, the frequency of this output is $f = fc/2^8 = 26MHz/256 = 100$ kHz. The MPU can alter the duty cycle of the chopper simply by altering the magnitude of the digital word written in port B of PIA.
5- The PWM output is ANDed with the gating signals from PA1 π PA2 to drive HEXFETs H1 π H2 respectively.

VI-CONCLUSION

A new power circuit for a four quadrant dc chopper is presented. The microprocessor implementation of such circuit is described. The cost is reduced by using power MOSFETs and conventional power transistors. The principle can be extended to three phase inverter using PWM technique where high switching frequency is necessary to reduce harmonics in output voltages.

From point of view of efficiency the circuit described has very high value at medium load voltage (48V). At low voltage efficiency is not so high but it is better than the case of any other four quadrant circuit.

VII-REFRENCES

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