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Fabrication, electrical investigation, and photovoltaic investigations of Au/In_2Se_3/p-Si/Al diode using thermal evaporation approach

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ABSTRACT

The heterojunction of Au/In_2Se_3/p-type silicon (p-Si)/Al was manufactured in this study by the deposition of the In_2Se_3 layer on p-Si wafers using the thermal evaporation process. The heterojunction's dark current-voltage characteristics were measured throughout a temperature range of 308 to 398 K. The characteristics and conduction mechanisms of heterojunction diodes have been investigated. The major electrical properties of the examined device were extracted via current-voltage measurements. At the targeted temperature range, the space charge-limited conduction mechanism was investigated, and thorough information about the conduction mechanism was obtained. Current-voltage characteristics and power-law dependence were discovered to be dictated by space charge-limited currents and temperature dependence. The extracted series and shunt resistances decreased as the temperature rose, indicating that the device's properties improved as the temperature rose. The manufactured films' and junction diode's measured properties indicate that they can be used as photodetectors and photovoltaic applications

1. Introduction

Because of their broad variety of technical applications and exceptional flexibility, semiconductor heterojunctions have become one of the most active research and development areas in recent years [1-4]. The heterojunction interface has many more customizable characteristics, allowing designers to tailor the properties of the heterojunction device to their specific requirements. Because Si is the most common semiconductor material, the idea of constructing photoelectronic devices with it has long been enticing because of the predicted cost, reliability, and functionality advantages[5]. The lack of effective Si light-emitting devices has hampered the development of Si optoelectronics so far [6]. Researchers are increasingly interested in semiconductor photocatalysis and photo electrocatalysis.

Because of its acceptable bandgap, low toxicity, and morphological diversity, In2Se3 is regarded as a promising material [7]. Due to the quick recombination of photoexcited electron-hole pairs and limited surface reaction kinetics, it is extremely difficult for a single semiconductor to achieve good activity [8].

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To increase the separation of carriers in existing photocatalysts, many tactics have been used, including morphological manipulation, element doping, and heterostructure creation [9]. Heterojunctions have been shown to widen the light absorption range and make carrier separation of target material easier, but the traditional heterojunction was generally associated with a complicated preparation method and poor interfacial contact [10]. Solar energy harvesting [11], photo-detection, and phase-change memory [12] have all been identified as uses for indium selenide, a direct bandgap III-VI semiconductor with a layered structure [13].

Indium selenide thin films were produced on FTO-coated glass substrates using a chemical spray pyrolysis process and examined for photoelectrochemical cell (PEC) applications by Yadav [14]. Studying the effect of substrate temperature and film thickness on photocurrent fluctuation via thin-film changes was also investigated. According to their findings, the In_2Se_3 film has n-type electrical conductivity. The photoelectrochemical cells (PEC) conversion efficiency and fill factor (FF) were found to be 0.71 % and 51 %, respectively.

The In_2Se_3 films that were recently formed on p-type silicon single crystals presented a wide range of prospective uses. The obtained n-In_2Se_3 device-based structure is appropriate for junction applications to an In_2Se_3-p-Si strong bonded junction. However, a technical issue in the development of the p-n junction diode is still the enhancement of charge production and decrease of charge recombination at the junction. The charge transport capabilities of the thin contact In_2Se_3/p-Si may be impacted by the temperature-dependent electrical characteristics of the material. Therefore, it is necessary to have a full understanding of the charge transport mechanisms between the layers of In_2Se_3 and doped p-Si to increase the stability and electrical conductivity of p-n junction diodes. We studied the feasibility of generating In_2Se_3 films using a thermal evaporation process, with an emphasis on structural properties and device-based In_2Se_3 films in this study. By regulating the parameters that determine device utilization efficiency, this strategy could lead to the optimum characterization and applications of In_2Se_3 films as well as cost-effective devices.

Using thermal evaporation, we created an Au/In_2Se_3/p-Si/Al heterojunction. This research aims to better understand the temperature dependency of the dark current-voltage characteristics for Au/In_2Se_3/p-Si/Al heterojunctions manufactured by thermal evaporation. The data from these measurements are evaluated and used to determine the heterojunction's distinctive properties and estimate the prevailing conduction mechanism.

2. Experimental details

2.1. Materials and chemical processing

The high-purity powder of In_2Se_3 (purity: 99.999%), was provided by Leybold Heraeus GmbH which was used without further purification. A polished p-type Si wafer with (100) orientation, a sheet resistance of 5-20, and a hole concentration of 1.6x 10^{17} cm^{-3} with a thickness of 400 nm was employed as a substrate. For 30 seconds, p-Si was chemically etched using HF: HNO_3:CH_3COOH (1:6:1) composition. The silicon wafers were etched, then washed with distilled water and isopropyl alcohol before being dried. On one side of the p-Si specimen, an aluminum (Al) electrode was deposited, while the other side was coated with In_2Se_3 films using a vacuum thermal evaporator (Edwards, E-306 A) at 300 K at a vacuum of 2×10^{-4} Pa. The In_2Se_3 layer was then covered with an Au mesh to serve as an ohmic electrode. The schematic diagram of Au/In_2Se_3/p-Si/Al heterojunction is illustrated in Fig.1. The deposition rate remained constant at 10 nm/min throughout the deposition process, whereas the thickness of In_2Se_3 varied from 232 to 1200 nm, measured by a crystal thickness monitor.

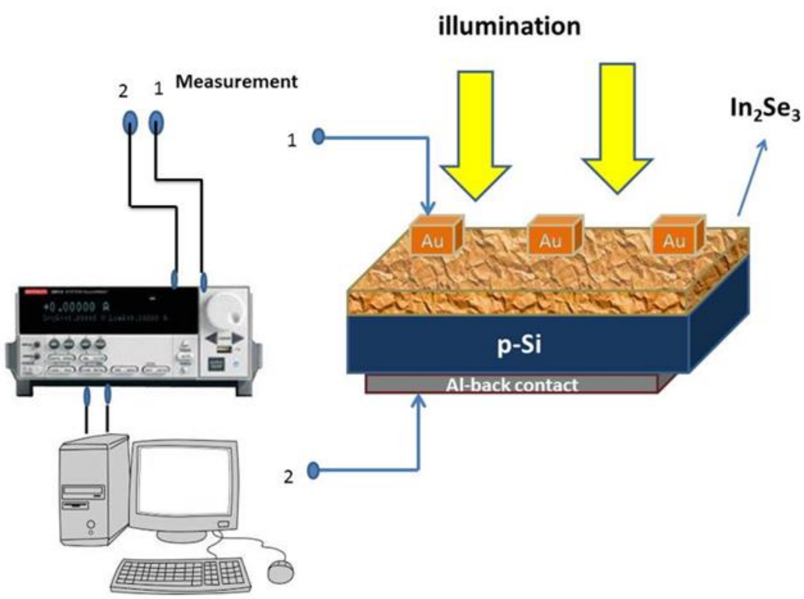

Fig.1. Schematic diagram of Au/In2Se3/P-Si/Al heterojunction.

2.2. Characterization tools

The surface morphology of In_2Se_3 thin films was studied using a JEOL JCM-6010LV scanning electron microscope operating at 20 kV. Transmission electron microscopy, type JEOL JEM-2100F, was used to study the crystallinity of the prepared films.

Using a Keithley 2635 A and a comprehensive computerization system, the current-voltage characteristics of the constructed heterojunction were determined by measuring the resulting current corresponding to a specific potential difference dropped across the junction. The temperature was directly monitored using a Pt–PtRh thermocouple and a monitor (Philips's thermostat PT 2282 A). To avoid an abrupt reduction in heater temperature, a proportional temperature controller (Eurotherm model no. 390-200) was utilized.

3. Results and discussion

3.1. Structural and morphology characterizations

The TEM image of the In_2Se_3 thin film is shown in Fig. 2(a). The TEM image may show the development of nanocrystalline rods in thin films. The optical characteristics and application system applicability are significantly influenced by its crystal structures, size, and shape [15]. An agglomeration of crystallites is seen in the figure. The selected area electron diffraction (SAED) pattern of In2Se3 thin films is shown in Fig.2(b). The polycrystalline nature of In2Se3 films is indicated by this electron diffraction pattern. The line profile distribution was used to confirm the nanoparticle structure, which results in a particle size of roughly 16 nm (Fig.2 (c)). The use of SEM to acquire information on surface morphological characterization is promising. The front image of the SEM micrograph is shown in different magnifications of 2000x and 7000x in Fig.3 (a) and (b). It's also possible to see a buildup of partially overlapping or merged grains. Furthermore, the figures acquired at a greater magnification reveal that the In_2Se_3 nanoparticles on the substrate surface are well-structured and firmly packed. Furthermore, Fig. 3(c) demonstrates that the roughness is around 10–20 nm with a nearly homogeneous surface, depending on the line profile distribution.

3.2. Current-voltage of Au/In2Se3/p-Si/Al heterojunction characteristics

The current-voltage characteristics study is incredibly important for identifying the characteristic parameters as well as the transport processes that influence the device's conduction process. The primary operational parameters of the investigated diode are the potential barrier height, Φ_b, diode quality factor (n), the reverse saturation current (I_o), the series (R_s), and shunt (R_{sh}) resistances.

Fig. 4 shows the dark current-voltage characteristics of the diode tested over a large temperature range of 308 K to 398 K. The diode exhibited great rectification performance over the measured temperature range and show temperature-dependent, as shown in the figure. The junction behavior of the investigated structure is confirmed by these graphs. The impact of series resistance (R_s) and interface states causes the divergence from linearity at greater applied bias [16].

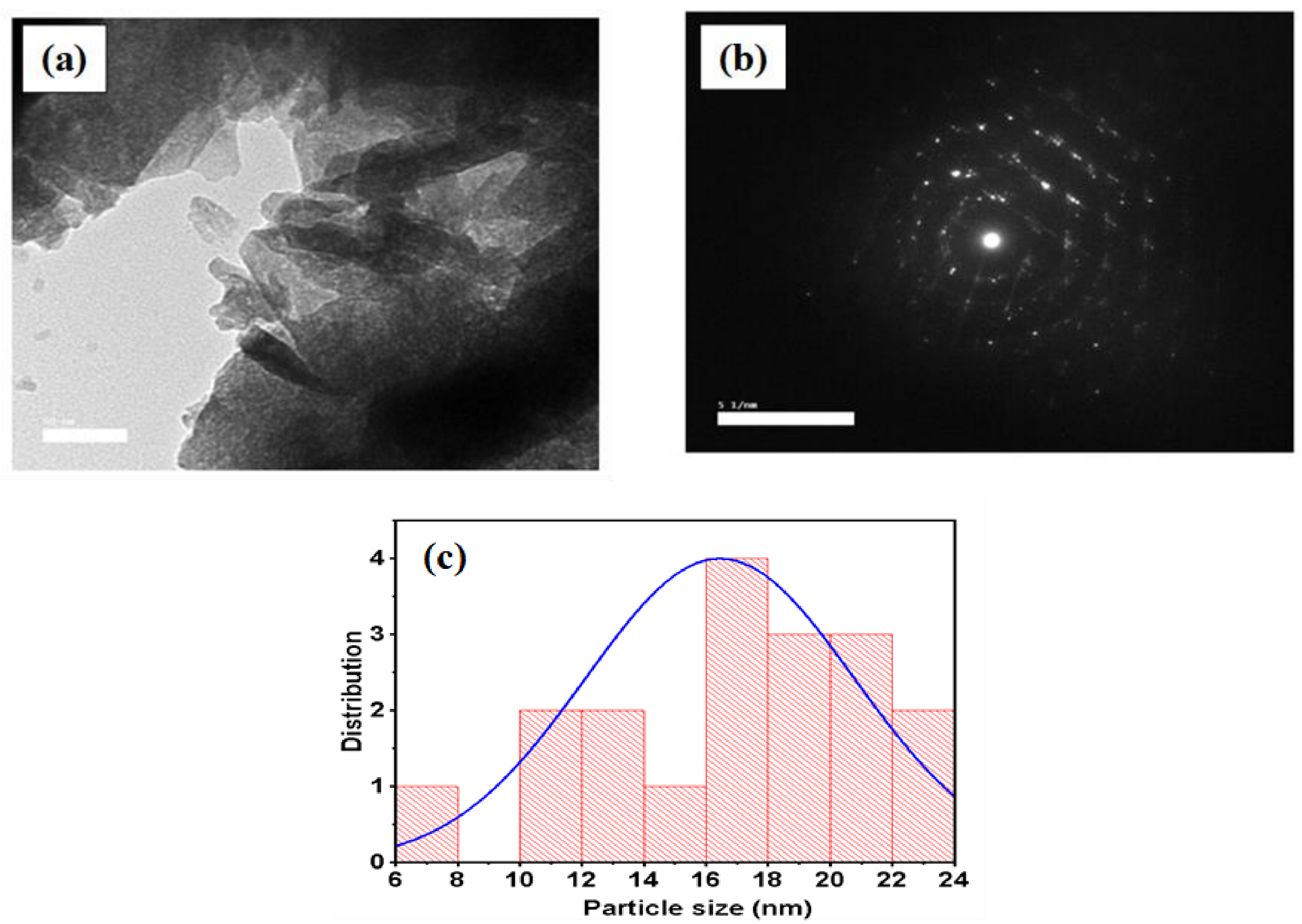

Fig. 2. (a) TEM image for In_2Se_3 thin film, **(b)** Electron diffraction pattern for In_2Se_3 thin film, **(c)** Distributional histogram of In_2Se_3 particle size deduced from TEM image.

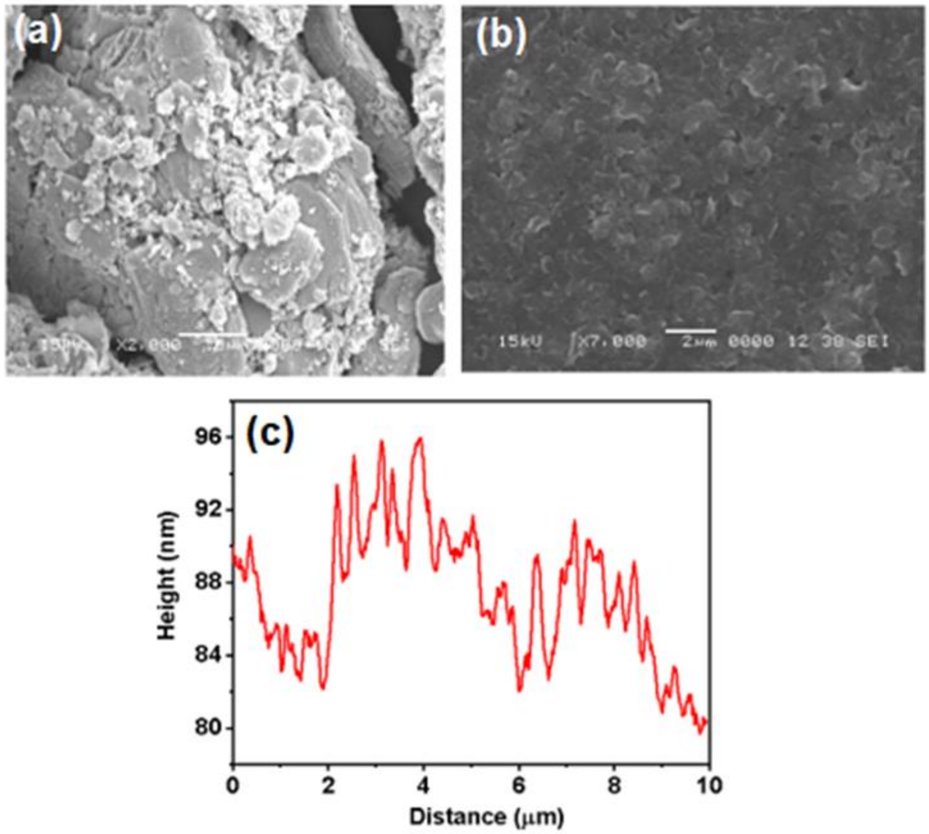

Fig.3. SEM image, (a) x=2000,(b) X=7000, (c) Height vs. distance of In_2Se_3 sample.

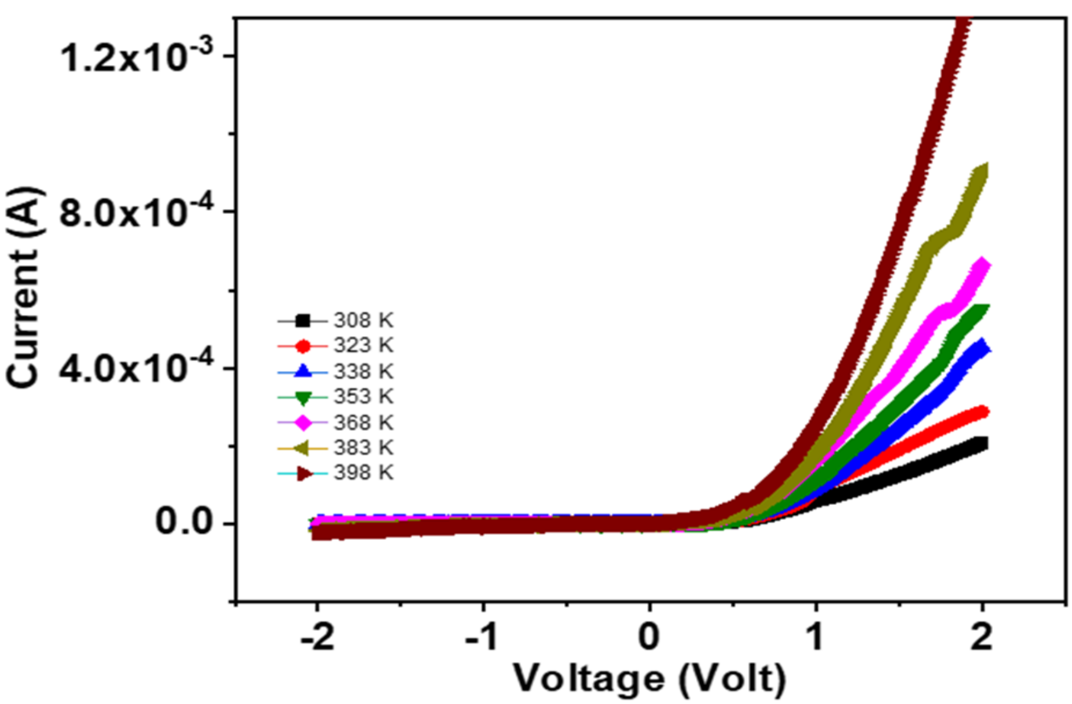

Fig.4. Current-voltage characteristics of $Au/In_2Se_3/p\text{-}Si/Al$ heterojunction at different temperatures in both forward and reverse bias.

This figure verifies the development of heterojunction, in which the barrier at the interface limits the forward and reverse carrier's flow across the junction, where the built-in potential can be created and can explain this phenomenon. The dark current-voltage characteristics of In2Se3-based junction with a Si substrate at various temperatures in steady-state can be described as follows [17]:

$$J = J_o\left(e^{\frac{q(v-JR_s)}{nKT}} - 1\right) + \frac{(V - JR_s)}{R_{sh}} \quad \textbf{(1)}$$

where n is the ideality factor, J_0 is the reverse saturation current density, R_s is the series resistance and R_{sh} is the shunt resistance.

Some characteristics, such as series, R_s, and shunt, R_{sh} resistances, play a significant role in controlling the heterojunction mechanism. Singh et al. [18] have explained how to derive the series resistance (R_s) and shunt resistance (R_{sh}) from the current-voltage characteristics. Accordingly, the current-voltage characteristics at low and high bias can be used to estimate these resistances. The voltage and temperature dependence of both series and shunt resistances are shown in Figs. 5 and 6. As can be seen, biassing influences the values of R_s and R_{sh}, and each minimum value is reached at a larger forward and reverse bias. Furthermore, as the temperature rises, the series and shunt resistances are found to decrease with increasing temperature. Additionally, the series and shunt resistance values are found to be higher than those reported in the literature, which is presented in Table 1 [14,31-33,36,37]. The results agree with those that Wageh et al. [19] and Gupta et al. [20] have already published. This effect can be explained by the fact that a diode's leakage current reduces, and its conductivity rises as temperature increases [21].

The ideality factor can be computed from the linearly fitted region of the slope of ln *J*- *V* characteristics utilizing the following Eq.

$$n = \frac{q}{kT}\frac{dV}{d\ln J} \quad \textbf{(2)}$$

Furthermore, the barrier height can be calculated by extrapolating the intercept with the y-axis of the forward current axis at zero bias using the following Eq.

$$\Phi_b = \frac{kT}{q}\ln\left(\frac{A^*T^2}{J_0}\right) \quad \textbf{(3)}$$

Table (1): The main calculated parameters of the In_2Se_3-based heterojunction in dark.

T(K)	R_s	R_{sh}	n	Φ_b (eV)	Ref.
In_2Se_3 (at 308 K)	9.6 x10³Ω cm²	6.2 x10⁸Ω cm²	7.6	0.8	**Our study**
In_2Se_3/1M(NaOH+Na_2S+S)/C At 350°c	69Ω	1.776x10³Ω	-	-	**[14]**
n-In_2Se_3|NaOH(1M) +S(1M)+Na_2S(1M) |c(graphite)	1.941x10³Ω	1.452 x10³Ω	3.85	0.53	**[31]**
ItO/In_2Se_3/$CuInSe_3$/Au	0.36 Ωcm²	9.0 x10³Ωcm²	1.23		**[32]**
Pure In_2S_3	1.95 Ωcm²	142x10³Ωcm²			**[33]**
In_2Se_3 doped Sn^{4+}1%	2.17Ωcm²	856.63Ωcm²			**[33]**
In_2Se_3 doped Sn^{4+}2%	1.48Ωcm²	533.41Ωcm²			**[33]**
In_2Se_3 doped Sn^{4+}3%	1.37Ωcm²	609.63Ωcm²			**[33]**
In_2Se_3 doped Sn^{4+}5%	2.45Ωcm²	126.18Ωcm²			**[33]**
β – In_2S	861Ω	993Ω			**[36]**
Cu_2ZnSnS_4/In_2S_3 (Copper concentration 2.5)	16.3Ωcm²	240Ωcm²			**[37]**
Cu_2ZnSnS_4/In_2S_3 (Copper concentration 3)	9.1Ωcm²	167Ωcm²			**[37]**
Cu_2ZnSnS_4/In_2S_3 (Copper concentration 3.5)	7.2Ωcm²	127Ωcm²			**[37]**
Cu_2ZnSnS_4/In_2S_3 (Copper concentration 4)	6.9Ωcm²	180Ωcm²			**[37]**

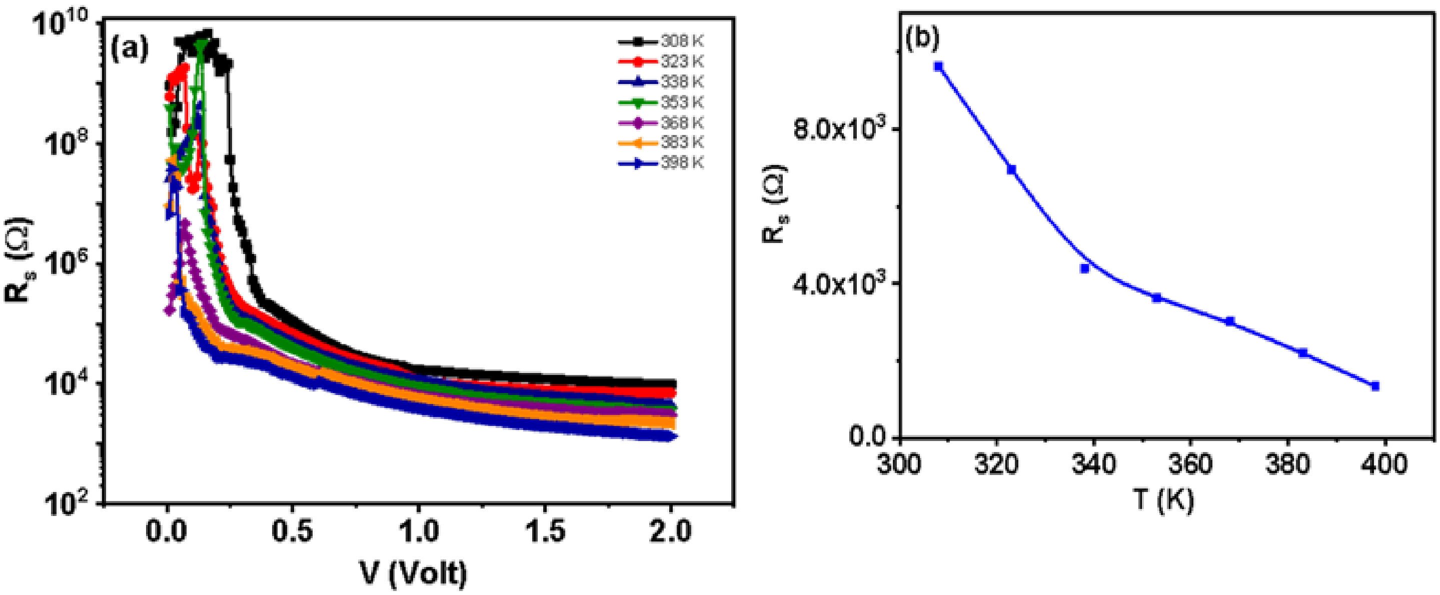

Fig. 5.(a) Series resistance behavior with applied voltage at a different temperature, **(b)** Plot of the temperature dependence of series resistance for Au/In_2Se_3/p-Si/Al device.

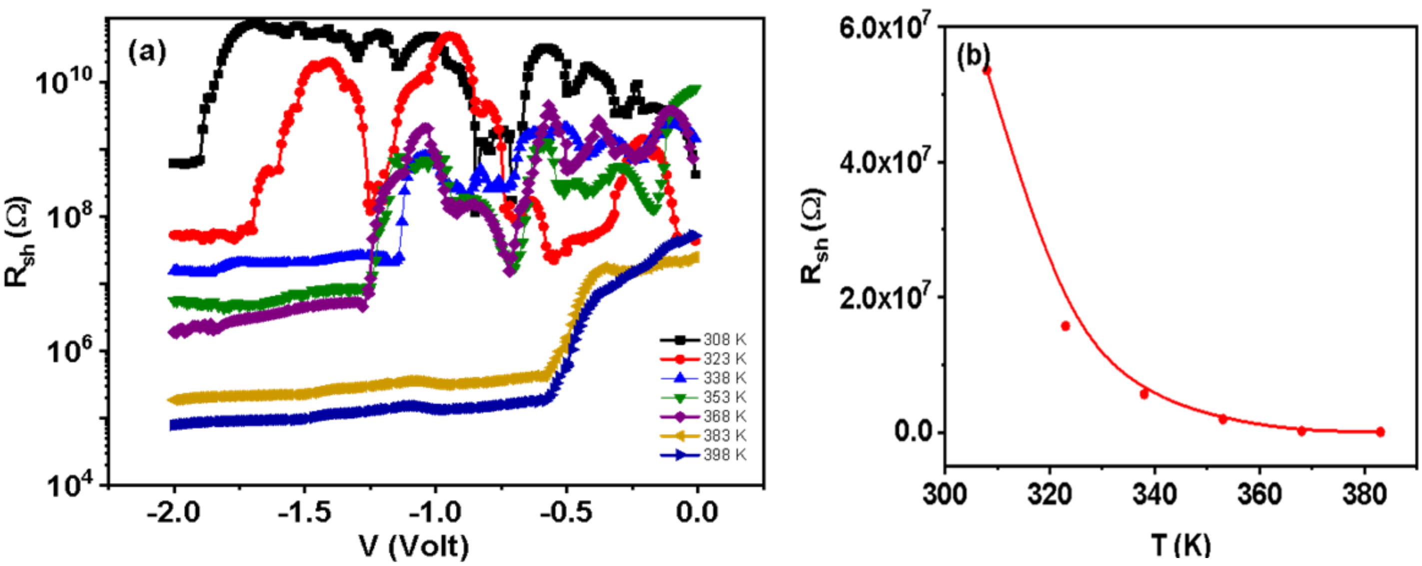

Fig. 6.(a) Shunt resistance behavior with applied voltage at a different temperature, **(b)** Plot of the temperature dependence of shunt resistance for Au/In_2Se_3/p-Si/Al device.

The ideality factor is determined to be unity for the ideal diode, but due to several circumstances such as the presence of an interfacial oxide layer and/or inhomogeneity of barrier height, it is significantly larger than this number [22]. The values of Φ_b and n of the investigated junction are shown in Fig. 7 and Table 1 as functions of temperature. Both parameters are significantly influenced by the temperature. The value of n decreases from 7.6 to 4.7 as the temperature climbs from 308 to 398 K, but the value of b rises from 0.8 to 0.95 for the same temperature range. The barrier height inhomogeneity brought on by the non-uniformity of the junction interface can be used to explain this behavior [23]. A graph of ideality factor vs barrier height is plotted for each temperature to achieve the ideal or homogenous barrier height; Fig. 8, the resultant straight-line fit reveals the presence of lateral barrier inhomogeneity. The homogenous value of barrier height is calculated to be 1.14 eV by extrapolating the straight line to an ideal value of n = 1. The lattice mismatch at the junction interface can cause the barrier height to deviate. More research was done to see if the thermionic conduction mechanism was the most prevalent functioning conduction mechanism. [24] gives the saturation current density according to this equation:

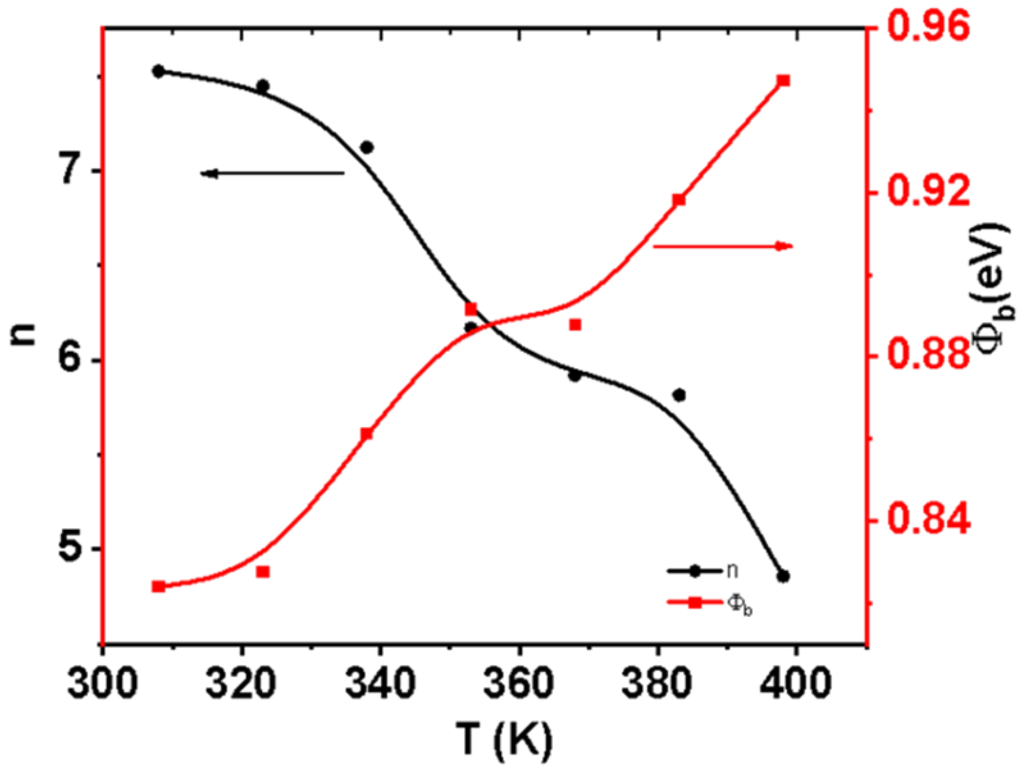

Fig. 7. Barrier height and ideality factor vs. temperature of Au/In_2Se_3/p-Si/Al heterojunction device.

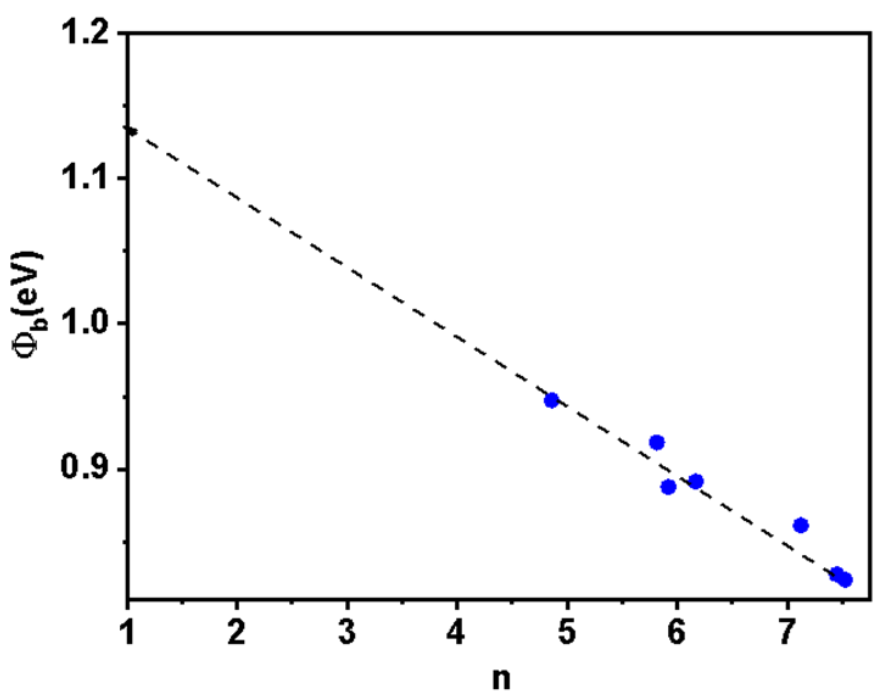

Fig. 8. Plot of barrier height, Φ_b vs. ideality factor, n of Au/In_2Se_3/p-Si/Al junction.

$$J_o = J_\infty \exp\left(\frac{-\Delta E}{kT}\right) \quad \textbf{(4)}$$

Where J_∞ is a constant. The activation energy was measured to be 1.18 eV based on the slope of the log J_0 vs. 1/T of the figure, shown in Fig. 9.

We re-plotted current-voltage characteristics in the log-log scale to better comprehend the conduction process, as shown in Fig. 10. Two separate linear zones are observed depending on the voltage region, showing various conduction processes, and confirming the presence of two major conduction mechanisms. By enforcing the law of current density changes in the form of $I \propto V^m$, if there is a deep trap at the interface, the charge transport profile is affected, and these variations influence the slopes of the current-voltage characteristics. Using a least-square fit, the m values were determined from the slopes of the two regions shown in Fig.10. The slope (m) in region I ($0 \le V \le 0.4$) is 3.8–1.64, whereas the m values in region II ($0.5 \le V \le 2$) are 9.9-2.7. This suggests that the first region's conduction mechanism is controlled by trap-charge limited current (TCLC) and determined by the energy distribution of trap levels within the forbidden band [25], whereas the second region's conduction mechanism is controlled by exponential trap distribution and converts to quadratic trap distribution as the temperature rises.

As seen in Fig. 11(a) and (b), the m1 and m2 values decrease as the temperature rises, confirming the same behavior of SCLC under influence of temperature. The trap-filling region with a charge injection in the bulk corresponds to the high value of m. With increasing voltage, the number of charge carriers participating in the conduction process grows. The rise in charge carrier density in the bulk causes a rapid increase in current with small increases in voltage. The bulk can use all injected charges in current conduction until it gets saturated, at which point injected charge begins to collect near the injecting electrodes [26]. The rate of growth of current with voltage reduces as the applied voltage is increased further, and the slope in the double log plot equals 2.

3.3. Photovoltaic characteristics of In_2Se_3-based junction

Fig. 12(a,b) shows the current density-voltage measurements of the examined junctions in dark under the illumination of 80 mW/cm2. The separation of electron-hole pairs at the junction contact can lead to the generation of the acquired photocurrent. The current was produced by the separation of electron and hole pairs, or electron-hole pairs. The electric field at the junction interface is causing these charge carriers to move apart from one another and subsequently produce a current [27, 28].

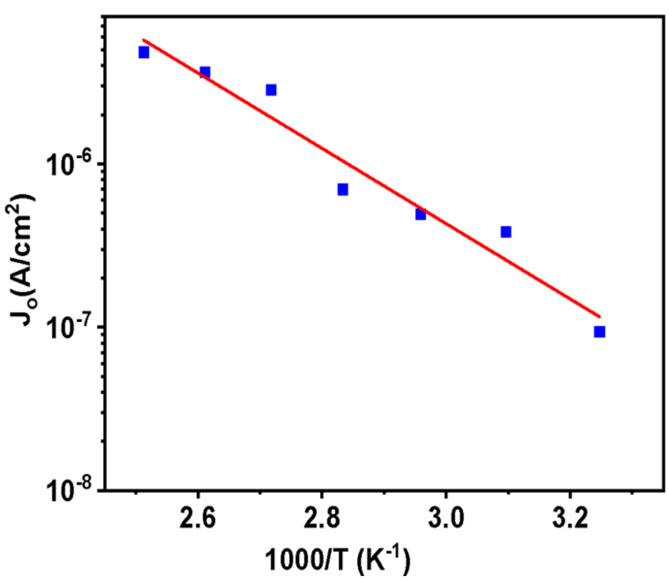

Fig. 9. A semilogarithmic plot of reverse saturation current density vs. 1/T for Au/In_2Se_3/p-Si/Al heterojunction.

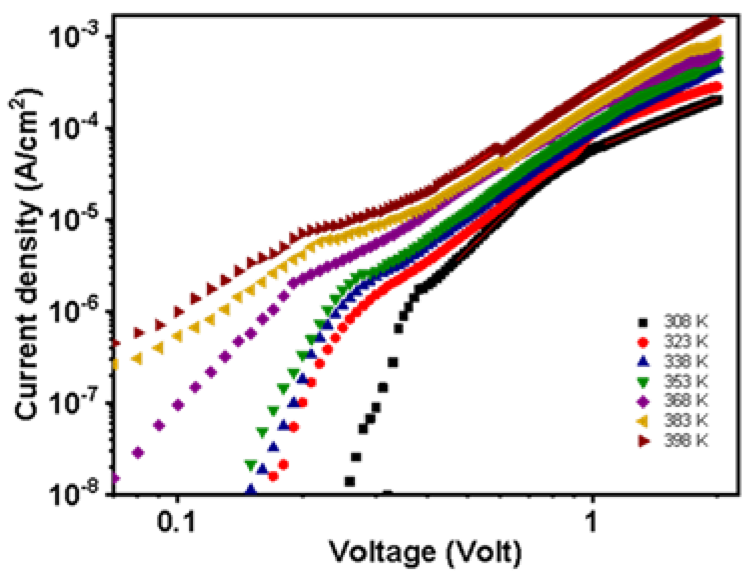

Fig. 10. Double logarithmic current density -voltage characteristics of Au/In_2Se_3/p-Si/Al heterojunction at different temperatures

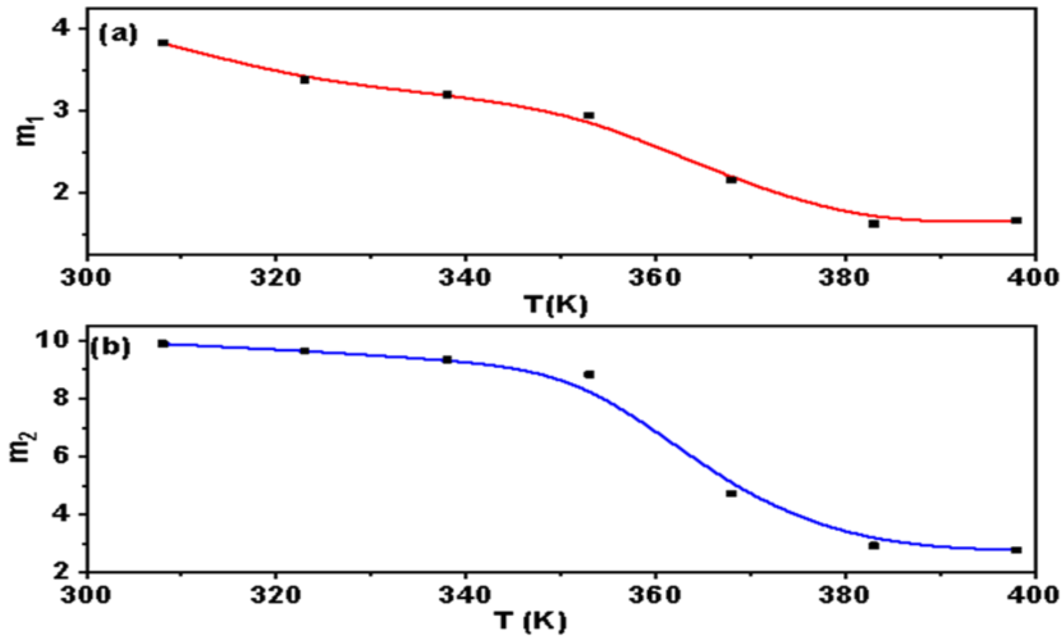

Fig.11. Plot of the slope, m vs. T of Au/In_2Se_3/p-Si/Al heterojunction device **(a)** in the first, **(b)** in the Second voltage region.

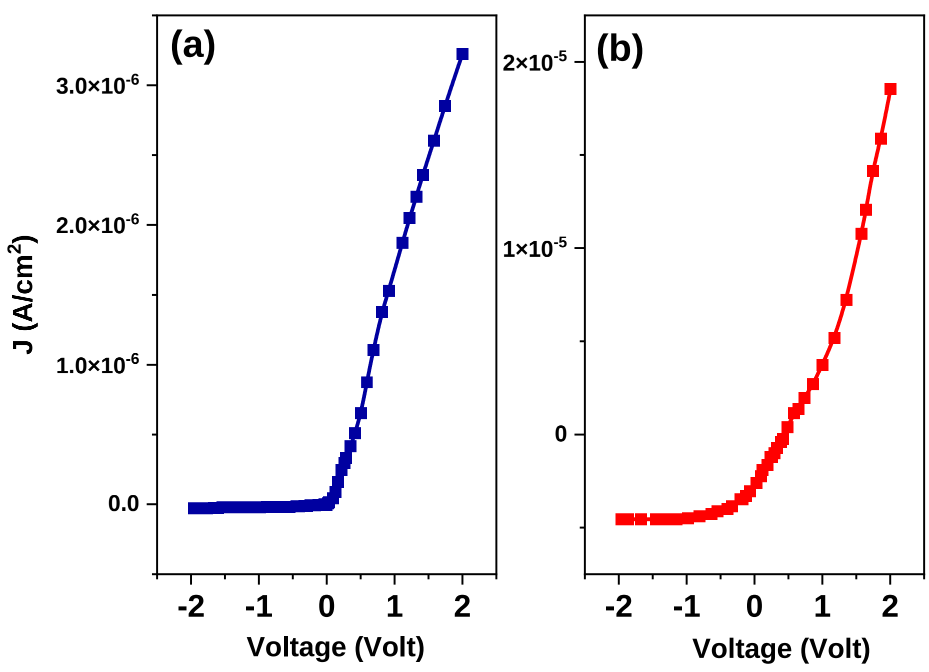

Fig.12. Plot of the J-V characteristics **(a)** dark, and **(b)** illumination of 80 mW/cm^2 of Au/In_2Se_3/p-Si/Al heterojunction device.

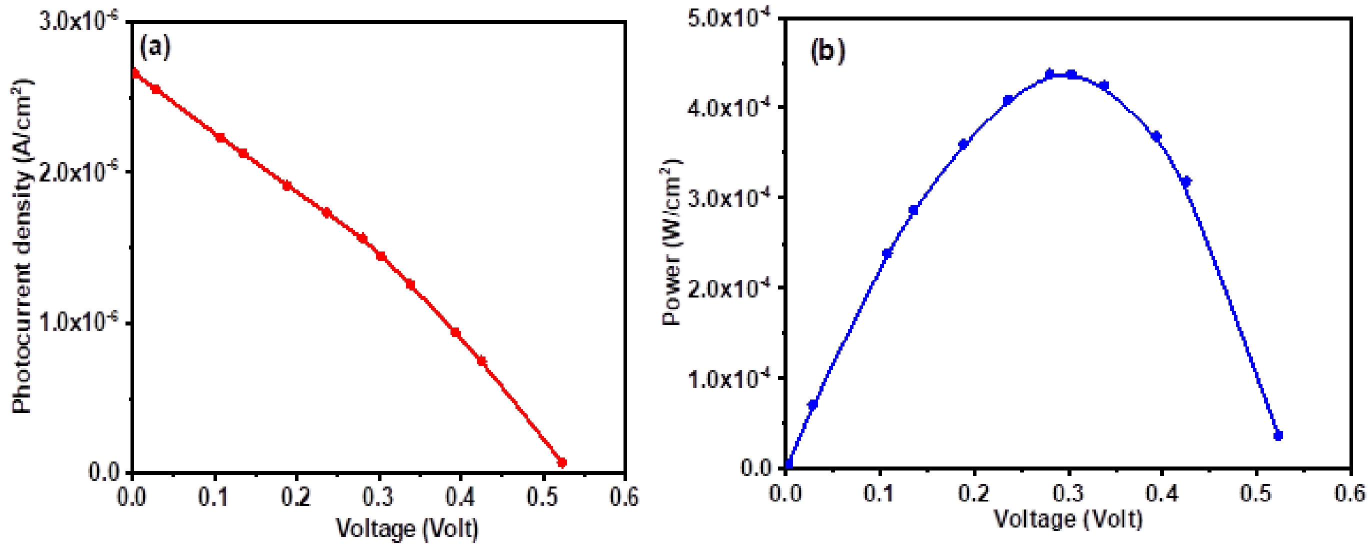

Fig.13. (a) Plot of the JPh-V characteristics, and **(b)** Power-voltage of Au/In_2Se_3/p-Si/Al heterojunction device under illumination of 80 mW/cm^2.

Table (2): The main calculated parameters values of the Photovoltaic under 80 mW/cm^2 illumination

compound	V_{oc}(V)	I_{sc} (A/cm^2)	P_{max}(mW/cm^2)	FF%	Ref.
Au/ In_2Se_3/p-Si/Al in dark under 80 mW/cm^2 illumination	0.53	2.6x10^{-6}	4.37 x 10^{-4}	31.70	**Our study**
In_2Se_3/1M(NaOH+Na_2S+S)/C At 350°c	0.261	-		51.00	**[14]**
n-In_2Se_3|NaOH(1M) +S(1M)+Na_2S(1M) |c(graphite)	0.153	20 x10^{-3}		29.41	**[31]**
ItO/In_2Se_3/$CuInSe_3$/Au	0.256	21.5 x10^{-3}		50.00	**[32]**
Pure In_2S_3	0.630	27.86 x10^{-3}		57.32	**[33]**
In_2Se_3 doped Sn^{4+}1%	0.650	24.23 x10^{-3}		66.54	**[33]**
In_2Se_3 doped Sn^{4+}2%	0.640	27.78 x10^{-3}		69.60	**[33]**
In_2Se_3 doped Sn^{4+}3%	0.660	29.75 x10^{-3}		73.86	**[33]**
In_2Se_3 doped Sn^{4+}5%	0.610	28.79 x10^{-3}		56.36	**[33]**
Mo/CIS/In_2S_3/ZnO	0.666	16.1 x10^{-3}		61.00	**[34]**
Mo/CGs/CBD-In_2S_3/ZnO	0.625	11.5 x10^{-3}		55.00	**[35]**
Mo/CGs/evap-In_2S_3/ZnO	0.785	14.5 x10^{-3}		62.00	**[35]**
β – In_2S_3	0.150	47 x10^{-3}		34.81	**[36]**
Cu_2ZnSnS_4/In_2S_3 (Copper concentration 2.5)	0.491	10.6 x10^{-3}		41.70	**[37]**
Cu_2ZnSnS_4/In_2S_3 (Copper concentration 3)	0.468	11.7x10^{-3}		46.00	**[37]**
Cu_2ZnSnS_4/In_2S_3 (Copper concentration 3.5)	0.395	12.4 x10^{-3}		47.1	**[37]**
Cu_2ZnSnS_4/In_2S_3 (Copper concentration 4)	0.369	12.2x10^{-3}		48.7	**[37]**

Fig. 13 (a) depicts the photocurrent versus voltage under 80 mW/cm^2. Moreover, the relationship between output power and voltage is demonstrated in Fig.13(b). The values of the maximum output power were observed, and they revealed substrate-type dependency. The substrate dependence of the junction for J_{sc} and V_{oc}, which were determined to be 2.6x10^{-6} A and 0.53 V, respectively, is shown in Figs. 13(a) and (b). As observed all the junctions under study exhibit photovoltaic properties with suitable values of J_{sc} and V_{oc}. The likelihood of free charge carrier recombination, a high estimate of series resistance, and a low estimate of R_{sh} [29] are among the limits that can be attributed to these results. The primary photovoltaic parameters are calculated using values for J_{sc} and V_{oc} as well as maximum output current, J_{max} (1.56 x10^{-6} A), and maximum output voltage, V_{max} (0.28 V) [30]. When compared to other junctions, In_2Se_3/p-Si-based junctions achieve acceptable values of J_{sc} and V_{oc}. Fig. 12 (b) also demonstrates the measured fill factor, *FF*, and maximum power, P_{max}, which are determined to be 0.317 and 4.37 x 10^{-4} mW/cm^2, respectively. The observed values of FF and P_{max} in this figure may be compared to the barrier property at In_2Se_3/p-Si-based junctions. This behavior has been attributed by Khan et al. [29] and Phang et al. [30] to the larger ideality factor value because of the effect of surface recombination and high leakage current on the junction performance for photovoltaic characteristics. Comparing the estimated photovoltaic parameter values to those that have been reported in the literature (Table 2) [14,31–37]. The findings showed that the V_{oc} values were found to be greater than those published in [14,31-32,37] and lower than those reported in most of the literature [33-36]. Additionally, it is shown that the J_{sc} and *FF* values that were obtained are lower than those that were reported in the literature [14,31-37], which may be explained by the higher values of the series resistances that can be decreased in future studies.

Conclusions

Thermal evaporation was used to produce the Au/In_2Se_3/p-Si/Al heterojunction. Scanning electron microscopy and transmission electron microscopy studies show that the In_2Se_3 film has a homogeneous morphology with polycrystalline and nanocrystalline structures. The current-voltage curves exhibited diode-like characteristics. As the temperature increased from 308 to 398 K, the values of R_s and R_{sh} for the heterojunction decreased. Two distinct mechanisms were used to explain the forward bias current: thermionic emission with a barrier height of 0.8 eV and a diode ideality factor of about 7.6 estimated at low forward bias and varying as the temperature increased. The device displayed a non-ideal diode due to large values of the ideality factor than unity. The ideality factor, series, and shunt resistances decrease as the temperature rises, while the barrier height increases. The obtained results also demonstrate the presence of lateral inhomogeneity of the barrier height. Under low and high voltage conditions, space charge-restricted conduction may be used to describe the main conduction mechanism of all the junctions that have been researched. The measured photovoltaic parameters for the research provide favorable results and can be enhanced in further work. The obtained results support the applicability of the In_2Se_3/p-Si junction for optoelectronic purposes.

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