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VOLTAGE SAG ENHANCEMENT IN MICROGRID WITH APPLICATIONS ON SENSITIVE LOADS

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ABSTRACT

Although one of the main problems of the power quality is voltage sag in nuclear installations, the terminology used for the compensation devices is different. A Thyristor switched capacitor control is one of the equipment for voltage disturbance mitigation. This paper suggests a Thyristor Switched Capacitor control for mitigation of voltage sag in nuclear research reactor as a sensitive load. Performance of the proposed control investigated under different types of voltage sag magnitudes and is modeled using the user-defined dynamic modeling (UDM) tools in ETAP. The results show appropriate operation of the proposed control system to examine the developed technique.

Keywords: Power Quality, Voltage Sag, Thyristor Switched Capacitor, ETAP

INTRODUCTION

A microgrid has own resources to keep the power quality, mainly the frequency and voltage rated values. The variations of voltage depend on the system reactive power, while the frequency depends on the system active power balance [1].

Power quality is an important issue due to its impact on electricity suppliers, equipment manufactures and customers. The Power quality definition according to the IEEE Standard 1100 "The concept of powering and grounding electronic equipment in a manner suitable to the operation of that equipment and compatible with the premise wiring system and other connected equipment" [2]. Power quality disturbances include phenomena such as voltage sag, voltage swell, flicker, and harmonics distortion [3].

Voltage sag in the electric power system can happen more than any other power quality disturbances [4]. The voltage sag definition according to the IEEE Standard 1159, "The decrease in the root mean square (RMS) voltage level to 10% - 90% of nominal value, at the power frequency for durations of half cycle to one minute" [5]. It is caused by large motors starting or by faults in the electric power system.

The use of Thyristor Switching Capacitors (TSC) is used to mitigation of voltage sag. This paper discusses the aspects of the thyristor switch capacitor control algorithm. Typical operating times of thyristor switching capacitor are in the range of a 5 milliseconds to one second and thus their interrelation with fast voltage sags which operate in the 10 millisecond to one minute [6]-[8].

Thyristor Switched Capacitor Banks Controller

To achieve the design objectives, the thyristor switched capacitor banks controller consisted of three different major components [9]- [12]:

PLC Controller: The operation of the PLC controller is described in figure 1. The band center point shows the middle point of the regulation dead band. Since the operation of the switching capacitor is non-continuous, the switching action is stopped as long as the terminal bus voltage stays within the band defined by the lower and upper voltage limits [13], [14].

The PLC determines how many capacitor banks need to be switched in to compensate the voltage sag as close as possible to the center of the dead band. There is no switching action, when the voltage at the bus return to the band until the bus voltage goes above or below the upper and lower value limits.

In addition, the PLC controller sends signals to the initial operation timer and to the upper and lower voltage exceed timers. Once the initial timer reaches the pre-defined value, a second operational time delay is worked [15]

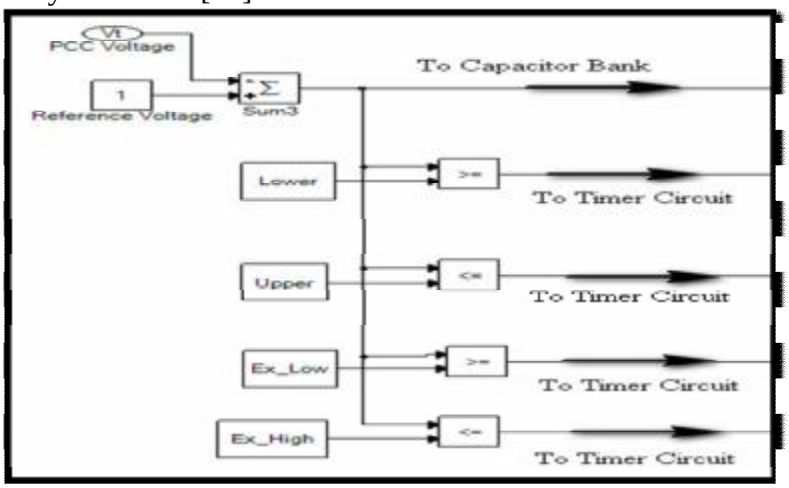


Figure 1: PLC Controller

The Timer Circuit: it consists of an automatic switch, gain, sum, time input and relational operator as shown in figure 2. This implementation is used to illustrate a timer for any other UDM model timer. The output of the timer circuit is directed to the operational time delay circuit. The switching capacitor action occurs after this additional time delay circuit has ended. Only a contactor operational time delay circuit is inserted before switching in or out the capacitor banks [16].

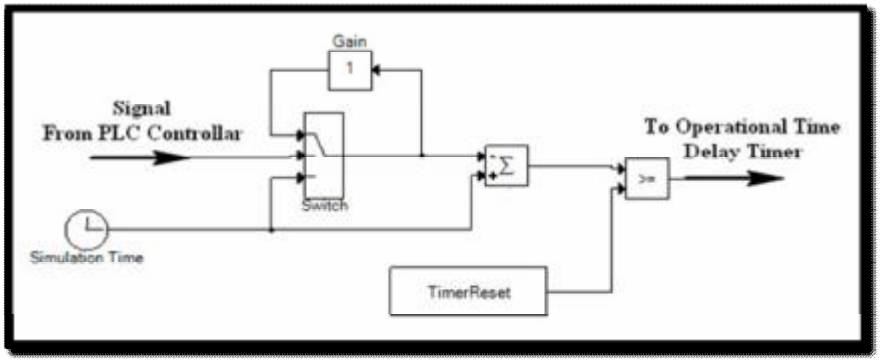


Figure 2: Timer circuit

The controller transfer function has three timers, this timers and their application are inserted in table 1. The timers are operated by the PLC, lower limits, and upper limits.

Table 1: Timers and its function

Timer	Function
Close switch	Add capacitor
Open switch	Remove capacitor
Operational Time Delay	Working time to change in or out the capacitor banks

The Capacitor Banks: they are designed as constant impedance devices once switched on. The number of capacitor banks required to raise the voltage is predetermined. For the implementation presented in this case, ten capacitor banks were used, each rated reactive power is 0.25 Mvar.
The switching device time delay is designed along with the mathematical representation of the capacitance being added to the system. Figure 3 illustrations the function of constant impedance capacitor banks. The number and size of the capacitor banks are pre-determined based on the desired quantity of correction [17].

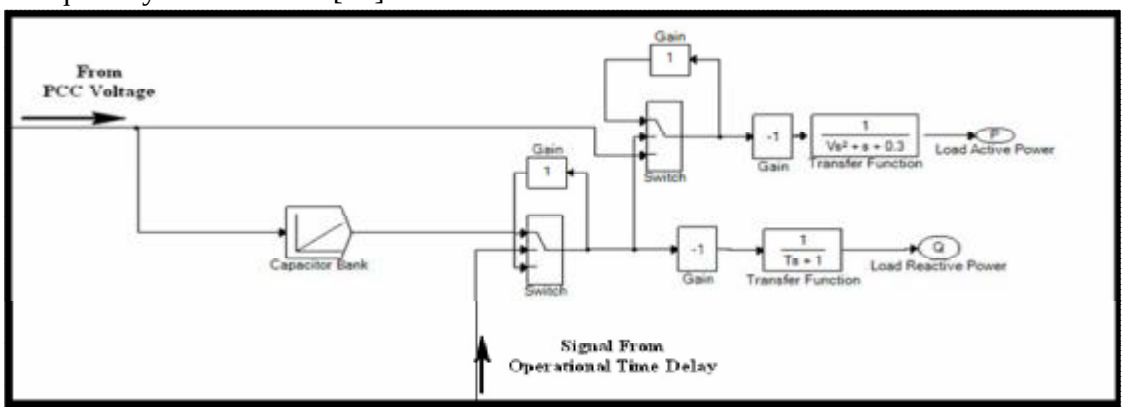


Figure 3: Definite Time Logic Implementation

The amount of banks capacitor is chosen based on the bus voltage to sense the voltage. After the timer retard, the capacitor banks are switched to adjust the reactive power. The desired voltage is adjusted to increase the general implementation of the system. If the bus voltage value exceeds the upper or lower thresholds, then the required numbers of capacitor banks are immediately switched in or out to avoid the system extreme conditions [18].

SIMULATION USING ETAP

In this paper, the application of thyristor switched capacitor bank in the nuclear research reactor is built in ETAP 12.6.0. A feeder with short-circuit power S_{sc} =65 MVAsc connected to the 11 kV bus, bus 2 which is Point of Common Coupling (PCC) connected to the 11 kV bus via 500 kVA (11/0.4 kV) transformer. There are four lumped loads 100KVA for each, two static loads and the other are motor loads. In addition, Lumped load 5 is an external load and connected in bus 6. The one-line diagram is shown in figure 4, and the relevant element parameters are shown in the diagram.

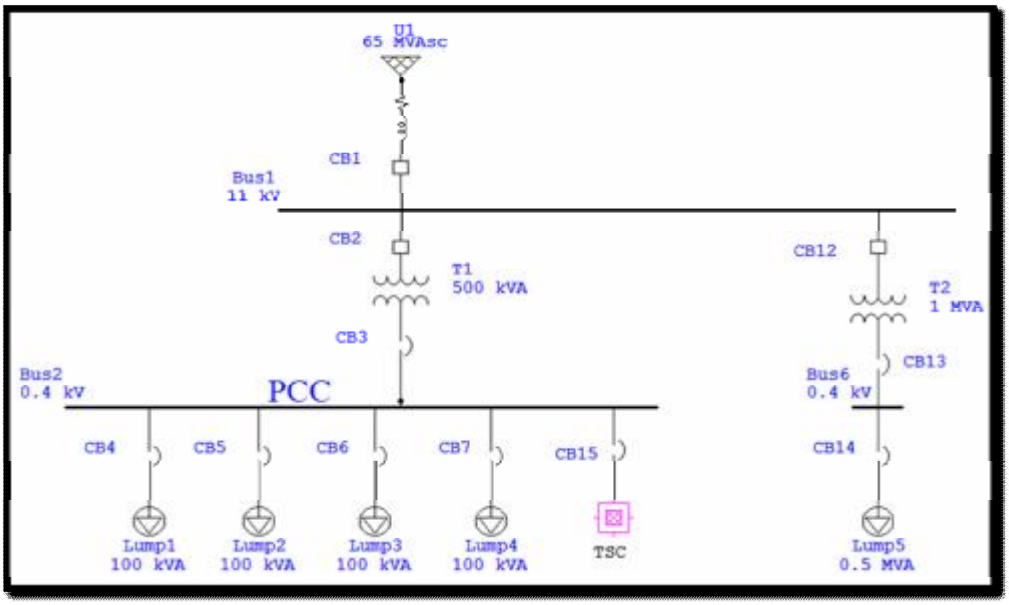


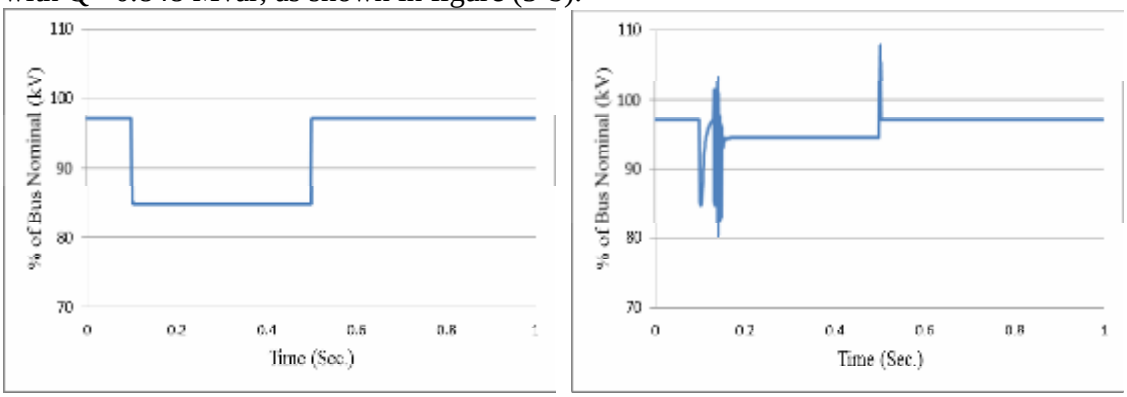
Figure 4: Circuit model in ETAP 12.6

When a three phase fault occurs in bus 6 for duration of 400 ms, from t = 100 ms till t = 500 ms, the PCC senses this fault as voltage sag. We can mitigate the voltage sag by using thyristor switched capacitor bank.

The proposed TSC is working automatically when the voltage is less than 0.9 pu. It injects reactive power according to the value of the voltage decreased. All the following figures will be divided into two plots (a) the PCC voltage without TSC, and (b) the PCC voltage with TSC.

The PCC voltage with sag 15%:

When The PCC voltage is decreased to 85.84% of its normal value, for duration 400 ms, from t = 100 ms till t = 500 ms, as shown in figure (5-a). The TSC mitigates the PCC voltage to 94.65 % with Q= 0.848 Mvar, as shown in figure (5-b).

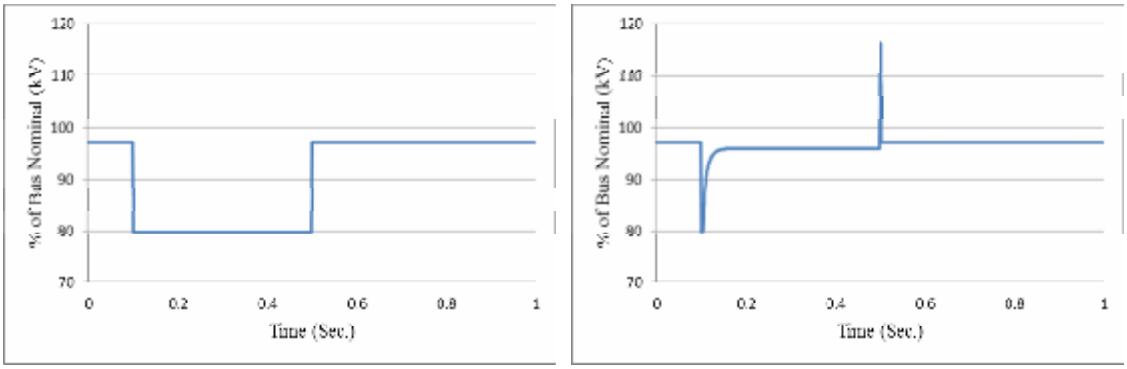


(a) (b)

Figure 5: The PCC voltage with sag 15% plots: (a) the PCC voltage without TSC, and (b) the PCC voltage with TSC.

The PCC voltage with sag 20%:

When The PCC voltage is decreased to 79.75% of its normal value, for duration 400 ms, from t = 100 ms till t = 500 ms, as shown in figure (6-a). The TSC mitigates the PCC voltage to 95.89% with Q= 1.388 Mvar, as shown in figure (6-b).

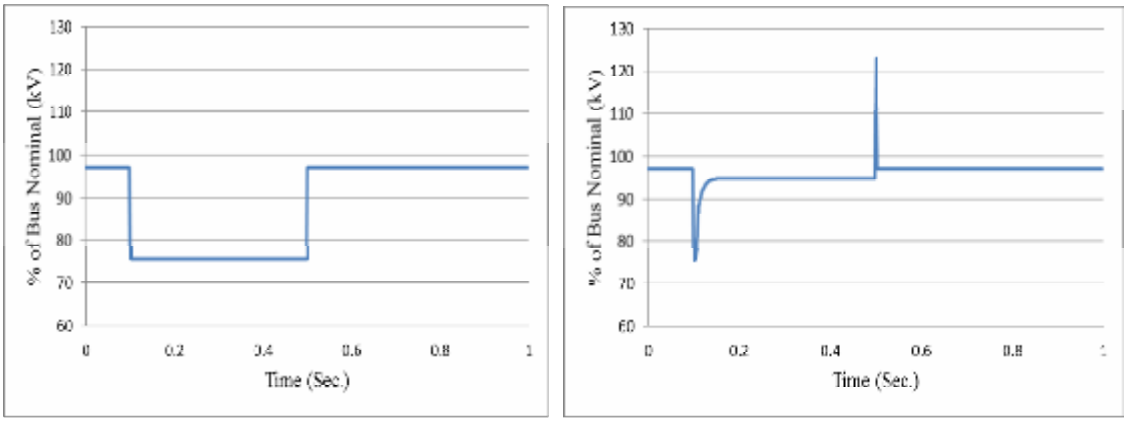


(a) (b)

Figure 6: The PCC voltage with sag 20% plots: (a) the PCC voltage without TSC, and (b) the PCC voltage with TSC.

The PCC voltage with sag 25%:

When The PCC voltage is decreased to 75.50% of its normal value, for duration 400 ms, from t = 100 ms till t = 500 ms, as shown in figure (7-a). The TSC mitigates the PCC voltage to 94.78% with Q= 1.681 Mvar, as shown in figure (7-b).

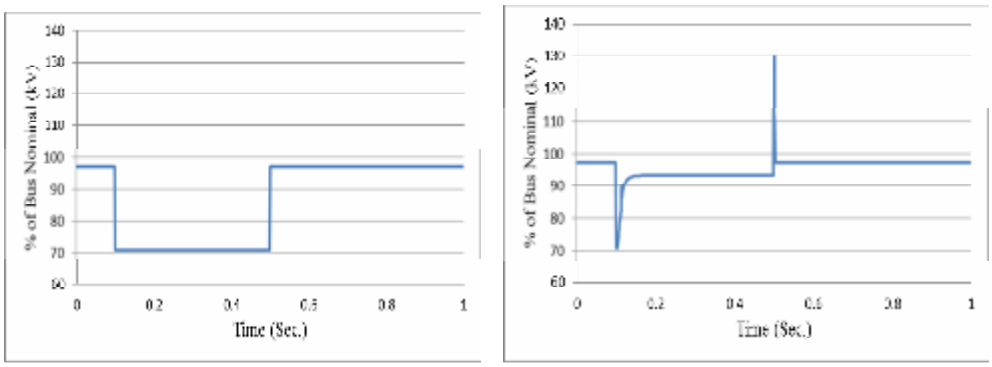


(a) (b)

Figure 7: The PCC voltage with sag 25% plots: (a) the PCC voltage without TSC, and (b) the PCC voltage with TSC.

The PCC voltage with sag 30%:

When The PCC voltage is decreased to 70.80% of its normal value, for duration 400 ms, from t = 100 ms till t = 500 ms, as shown in figure (8-a). The TSC mitigates the PCC voltage to 93.26% with Q= 1.891 Mvar, as shown in figure (8-b).

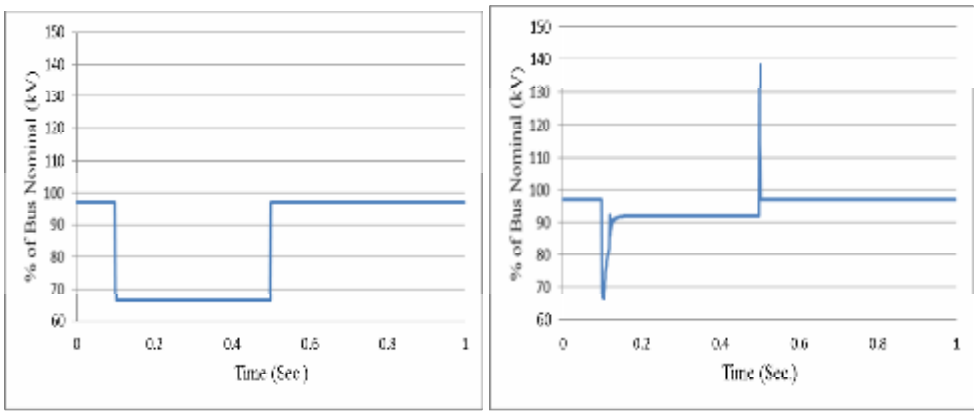


(a) (b)

Figure 8: The PCC voltage with sag 30% plots: (a) the PCC voltage without TSC, and (b) the PCC voltage with TSC.

The PCC voltage with sag 35%:

When The PCC voltage is decreased to 66.36% of its normal value, for duration 400 ms, from t = 100 ms till t = 500 ms, as shown in figure (9-a). The TSC mitigate the PCC voltage to 91.99% with Q= 2.094 Mvar, as shown in figure (9-b).



(a) (b)

Figure 9: The PCC voltage with sag 35% plots: (a) the PCC voltage without TSC, and (b) the PCC voltage with TSC.

Table 2 shows the comparison of the PCC voltage with and without TSC in different type of sag. It can be seen that TSC gave an optimum performance and have the ability to mitigation of voltage sag at PCC bus.

Table 2: The comparison of the PCC voltage without and with TSC

The PCC voltage with sag	The PCC voltage without TSC	The PCC voltage With TSC	The amount of Reactive Power (Mvar)
15%	85.84%	94.65 %	0.848
20%	79.75%	95.89%	1.388
25%	75.50%	94.78%	1.681
30%	70.80%	93.26%	1.891
35%	66.36%	91.99%	2.094

Figure 10 shows the relation between the voltage sag and Reactive Power.

A) The proposed control,

B) The amount of Reactive Power with PCC voltage sag

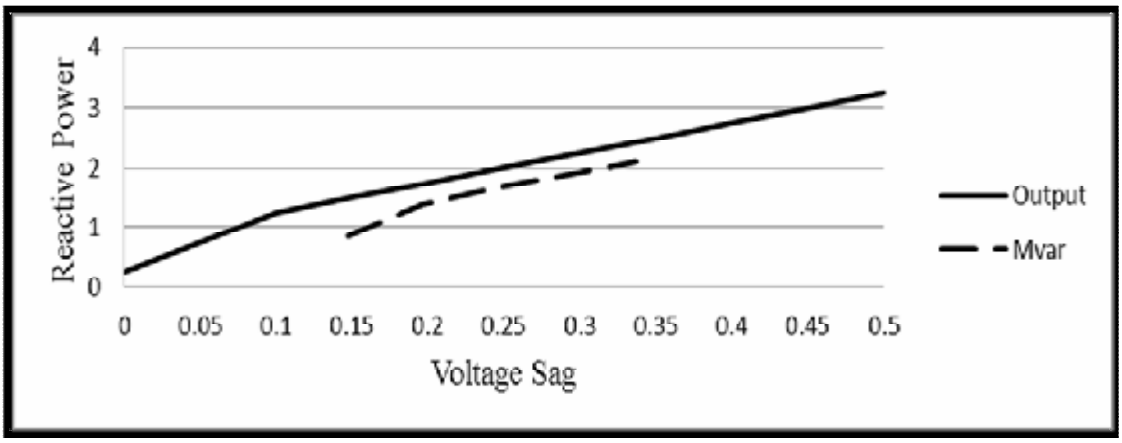


Figure 10: shows the relation between the voltage sag and Reactive Power

CONCLUSION

In this paper, we introduced the voltage sag as one of more occurring than any other power quality phenomena in the power distribution system. Thyristor switched capacitor banks are considered efficient and effective solution for voltage sag mitigation in the nuclear research reactor. Different types of voltage sag magnitude are modeled by using the user-defined dynamic modeling (UDM) tools in ETAP. The proposed control is effective to compensate the sensitive load voltage to the pre-fault value and makes it smooth under different cases of sags.

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