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EXPERMENTAL ANALYSIS OF THE BOUNDARY SCAN AS DESIGN FOR TESTING TECHNIQUE

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ABSTRACT

Boundary Scan testing is the IEEE Standard 1149.1 that overcomes many of the drawbacks of the other traditional test techniques. Boundary scan architecture enables us to go step in the direction of the portable testing systems. Designing testable circuits and interfacing it with the portable computer evaluate the design as a real time application. Therefore, IEEE-1149.1 boundary scan architecture is presented in this paper. A testing architecture of the boundary scan, designed for FPGA, is implemented and evaluated. Channel card of multiplexer is selected as a case study for this evaluation.

KEY WORDS

DFT, ICT, Boundary scan, IEEE Standard 1149.1

1. INTRODUCTION AND BACKGROUND

Functional testing is the original method of testing electronics, where the growing complexity of modern systems has made functional test preparation a lengthy job, while the fault coverage of such test programs may remain unknown. By providing direct electrical access to the components on a Printed Circuit Board (PCB) via an electromechanical "bed-of-nails" test fixture, it was possible to test for manufacturing faults. However along with newer fine line PCBs and more complex array style IC packages, test access has become severely limited. Test fixture technology does not keep up with the ever decreasing dimensions of pins and pitches and the higher pin-counts of packages. During manufacturing, the In Circuit Testing (ICT) and other methods that rely on physical access cannot provide adequate test coverage for today's PCBs due to the lack of the accessibility of the nodes. To complement ICT with access-free test, a new test methodology called boundary scan has emerged [1].

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The incorporation of boundary scan technique capability inside a VLSI chip is increasingly desirable. Boundary Scan IEEE 1149.1 standard describes a special method for testing digital components on the PCBs. The boundary scan technique offers a convenient alternative to physical probing by effectively migrating the test probe circuitry into the chip as shown in Fig.1. It enables a non-contact method of accessing chip pins for testing that achieves the controllability and observability. The work in [2] says that Boundary scan testing coexists with more traditional functional test methods that test digital circuitry by exercising it in a manner that approximates the function for which it was designed. Boundary scan assures that the unit under test is free of shorts and opens.

2. IEEE 1149.1 BOUNDARY SCAN STANDARD

a) BASIC IDEA

This paper introduces the testing structure approach based on the boundary scan architecture, protocol, and required instruction sets, designed for FPGA. It includes a Test Access Port (TAP) controller, scan register; boundary scan registers necessary to execute the Boundary Scan (BS) commands like: External Test Instruction (EXTEST), Bypass Instruction (BYPASS), Internal Instruction (INTEST) and Sample outputs/Preload inputs (SAMPLE/PRELOAD).

b) BASIC ARCHITECTURE OF THE STANDARD

Boundary-scan architecture uses a boundary-scan cell (BSC) at every I/O pin as illustrated in Fig.1 which can interrupt normal data, sample data and inject test data according to the IEEE1149.1 instruction set. The boundary-scan register cells (BSCs) are interconnected to form a scan path between a test data input (TDI) pin and a test data output (TDO) pin. During normal IC operation, input and output signals pass freely through each BSC, from the normal data input (NDI) to the normal data output (NDO). However, when the boundary-test mode is entered, the IC's boundary is controlled in such a way that test stimulus can be shifted in (at TDI) and applied from each BSC output, and test response can be captured at each BSC input and shifted out (at TDO) for inspection [3].

External testing of wiring interconnects and neighboring ICs on a board assembly is accomplished by applying test stimulus from the output BSCs and capturing test response at the input BSCs. As an option, internal testing of the IC core logic can be accomplished by applying test stimulus from the input BSCs and capturing test response at the output BSCs. The complete test architecture consists of the boundary-scan register, a one-bit bypass register, an optional device identification register, other optional user data register(s), a single instruction register, and the JTAG TAP controller [3, 4]. The basic architecture of IEEE- 1149.1 standard, incorporated at the chip level. The basic two pins are for serially shifting data into and out of the chip, referred to as Test Data Input (TDI) and Test Data Output (TDO) [5].

The TAP controller (TAPC) recognizes the communication protocol. It generates the control signals, required for correct operation of all controlled blocks, and performs a number of different operations as in Fig 2. The Instruction Register (IR), controlled by the TAP, is placed between TDI and TDO for loading serially shifted instruction data. IR is used to set the mode of operation for one or more test data registers. Test data registers, controlled by the TAP, are also placed between TDI and TDO for loading serially shifted data. Data registers have two mandatory registers which are the Bypass Register (BYR) and the Boundary Scan Register (BSR). Another register is described by the standard, the Device Identification Register, but is optional. The addition of user-defined data registers are allowed as well.

The instruction Register (IR) defines the mode in which test data registers will operate and determines the test sequence to be performed. The instructions can perform multiple functions. They allow the testing of off-chip system logic and the board level interconnects, sampling chip input and output signals without influencing them, and activating BIST operation on the system circuitry of the chip. The IR is composed of an instruction shift register and an instruction shadow register. The instruction shift register is parallel loaded at the CAPTURE-IR state and its contents are shifted one bit towards TDO on each rising edge of TCK for as long as the FSM remains in the SHIFT-IR state. The contents of the instruction shift register are transferred to the instruction shadow register on the falling edge of TCK in the UPDATE- IR state [6]. The instruction shadow register is necessary to prevent the intermediate contents of the instruction shift register from being acted upon by the TAPC decoder while shifting is in progress, which could otherwise lead to undesired operation of the test logic.

In this section, the design on the chip is tested. The control signals which are applied on timing simulation (TMS, TCK) with test data input TDI are combined and recorded all the transitions as a digital vector input to the design in decimal format in a table. Then, the computer is used to apply these signals to the design on chip and to capture the data results (TDO) from the design on chip using the interface circuitry. The measured results are investigated using the computer to compare with the expected results.

All boundary scan instructions set operational modes which place effectively a selected test data register between TDI and TDO. The function of this register is dictated by the instruction currently loaded (active) in the IR. Some test data registers are composed of a shift register part, referred to as capture (CAP) register, and a shadow register part, referred to as update (UPD) register, similar to IR. Other test data registers are simpler because they do not require an UPD register.

The standard defines two mandatory test data registers, the boundary scan register (BSR) and bypass register (BYR) [7, 8]. A third optional test data register, the device identification register (Device ID register), may also be incorporated into a design. The designer is also free to add user-defined data registers, to provide support for additional test features.

Boundary scan register (BSR) has a boundary scan cell adjacent to each digital chip input and output pin (but not the TAP pins). This register enables the logic levels present at the chip pins to be sampled during normal operation. It allows the testing of off-chip system logic and the board level interconnects. The other optional mode of operation injects test data into the chip inputs and captures the response at the chip outputs, testing the internal system (core) logic through the TAP [9].

The tri-state and bi-directional I/O pads require both data and control signals, the scan cells used for such system pins must be able to control and observe the logic levels on both the data and control signals. However, when a group of pins share a common control signal, a single scan cell may be provided for the control signal, which is then used to control and observe the operating mode of each pin within the group simultaneously [10].

Bypass register (BYR) consists of only one scan cell. The data, presented at TDI on the rising edge of TCK in the SHIFT-DR state, will appear on TDO on the following falling edge of TCK. In the CAPTURE-DR state, it is required that the BYR loads a fixed logic 0 which is subsequently shifted out. This will be useful for chain integrity testing. Since the BYR is not provided with an UPD flip-flop, the UPDATE-DR state has no effect on the BYR. When the BYPASS instruction is loaded, the BYR shortens the shift path within a chip to a single cell. This shortens the length of the scan path of the board under test, thus reducing time required to shift data in and out of the active test chips.

3. IMPLEMENTATION OF THE BOUNDARY SCAN ARCHITECTURE

This section presents the complete design/implementation of the IEEE 1149.1 Boundary Scan hardware architecture on an FPGA chip. A desired stimuli is set on CUT inputs by a PC as master controller and TAPC of BS as slave controller. After that, instruction is loaded on IR. then, the selected operation will be executed and the result is shifted out through TDO of JTAG. A comparison is done between the results and stored (expected) output.

As shown in Fig.3, PC is used as master controller and TAPC of BS as slave controller to set the desired stimuli on the CUT inputs and observe the response by PC. After that, instruction is loaded on IR, and, selected operation will be executed and the result is shifted out through TDO of JTAG. A comparison is done between the results and stored (expected) output. If the comparison is equal, then the result is (PASS), else will be (FAIL).

4. EXPERIMENTAL RESULTS

a) INTEST Operation

The optional INTEST instruction places the IC in an internal boundary-test mode and selects the boundary-scan register to be connected between TDI and TDO. During

this instruction, the boundary-scan register is accessed to drive test data on-chip via the boundary inputs and receive test data on chip via the boundary outputs.

The instruction INTEST is a pin-permission operational instruction and the standard does not specify an instruction bit pattern for it. It is similar to that of the EXTEST instruction, but it is intended to test the internal system (core) logic of a device. It connects the BSR between TDI and TDO. It puts the system (core) logic inputs under control of the BSR input cells. The BSR output cells, connected from core logic outputs, sample the logic values produced by the core logic at the CAPTURE-DR state. Thus, at the UPDATE-DR state, a test pattern can be applied to the core logic inputs, and at the CAPTURE-DR state, the results of that test can be sampled. These results can be shifted out and a new test pattern can be shifted in. While this is happening, the logic values, driven to the output pins, are controlled by the BSR output cells so that known safe values are held during the test. Board level conflicts can be controlled by assuring that the chip outputs are held to benign values by the BSR. The INTEST instruction differs from EXTEST instruction in that the system logic may be clocked for a desired number of clock cycles which may be derived from TCK, before the test results are captured. The steps below illustrate this operation:

1-The code for INTEST instruction is no longer defined (left to designer) which is (xxxx10).The first four bits describe the state of TAPC of BS standard
2-Test patterns are entered to TAPC resetting it to load the instruction registers as in Fig. 4a.
3-Shift in the test patterns to CUT inputs/outputs, bit by bit, (16 input+52 output=68) as in Fig. 4b. This DR scan will be repeated 68 cycles until shifting all test pattern.

b) BYPASS Operation

Its purpose is to produce a short one-bit shift path through a chip, and for this chip to operate normally. This instruction must be selected by the binary instruction code consisting of logic 1 in each instruction register stage. The standard also states that all unused instruction codes, not declared to be user-defined, must also decode to BYPASS instruction. The steps below illustrate BYPASS operation:

1-The code for BYPASS instruction is defined by standard 1149.1 which is (xxxx11).The first four bits describe the state of TAPC of BS standard
2- Test patterns are entered to TAPC resetting it and loading the instruction registers.
3- Shift in the test patterns to CUT inputs/outputs (16 input+52 output=68).
4- The test data output from TDO is extracted and compared to stored correct response (signature) and the result will be (PASS) or (FAIL).

5. CONCLUSION

This paper presents the implementation of the boundary scan architecture on FPGA. Design and implementation of Circuit under Test with the boundary scan architecture on FPGA are presented. Finally, experiments, results, and conclusion are presented. Table I shows the device utilization summary for channel card itself and this channel card with the implementation of boundary scan. As an updated manufacturing DFT guidelines to implement boundary scan architecture, we can refer to reference [12].

TABLE I. DEVICE UTILIZATION SUMMARY

Device Utilization Summary						
Design Type	Channel Card			Channel Card with BS		
Logic Utilization	*Used*	*Avail-able*	*Utili-zation*	*Used*	*Avai-lable*	*Utili-zation*
Number of Slice Flip Flops	806	1,920	41%	910	1,920	47%
Number of 4 input LUTs	1,124	1,920	58 %	1,303	1,920	67%
Number of Occupied Slices	853	960	88%	936	960	97%
Number of Slices containing only related Logic	853	853	100%	935	935	100%
Total number of 4 input LUTs	1,262	1,920	65%	1,441	1,920	75%
Number used as logic	1,040			1,219		
Number of bonded IOBs	64	66	96%	27	66	40%
Number of BUFGMUXs	2	24	8%	3	24	12%
Average Fan out of Non-clock Nets Non-clock Nets	3.52			3.56		

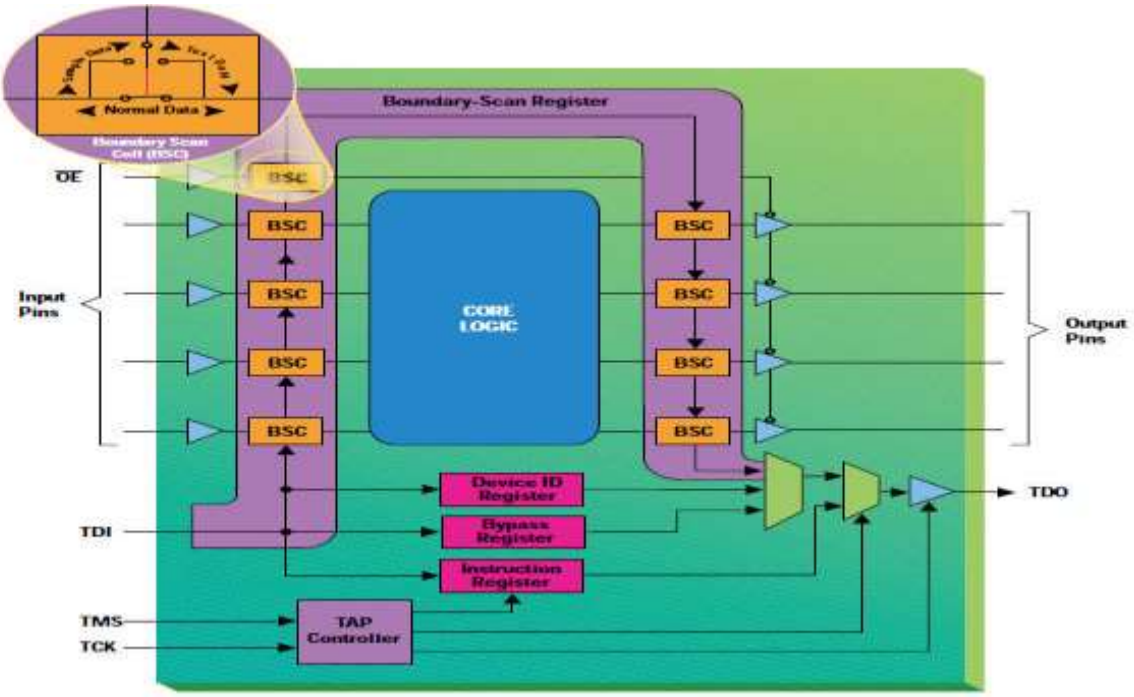

Fig.1. Basic architecture of IEEE-1149.1 standard

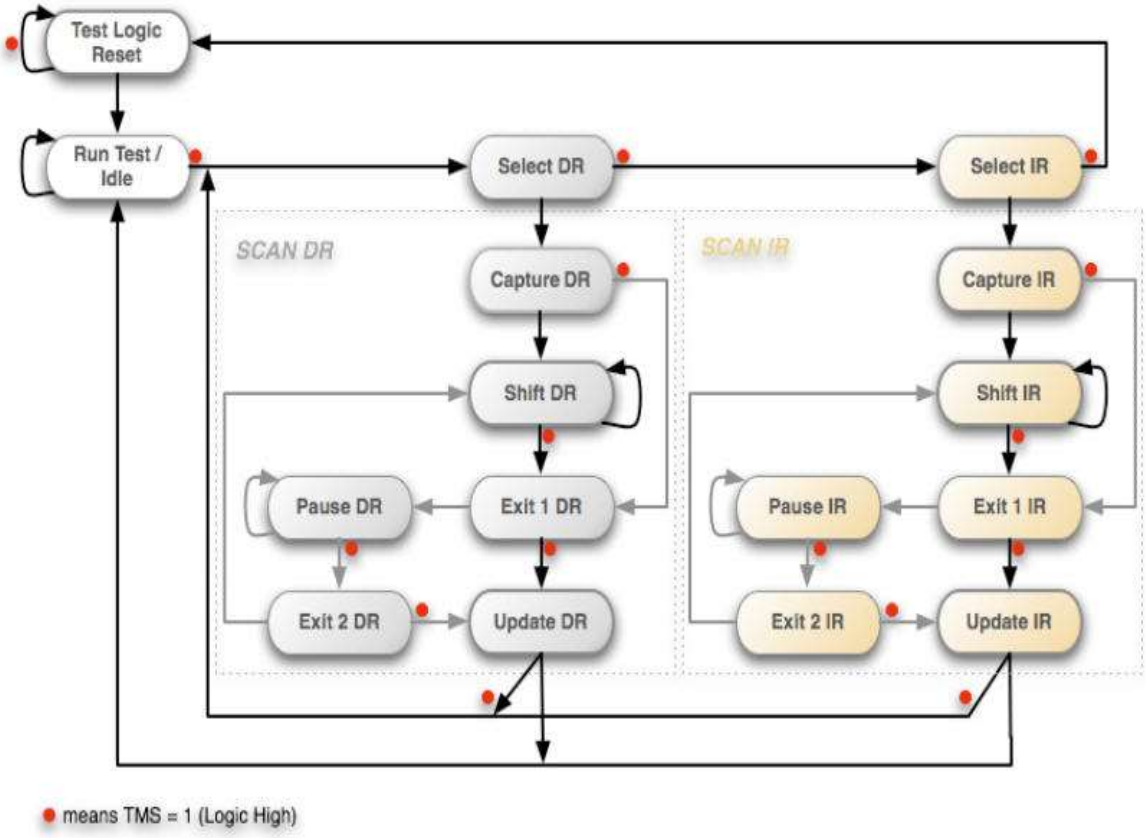

Fig.2. .TAP Controller communication protocol [6].

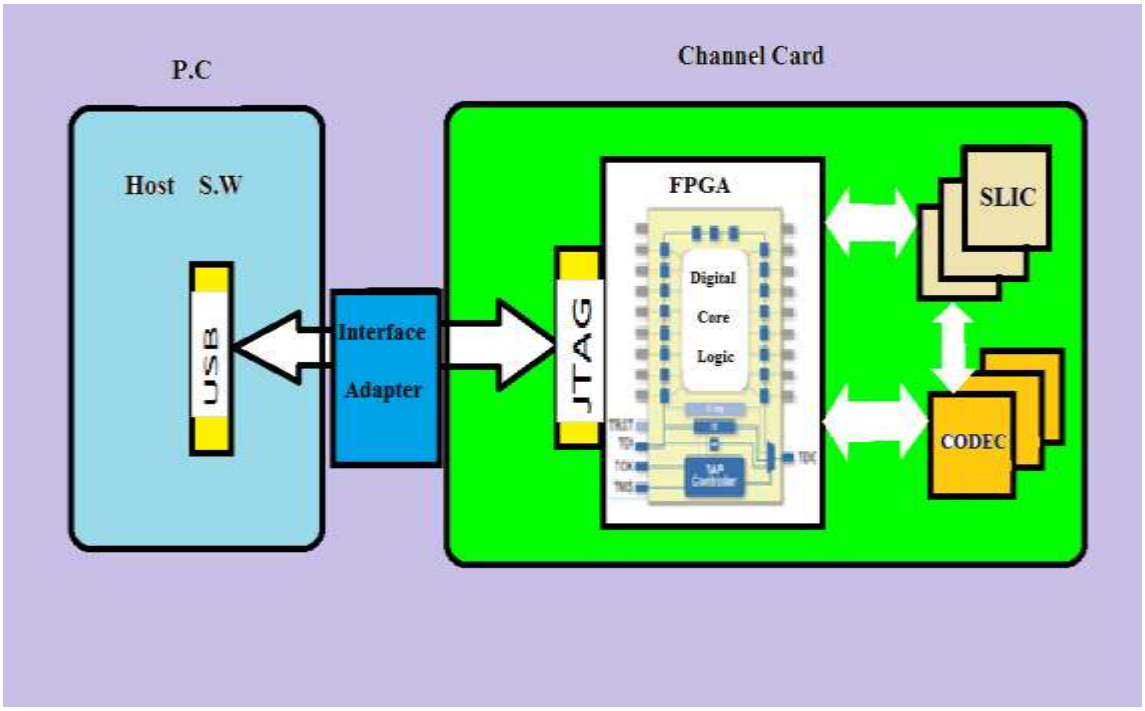

Fig.3. Block diagram of the Top Design with a Typical JTAG Interface

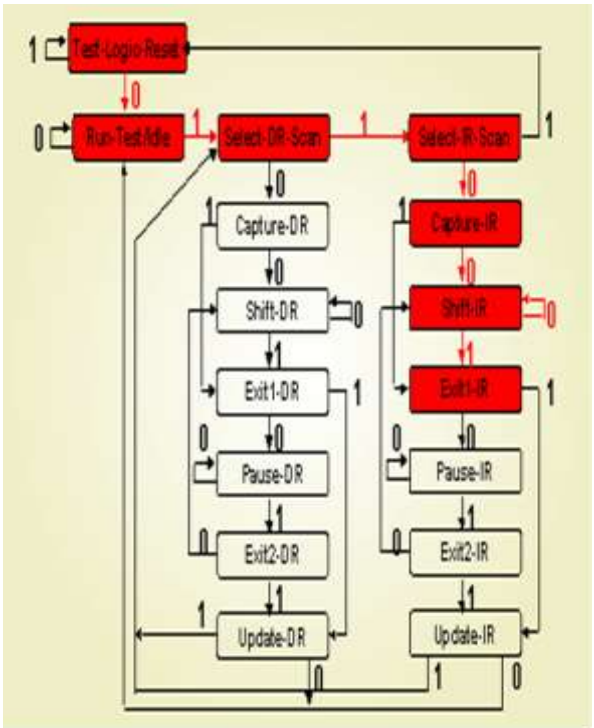

Fig.4a. Instruction shifting cycle

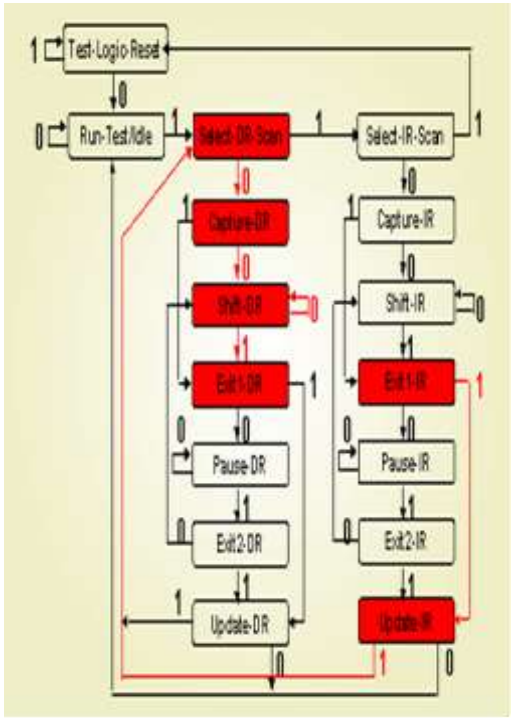

Fig.4b. Data shifting cycle

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