Photonic Crystal OR Gate with Minimum Size and Ring Resonator Based Structure

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Abstract*— The OR-gate structure is proposed in this paper. It can be constructed in different topologies such as ring resonator, self-collimation, waveguide, and cavity-based structures. Linear and nonlinear materials are used to realize this gate in the literature. The proposed design is formed in a linear photonic crystal square lattice based on ring resonator topology. By applying sensitivity analysis; OR-gate is identified. Minimum area structure and high bit rate are the remarkable characteristics for this design. The minimum size of 56.16 μm², and the bit rates of 2.5 Tb/s are obtained. The phase shift between the input powers and their effect are examined carefully to achieve two new gates. Comparative table is formed for the OR-gate based on ring resonator topology. This structure is designed, and simulated at 1.55 μm wavelength.

***Keywords*-- OR-gate, Photonic crystals, Ring resonator, Bit rate, Contrast ratio.**

I. Introduction

Minimum size circuits and ultra fast digital processing are the main aims for modern technologies. The semiconductor materials led to the manufacture of various electronic circuits [1, 2]. Combinational and sequential logic designs were fabricated to execute arithmetic and logic operations [3]. The mandatory needs for high data rate let the electronic devices oppose a problem to do that. Semiconductor optical amplifiers (SOA) [4], periodically poled lithium niobate (PPLN) waveguides [5], and photonic crystal (Ph. Cs.) [6] are some representation forms to realize high-speed applications and small size designs in an optical regime.

The usage of light as the source for photonic crystal (Ph. Cs.); provides to develop high speed applications like sensors [7], filters [8], logic gates (i.e., AND, OR, XOR) [9], multiplexers and demultiplexers [10, 11], flip-flops [12], encoders [13], decoders [14] and half adders [15]. (Ph. Cs.) can be constructed from artificial crystals that have highly ordered dielectric materials with of light control propagation [6]. Photonic band gap (PBG) prevents light to present in a particular wavelength range likewise the electronic band gap forbids electrons in a certain region [6].

Ring resonator [16], self-collimation [17], cavity [18], and waveguide [19] are the topologies that are used to implement (Ph. Cs.) applications. All of them could be shown in square or hexagonal lattice type. RSOFT [20], COMSOL [21] are two software packages that are used to simulate and evaluate (Ph. Cs.) structures.

In this paper, two dimensional (Ph. Cs.) OR logic gate ring resonator based is carefully explored and tested. The figures of merits such as: the size of the structure, bit rate (BR), contrast ratio (CR), and linearity will be represented. Phase shift between the two inputs is applied to examine its effect on the gate behaviour.

This paper is organized as follows. Section II reports the structure details. Simulations and results can be found in sections III. The conclusions are introduced in section IV followed by the most relevant references.

II. Structures Details

A. Basic Concepts

The OR- gate is considered one of the digital logic components. It exists with other gates to build more complex circuits. It is a type logic whose output goes high when at least one input is high. However, the output goes low when all inputs are low. The Boolean expression is defined as in (1) [3]:

$$Q=A+B \quad (1)$$

B. Structure Description and Dimensions

The proposed structure is built on a two-dimensional (Ph. Cs.) square lattice floor with a lattice constant (a) (i.e., the distance between the centre of two rods) of 0.6 μm. It has (12X13) Silicon (Si) rods in a background of air. All the rods have rod radius (r) = 0.12 μm and the same material with refractive index (n) = 3.4. The design is shown in Fig. 1. The ring resonator is the basic element in the proposed design. Scattering rods are carefully positioned (i.e., marked in blue). Two rods are adjusted in the ring resonator (i.e., marked in green) to verify the intended logic gate. The position of the output ports is selected by applying sensitivity analysis.

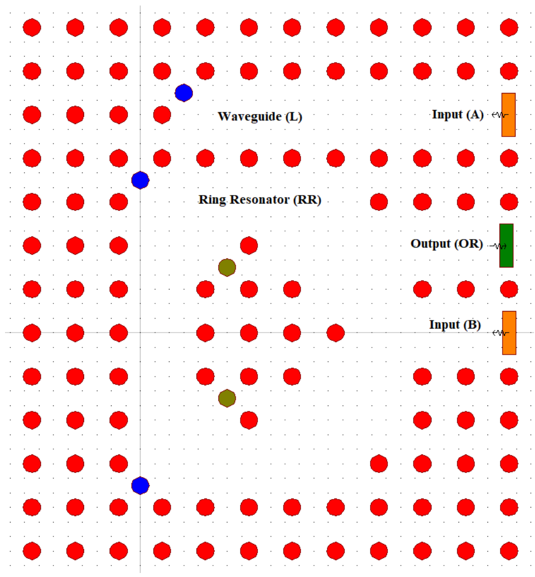


Fig. 1 The proposed structure for OR and XOR logic gate.

III. Simulation of the Proposed Design

A. Numerical Methods and Photonic Band Gap (PBG)

Finite-difference time domain (FDTD) is one of the numerical methods that are used to simulate (Ph. Cs.) structures. The power distribution, the time response, and the power level for each state are displayed. The (PBG) is calculated by using plane wave expansion (PWE) method. The design is simulated by applying transverse electric (TE) field.

From Fig. 2, the (PBG) falls in the range between1.429 µm and 2.142 µm. The position of input ports and output port is located as shown in Fig. 1 by using sensitivity analysis. Ring resonator topology is carefully designed to operate in the C-band optical wavelength (i.e., between 1530 to 1565 nm).

B. The Proposed Logic Gate Operation

In this section, the power distribution and the time response are investigated. The results are executed at 1.55 µm wavelength. Four states will be explained in the following section to verify the operation and to extract the valued results. The output power levels are normalized. As shown in Fig.1, the output will be switched on and off based on the state of the two inputs as will be shown.

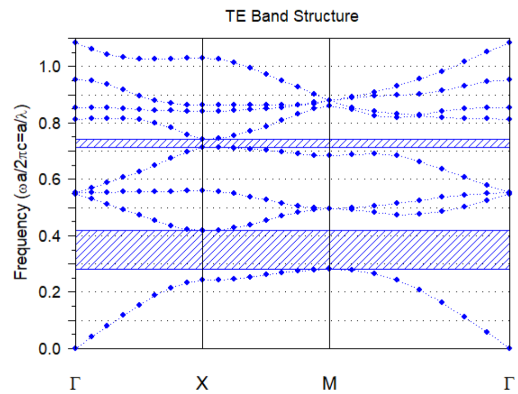


Fig. 2 The photonic band gap of TE- polarization.

1) Case 1: when no power is applied to both inputs, there is no power at the output port.

2) Case 2: when one of the inputs is on (i.e., input A=1, B=0) a light wave will propagate through the waveguide and mutually couple into ring resonator. The power that exists now in the ring resonator is guided with the effect of the scattering rods to arrive to the output. Figure 3, displays this state with output equals 0.6 and which is considered logic (1).

3) Case 3: on the other hand, when the input power lunched through port B (i.e., B=1) and the other port is disabled (i.e., A=0). The applied signal is circulated within the ring at its resonant wavelength (i.e., 1.55 µm) to deliver the power directly to the output port. The output is logic (1) with the power level of 1.0 as shown in Fig. 4.

4) Case 4: when both inputs (i.e., A and B) are logic (1). Figure 5 demonstrates a constructed field is done between the two input beams. The result of this case is to confirm OR-gate operation as the output is equal 1.0.

C. Bit Rate Calculation

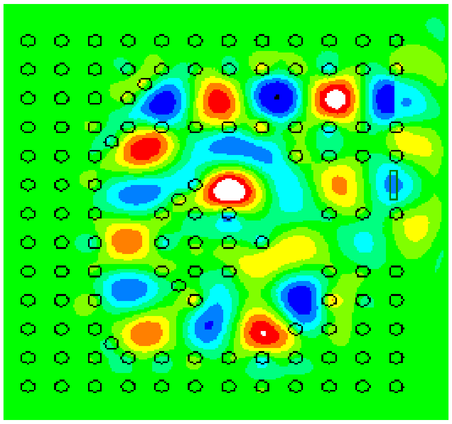
The bit rate is defined as the reciprocal of the response time (RT) as show in (2) [9].

$$RT = t_d + t_r + t_f = t_d + 2t_r \qquad (2)$$

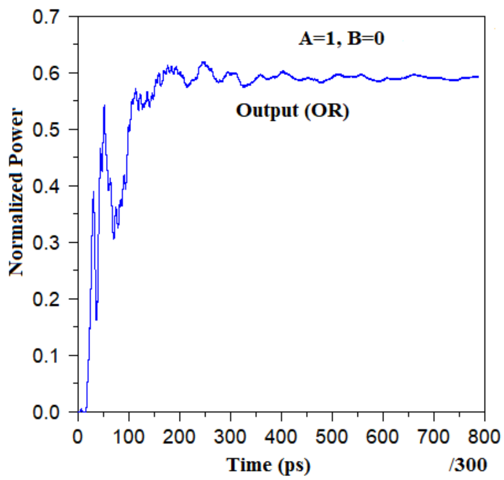
Where the delay time (t_d) is the time taken to go up the output power from 0 to 10% of the steady-state output power. The time that is taken between 10% to 90% of the average output power is called transition time (t_r). The falling time (t_f) is the time for final steady-state power to 10%, which is approximately equal to (t_r) in linear material scenarios as in [9]. The (BR) is calculated from the time response to be 2.5 Tp/s.

D. Phase Shift Effect

The XOR operation can be summarized as: the output will be logic (1) as long as the two inputs are different. On the other hand, the output will be logic (0) when the two inputs are the same [3].

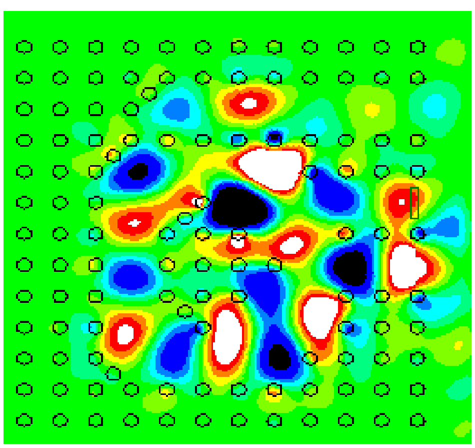


(a)

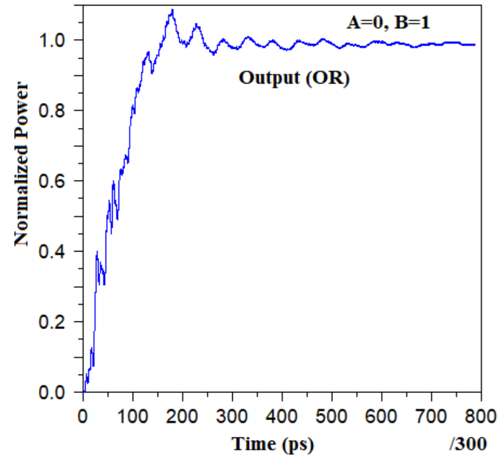


(b)

Fig. 3 A = 1 and B = 0 for (a) power distribution, (b) time response.

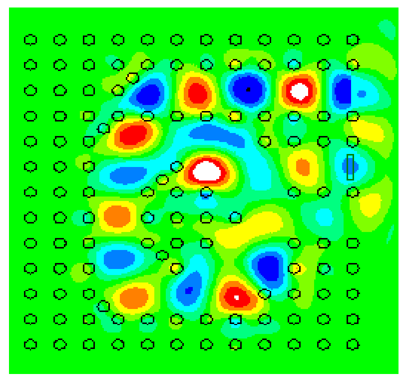


(a)

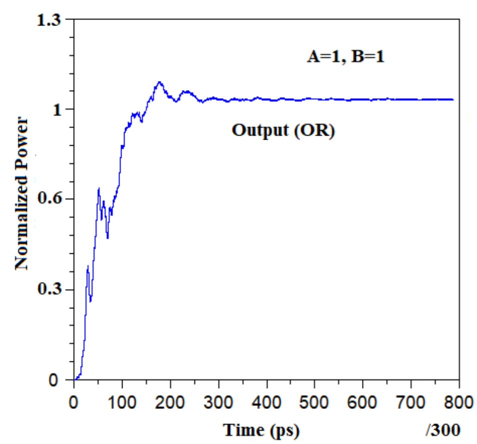


(b)

Fig. 4 A = 0 and B = 1 (a) power distribution, (b) time response.



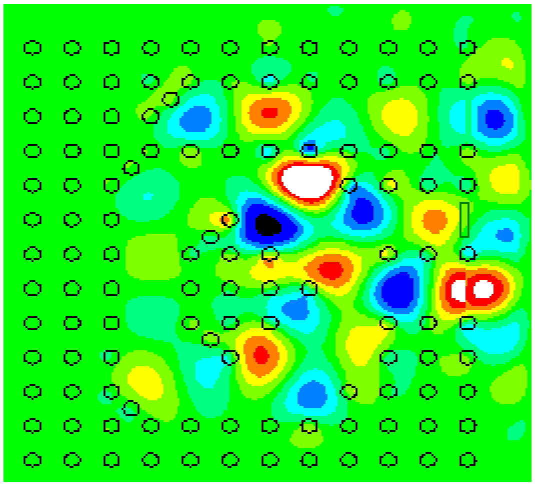
(a)



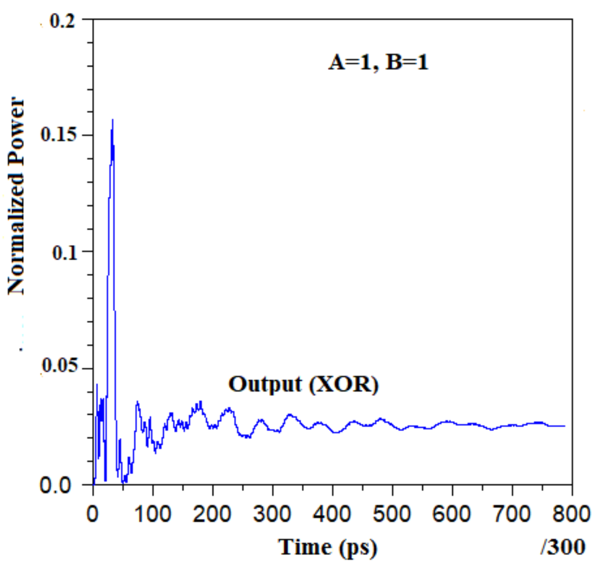
(b)

Fig. 5 A = 1 and B = 1(a) power distribution, (b) time response.

The NOT-gate or what is called inverter has one input-one output port. It provides the negation for the input. This gate needs an auxiliary input to verify its operation. It can be implemented by fixing one input of the XOR to logic (1) (i.e., A=1). By changing the other input (i.e., B), the output will be inverted.



(a)



(b)

Fig. 6 A = 1 and B = 1 with phase shift 180 degree for (a) power distribution, (b) time response.

The (CR) can be computed for the XOR- gate from (3). It is defined as the ratio between the minimum output power for logic (1) and the maximum output power of logic (0) [9].

$$CR = 10 \log (p_1/p_0) \quad (dB) \quad (3)$$

where p_1 is the minimum output power for logic (1) and p_0 is the maximum output power of logic (0). Therefore, the (CR) will be 13.02 dB.

As will be shown, Table I includes the analogy between the proposed structure and its counterpart in the literature. Most of the designs are used (Si) as the rod material. The maximum number of gates appears in [28]. The highest (CR) occur in [45] in a hexagonal shape lattice type with only OR- gate as in Table I. The maximum size with 1287 μm^2 exists in [44]. The intended structure for the OR- gate has minimum size and the high (BR). It can be implemented with the same rod radius. No need for any auxiliary inputs to verify the operation.

TABLE I
COMPARISON BETWEEN THE PUBLISHED ALL- OPTICAL OR TOPOLOGIES IN THE LITERATURE

Ref. and Year	Contrast ratio (dB)	Bit rate (Tb/s)	Size (μm^2)	Auxiliary input	Implemented gates
Ref [22-2015]	16.7	0.33	136	√	OR, AND, XOR
Ref [23-2015]	4.77	0.2	303	√	OR, AND, XOR , NOT
Ref [24-2015]	18.7	0.33	499	√	OR, NOT
Ref [25-2016]	NA	0.8	200	X	OR
Ref [26-2017]	NA	0.33	134	X	OR, AND
Ref [27-2017]	25	0.13	283	√	OR , NOR
Ref [28-2017]	NA	3.8	132	X	OR, AND, XOR, NOT, NOR, NAND, XNOR
Ref [29-2018]	9.29	NA	335	√	OR, AND, NAND
Ref [30-2019]	18	4.7	250	√	OR,AND
Ref [31-2019]	19	0.5	1287	√	OR
Ref [32-2021]	29	5	454	√	OR
Proposed design	NA	2.5	56.2	X	OR

The recent published paper with the same topic can be found in [33]. It has structures to implement the same gates but by using waveguide topology not ring resonator. But the proposed design still has less space.

IV. Conclusion

The OR gate with new proposed design is implemented in this paper. The performance and the figures of merits are calculated. This design operates in linear regime that let them to save the power consumption. FDTD and PWE methods are the two numerical techniques that are used for simulation and analysis. The core for this module is the ring resonator topology. Therefore, the comparison table is organized and concentrate on the same logic with this topology type. The main targets are to verify OR, XOR, and NOT logic gates and to get the minimum size and high bit rate with respect to the other published papers in literature. Phase shift is applied to convert the operation of the OR to XOR gate.

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