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REALIZATION OF KHN AND TT FILTERS USING DDCCTA BLOCK

N. A. KHALIL[1], R. F. AHMED[1], R. A. ABULSOUD[1], A. M. SOLIMAN[2]

ABSTRACT

A new active building block for analog signal processing, namely, Differential Difference Current Conveyor Transconductance Amplifier (DDCCTA) provides the possibility of inbuilt electronic tuning of the parameters of the analog function circuits to be implemented. This block is modified and the performance is checked through PSPICE simulations. A modified block is utilized to realize the KHN and TT filters. The proposed realizations use three DDCCTA for the KHN filter and only one DDCCTA for the TT filter circuit. Also, the resulted realizations are tested via PSPICE simulations.

KEYWORDS:DDCCTA, KHN filter, TT filter.

1. INTRODUCTION

Recently some new analog building blocks, such as current conveyor transconductance amplifier (CCTA) [1,2], current controlled current conveyor transconductance amplifier (CCCCTA) [3], current difference transconductance amplifier (CDTA) [4], current controlled current difference transconductance amplifier (CCCDTA) [5], differential voltage current conveyor transconductance amplifier (DVCCTA) [6], and differential voltage current controlled conveyor transconductance amplifier (DVCCCTA) [7], are reported in the literature. These may be constructed by cascading of current mode building blocks with transconductance amplifier (TA) analog building blocks in monolithic chip for compact implementation of signal processing circuits and systems.

In 2011, the recently new active element called the differential difference current conveyor transconductance amplifier (DDCCTA) was introduced to provide the possibility of inbuilt electronic tuning of the parameters of the analog function circuits to be implemented [8-10].The DDCCTA has the differential difference current conveyor (DDCC) [11,12] as an input stage and is followed by a transconductance amplifier in monolithic chip. It also has all the good properties of the DDCC, such as high-input impedance, employs fewer active of passive components and easy implementation of differential and floating input circuits. Accordingly, many applications of DDCCTA-based circuits were developed [7,10–14] and especially bi-quadratic filters using DDCCTAs as active elements were proposed [7,10,14]. However, they need some external passive resistors for their realizations.

The main intention of this paper is to present equivalent KerwinHuelsman Newcomb (KHN) and Tow-Thomas (TT) realizations using modified DDCCTA block and with all passive elements are grounded.

It is worth noting that the KHN circuit using current conveyors (CCII) was introduced in [15] with a one to one correspondence to the three building blocks in the classical KHN resulting in circuits with four or three floating resistors. Shortly thereafter it was modified to have all grounded resistors and capacitors [16] and to provide all possible eight sign combinations of the three filter responses by changing the polarity of the Z terminal of the CCII [16]. Current mode two integrator loop filters using CCII was also introduced in the literature in [17].Using three or four Differential Voltage Current Conveyor (DVCC) are generated from the basic KHN and inverted KHN block diagrams. The circuits are classified into two types, type A employs three DVCC and type B employs four DVCC [18].

The realization of the TT circuit using the CCII was introduced in [19]. Realization of the TT circuit using the operational trans-resistance amplifiers (ORTA), CCII and the differential voltage current conveyor (DVCC) is reviewed in [20]. The current mode version of the TT circuit using balanced output current conveyors was also realized in [19]. In [21] introduced a new methodology to generate equivalent TT Circuits using CCII and TA.

The paper is organized as follows; the modified DDCCTA is described in section II. In section III, the equivalent DDCCTA-KHN realizations are presented. Also, the realizations of DDCCTA-TT filter are given in section IV. Finally, section V concludes the work.

2. THE MODIFIED DDCCTA

The DDCCTA is a versatile analog active building block consists of differential amplifier, current mirrors, and TA. Here, the CMOS realization of this block, given in [10] and shown in Fig. 1, is modified to get balanced output currents instead of double output currents.

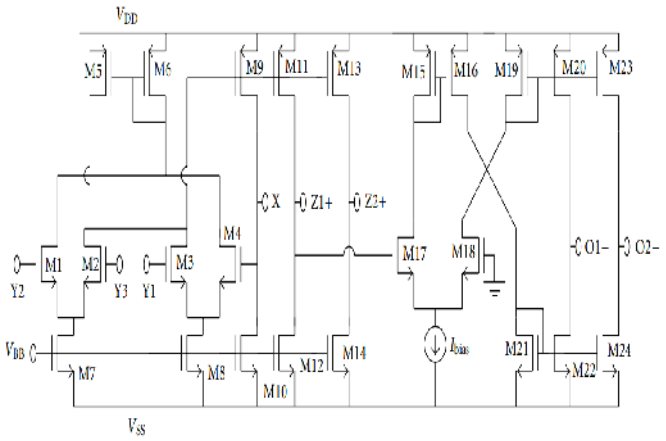


Fig. 1. The CMOS realization of the DDCCTA[10]

The modified CMOS realization is shown in Fig. 2 and the symbol of the DDCCTA is shown in Fig. 3.The port relationships of the modified DDCCTA block are characterized by the following matrix:

$$\begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & -g_m & 0 \end{bmatrix}$$

Where g_m is transconductance of the DDCCTA

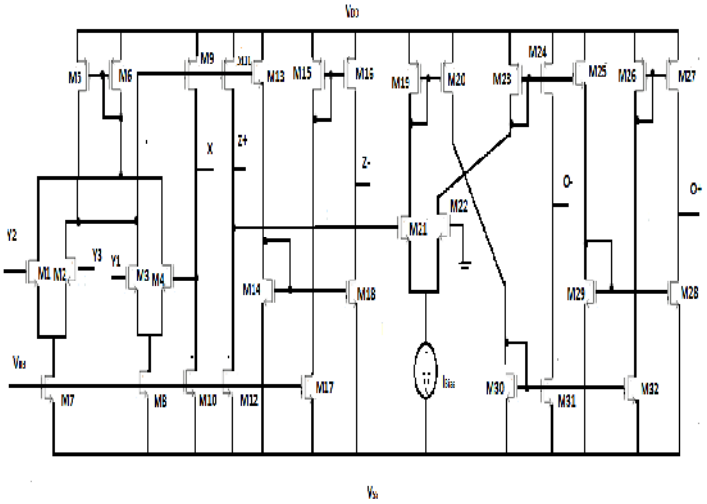


Fig. 2. The CMOS realization of modified DDCCTA [10]

In this case, the transconductance gain (g_m) of the DDCCTA can be given by:

$$g_m = \sqrt{\left(I_{Bias}\frac{W}{L}\mu C_{ox}\right)} \quad (2)$$

Where I_{Bias} is an external DC bias current, μ the effective channel mobility, C_{ox} is the gate-oxide capacitance per unit area, W and L are channel width and length of the MOS transistor M21, respectively. Eq. (2) reveals that the g_m-value of the DDCCTA can be adjustable electronically by I_{Bias}.

To validate the behavior of the modified element shown in Fig. 2, PSPICE simulations have been carried out using 0.25µm CMOS process model parameters. The supply voltages of VDD=−VSS =1.25 V and VBB=−0.9V are used. The aspect ratio of various transistors for DDCCTA is given in Table 1. The DC transfer characteristics of the DDCCTA fromY1 terminal to X terminal are shown in Fig. 4. It is clear that the voltage at X terminal follows the Y terminal voltages in the range of −200 mV to +200 mV with error less than 13mV. The variation of current at Z+ and Z- terminals with X terminal current from −100µA to 1300µA is shown in Fig. 5. This Figure shows that the max current deviation is equal to 13.1348µA. The variation of the output current at O+ and O- terminals among with X terminal current from −100µA to 100µA is shown in Fig. 6. These current variations are plotted for the Z terminal is connected to 10kΩ resistance. It worth noticing that the change of aspect ratio of transistors helps us to

increase the range of transconductance at port O, so we can realize filters with high quality.

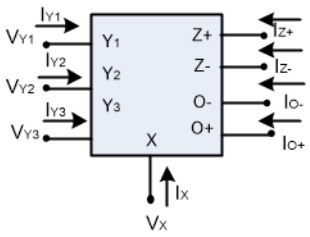


Fig. 3. Circuit symbol of the DDCCTA

Table 1. Aspect ratio of various transistors

MOS Transistor	Aspect ratio(W(µm)/L(µm))
M1 - M4	1.8/0.7
M5 – M6 , M9 , M11 and M13	20/0.7
M7andM8	5.2/0.7
M10 ,M12 , M17	58/1
M14 - M16,M18-M20 , M23 – M32	4/0.7
M21 – M22	1/1

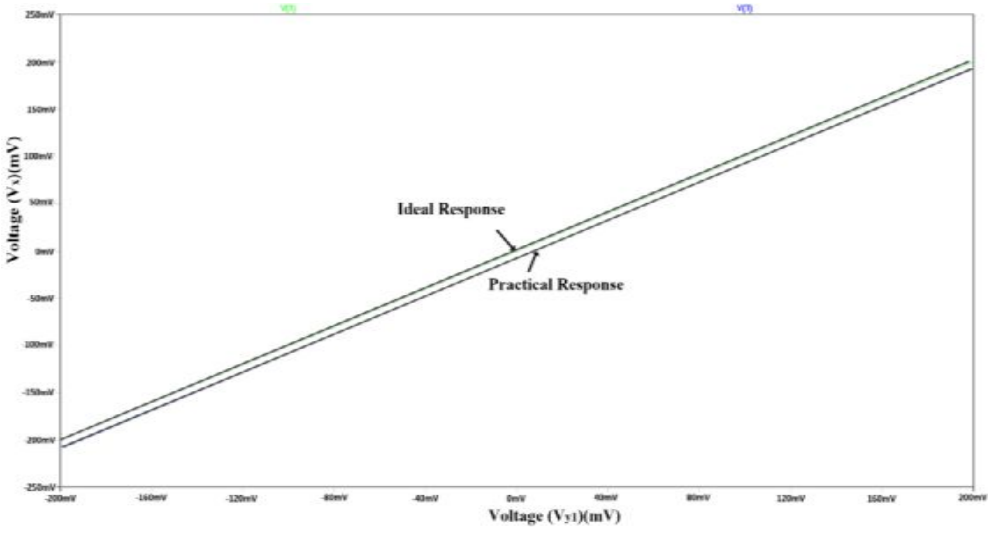


Fig. 4. DC transfer characteristic for voltage transfer from Y1 port to X port

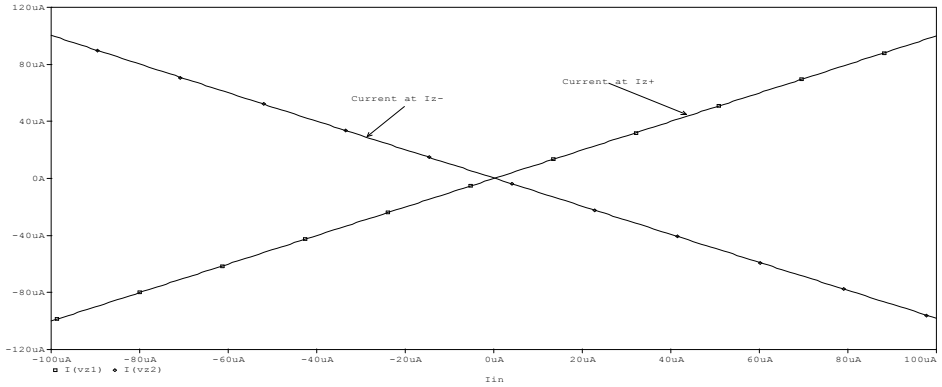


Fig. 5. DC transfer characteristic for current transfer from X port to Z+ and Z- Ports.

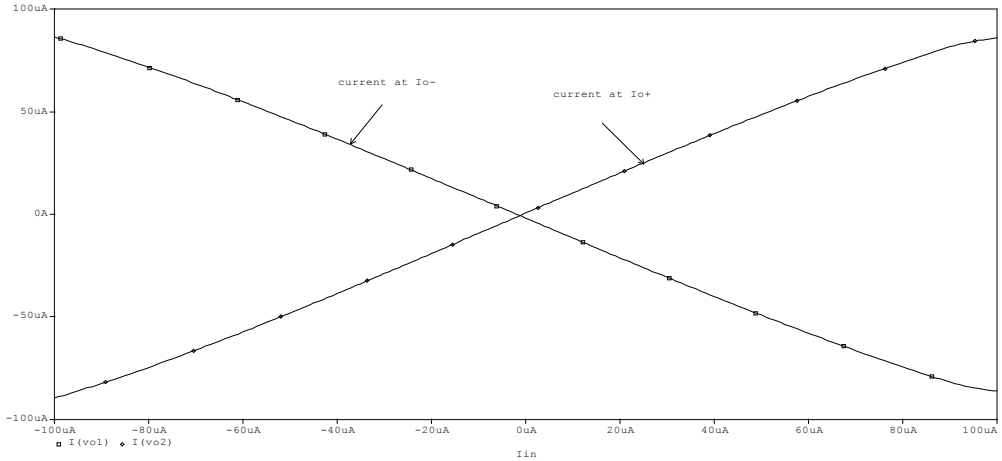


Fig. 6. DC transfer characteristic for current transfer from X port to O+ and O-

3. REALIZATION OF KHN FILTER USING MODIFIED DDCCTA

The KHN filter [22, 23] provides simultaneously the three basic filtering functions namely the high-pass (HP), band-pass (BP) and low-pass (LP) responses at three different outputs. The circuit uses three op-amps as shown in Fig. 7. The input voltage is applied to the non-inverting input terminal of the op-amp as shown in Fig. 7 (a) and this is defined as KHN of type A. It is also possible to apply the input voltage to the inverting terminal resulting in the inverted KHN filter shown in Fig. 7 (b) and this is defined as KHN of type-B [23].

There are four classes for each KHN type A or B, given in Tables 2 and 3 respectively [24]. Note that V_1 represents the High Pass response (HP), V_2 represents the Band Pass response (BP), V_3 represents the Low Pass response (LP) and V_4 represents the input voltage.

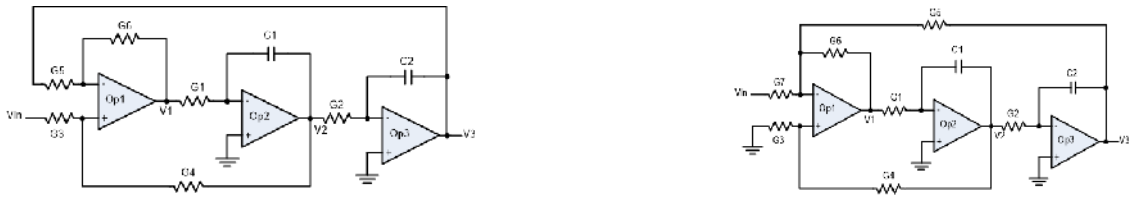
Table 2. Circuit equations of the three stages of the type A –KHN [24]

Class	Summer stage	Integrator 1	Integrator 2
I	$-G_6V_1+G_4V_2-G_5V_3+G_3V_4=0$	$G_1V_1+sC_1V_2=0$	$G_2V_2+sC_2V_3=0$
II	$-G_6V_1-G_4V_2-G_5V_3+G_3V_4=0$	$G_1V_1-sC_1V_2=0$	$G_2V_2-sC_2V_3=0$
III	$G_6V_1-G_4V_2-G_5V_3+G_3V_4=0$	$G_1V_1+sC_1V_2=0$	$G_2V_2-sC_2V_3=0$
IV	$G_6V_1+G_4V_2-G_5V_3+G_3V_4=0$	$G_1V_1-sC_1V_2=0$	$G_2V_2+sC_2V_3=0$

Table 3. Circuit equations of the three stages of the type B –KHN [24]

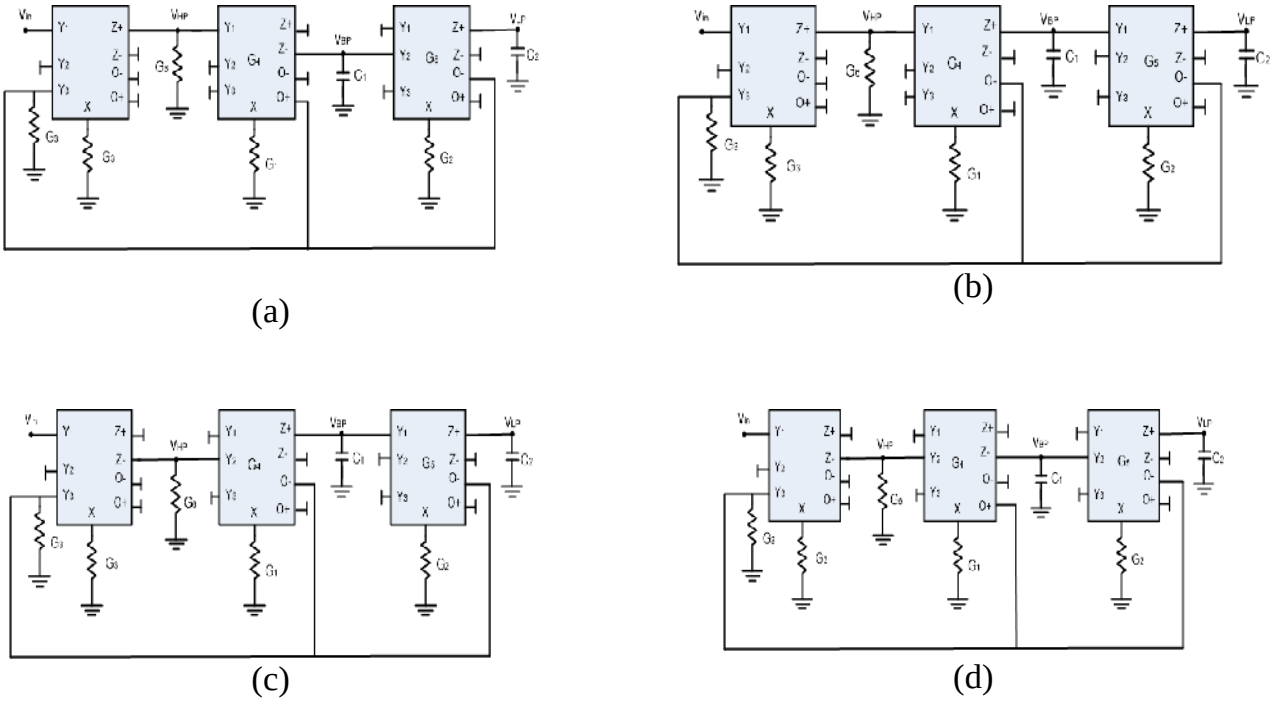
Class	Summer stage	Integrator 1	Integrator 2
I	$G_6V_1-G_4V_2+G_5V_3+G_3V_4=0$	$G_1V_1+sC_1V_2=0$	$G_2V_2+sC_2V_3=0$
II	$G_6V_1+G_4V_2+G_5V_3+G_3V_4=0$	$G_1V_1-sC_1V_2=0$	$G_2V_2-sC_2V_3=0$
III	$-G_6V_1+G_4V_2+G_5V_3+G_3V_4=0$	$G_1V_1+sC_1V_2=0$	$G_2V_2-sC_2V_3=0$
IV	$-G_6V_1-G_4V_2+G_5V_3+G_3V_4=0$	$G_1V_1-sC_1V_2=0$	$G_2V_2+sC_2V_3=0$

The realizations of KHN type A, using modified DDCCTA block is shown in Fig. 8. Note that one can get the possible realizations of KHN type B by inverting the input signal. i.e. the input signal is connected to the Y_2 terminal instead of Y_1 terminal. It may be of interest to show simulations of the generated KHN circuits. The KHN type A circuit is designed for Q= 5 and f_0=1MHz taking C1=C2=15 pF, R1=R2=15.9 kΩ, R5 =R6= 10 kΩ , R4 = 50 kΩ and R3=10 kΩ. The input signal is a sinusoidal input voltage source of 1 V magnitude. Fig. 9 represents the magnitude plot of the three output responses of the DDCCTA-KHN circuits of Figures 8(a) and (d) compared with the ideal response. Table 4 summarizes the simulation results for the DDCCTA –KHN type A equivalent circuits. It is obvious that the lowest errors belong to the configurations of Figures 8 (a) and (d). The highest error in the quality factor and ω_0 is found in the realization of Figures 8(b) and (c) which are rejected.



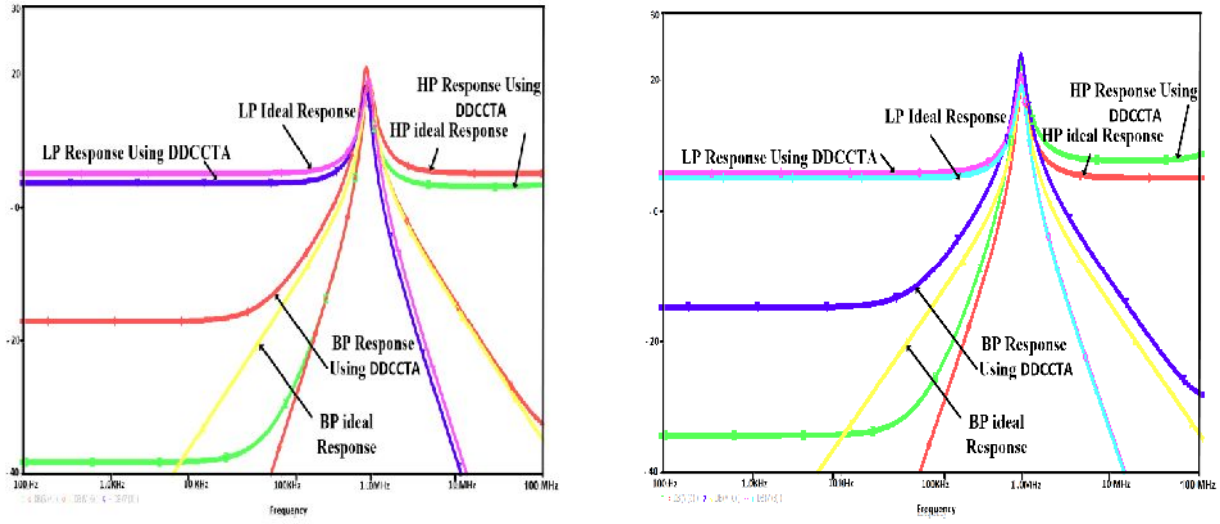
(a) (b)

Fig. 7. (a) Type A KHN circuit using three op amps [2]. (b) Type B inverted KHN circuit using three op amps [50].



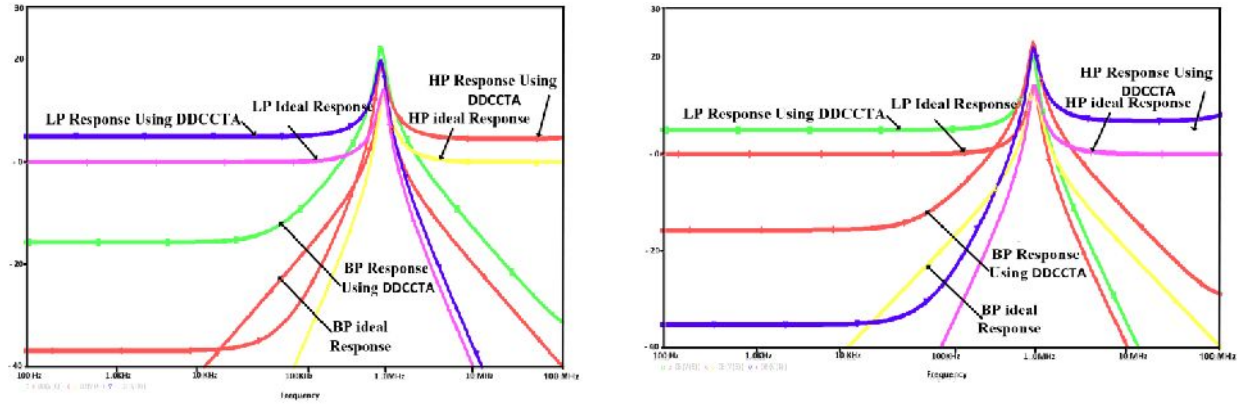
(a) (b) (c) (d)

Fig. 8. (a) DDCCTA-KHN realizations type A (a) Class I (b) Class II (c) Class III (d) Class IV



(a) (b)

Fig. 9. (a) Magnitude Response of Fig. 8 (a) compare to ideal response
(b) Magnitude Response of Fig. 8 (d) compare to ideal response



(a) (b)

Fig. 10. (a) Magnitude Response of KHN type B class I compared to ideal response
(b) Magnitude Response of KHN type B class IV compared to ideal response

Also, Fig. 10 represents the magnitude plot of the three output responses of the DDCCTA-KHN circuits of type B, classes I and IV compared with the ideal response. Table 5 summarizes the simulation results for the DDCCTA –KHN type B equivalent circuits. It is obvious that the lowest errors belong to the configurations of classes I and IV. And the realizations of classes II and III are rejected due to the large error in the simulations.

Table 4. Summarized results of simulations for equivalent circuits of KHN type A

The equivalent configuration	Bandwidth (kHz)	Center frequency (MHz)	Gain	Quality factor
Ideal response	200	1	10	5
Fig. 8 (a)	171.55231	1.00883	9.63574	5.88059
Fig. 8 (b)	395.86981	1.04388	3.97761	2.63693
Fig. 8 (c)	508.84431	1.29204	3.41318	2.53916
Fig. 8 (d)	173.59480	1.05286	9.95438	6.06505

Table 5. Summarized results of simulations for equivalent circuits of KHN type B

The equivalent configuration	Bandwidth (kHz)	Center frequency (MHz)	Gain	Quality factor
Ideal response	200	1	10	5
Fig. 8 (a)	171.55231	1.00883	9.63574	5.88059
Fig. 8 (b)	395.86981	1.04388	3.97761	2.63693
Fig. 8 (c)	508.84431	1.29204	3.41318	2.53916
Fig. 8 (d)	173.59480	1.05286	9.95438	6.06505

4. REALIZATION OF TT FILTER USING MODIFIED DDCCTA

The TT second order filter is shown in Fig. 11 [25, 26]. This filter is an active-RC topology used to realize both low-pass and band-pass bi-quadratic filtering. This topology has been widely used because it is simple, versatile, ad require few components. But it is well known that the classical TT circuit using op-amps has frequency limitations due to the finite gain-bandwidth of the op-amps.

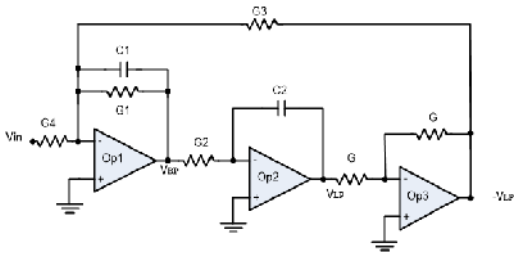


Fig. 11. Tow-Thomas (TT) second order filter using three Op Amps [25, 26]

Writing Kirchhoff's Current Law (KCL) at the inverting input nodes of the first two op amps result in:

$$G_4V_1 + (sC_1 + G_1)\,V_2 - G_3V_3 = 0 \qquad (3)$$

$$G_2V_2 + sC_2V_3 = 0 \qquad (4)$$

Where V_1 represents the input signal, V_2 represents the BP response and V_3 represents the LP response.

TT can be represented with four classes as in [19].Table 6 show the four class of TT. The realization of TT using DDCCTA block is shown in Fig. 12.

Table 6. Circuit equations of the three stages of the TT [19]

Class	Summer stage	Integrator 1
A	$G_4V_1 + (sC_1 + G_1)V_2 - G_3V_3 = 0$	$G_2V_2 + sC_2V_3 = 0$
B	$-G_4V_1 + (sC_1 + G_1)V_2 - G_3V_3 = 0$	$G_2V_2 + sC_2V_3 = 0$
C	$G_4V_1 + (sC_1 + G_1)V_2 + G_3V_3 = 0$	$-G_2V_2 + sC_2V_3 = 0$
D	$-G_4V_1 + (sC_1 + G_1)V_2 + G_3V_3 = 0$	$-G_2V_2 + sC_2V_3 = 0$

It may be of interest to show simulations of the generated DDCCTA- TT circuits. The TT circuit is designed for Q= 5 and f 0=1MHz taking C1=C2=15pF, R=R3=R2=15.9 kΩ,

R1/R=5 and r=10 kΩ .The input signal is a sinusoidal input voltage source of 1V magnitude. Fig. 13 represents the magnitude responses of the TT equivalent circuit of Fig. 12(a) and compared with ideal.

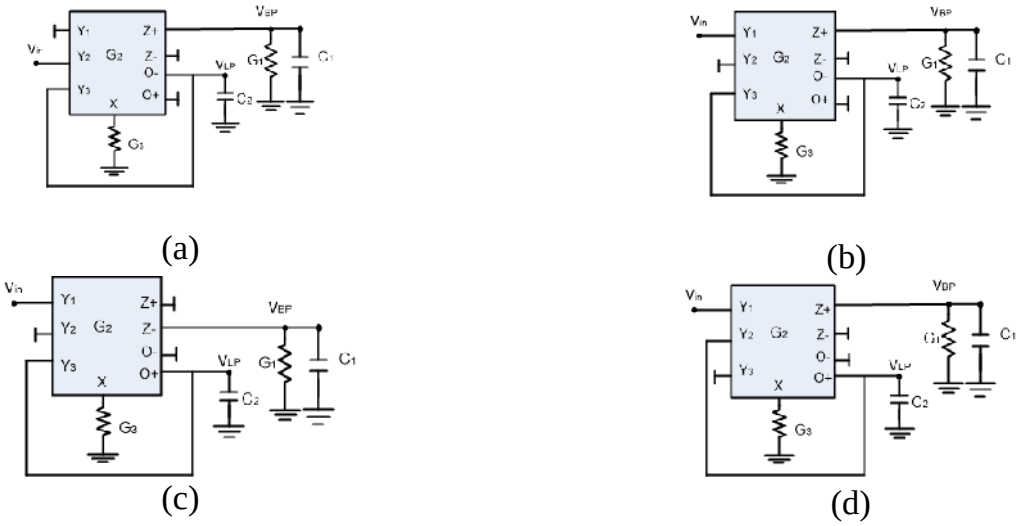


Fig. 12. DDCCTA-TT Realizations(a) Class A (b) Class B (c) Class C (d) Class D

Table 7. Summarized results of simulations for equivalent circuits of TT

The equivalent configuration	Bandwidth (kHz)	Center frequency (MHz)	Quality factor
Ideal response	200	1	5
Fig. 12 (a)	234.60282	1.09813	4.68080
Fig. 12 (b)	234.60151	1.09813	4.68083
Fig. 12 (c)		rejected	
Fig. 12 (d)	231.59666	1.11225	4.80253

Table 7 summarizes the simulation results of all the generated DDCCTA-TT circuits. We can find that the lowest ΔQ belongs to the configuration of Fig. 12 (d) and the lowest $\Delta\omega_0$ belongs to the configurations of Figures 12 (a) and (b). The configuration of Fig. 12(c) is rejected due to its bad simulation responses.

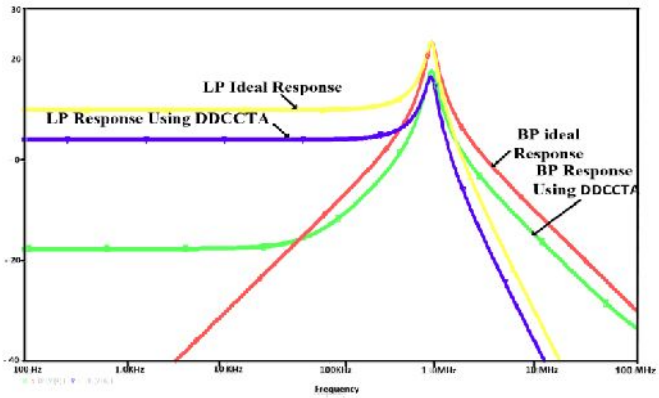


Fig.13 Response of TT configuration of Fig.12 (a) and ideal resonse

5. CONCLUSIONS

The paper first modifies the DDCCTA block and then uses it to generate a family of KHN-DDCCTA equivalent circuits and TT-DDCCTA equivalent circuits. The DDCCTA-KHN was realized with three DDCCTA blocks and five resistances. Also, the DDCCTA-TT was realized with only one DDCCTA block and two resistances. All the generated circuits have grounded passive elements. The generated circuits have been confirmed using PSPICE simulation and the simulation results showed that some generated circuits have very good performance compared to the ideal responses.

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