



A Brief introduction to Memristor Device

Eman Omar ^a, Hesham H. Aly ^{b*}, Mostafa Fedawy ^c

^a Department of electronics and communications engineering, Faculty of Engineering, International Academy for Engineering and Media Science (IAEMS)

^b Department of electronics and communications engineering, Faculty of Engineering, Arab Academy for Science and Technology and Maritime Transport (AASTMT),

^c Department of electronics and communications engineering, Faculty of Engineering, Arab Academy for Science and Technology and Maritime Transport (AASTMT),

*Corresponding author: Email address: eomar2443@gmail.com

Received: 01-11-2022

Accepted: 19-11-2022

Published: 07-06-2023

ABSTRACT

In this paper, a brief introduction to memristor device will be presented. Since 1971, memristor device invented by Leo Chua which included in the fundamental electrical elements besides resistors, capacitors and inductors. Memristor is considered as the missing elements that correlate between the flux and the charges of the electrons. Memristor was not realized as a physical component until recently. HP and Knowm are the available physical memristor device in the market with different structure. However, HP memristor is considered to be the most structure have been studied from the researchers. Now a days considered is the core element in AI accelerators which depends on memory processor structure. This paper will discuss the history of memristor and its structure based on HP and Knowm approach with mathematical models. Some fabrication techniques will be discussed and the applications.

Keywords: memristor, HP, Knowm, memristor fabrication, memristor applications, memristor modelling.

1 INTRODUCTION

By entering the era of artificial intelligence (AI), the traditional architecture of processors may not be suitable for the huge data processing or implementing AI algorithms. The main idea of the AI processors or what is called now “Accelerator” is based on memory processing. This leads to focus the current research on developing the memory design and the time of fetching and executing the data. One of the huge step taken to develop the AI accelerator is the use of what is called a memristor device.

Memristor has been invented by Leon Chua in 1971 as the fourth fundamental passive electronics element with a nonlinear voltage-current behavior [1]. Since then, it was a theoretical element that needed to be proven with some physical device. In 2008, HP lab presented a new resistive switch device, it was TiO₂-based resistive switching device and was called a first physical memristor. Memristor was then deployed and researched worldwide. The HP memristor with bipolar switching were oxygen-ion conducting cells with valence change memory (VCM) effect. Then, in 2018 Knowm Inc. implemented a new memristor known as W dopant type similar to HP memristor and is based on the redox phenomena. However, Knowm devices based on electromechanical metallization memory (ECM) effect [2].

The device presented by Chua (Memristor) represented the connection between the magnetic flux and the charge which is considered to be the fourth fundamental circuit element where the other three basic elements are resistor, inductor, and capacitor. These three elements defined connections between basic circuit parameters such as current (i), charge (q), voltage (v), and magnetic flux (φ). The connection between the charge and the magnetic flux was missing until the memristor was invented. Figure 1 shows the four basic circuit elements and parameters. [3][4]

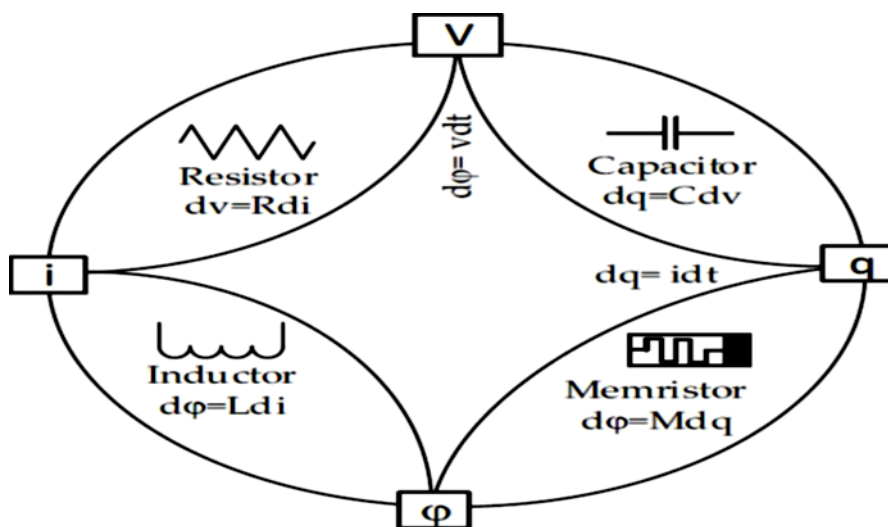


Figure 1. Connection between four basic circuit elements and basic parameters [3]

Chua defined the memristor as: “any 2-terminals device, exhibiting a pinched hysteresis loop which always passes through the origin in the voltage-current plane when driven by any periodic input

current source, or voltage source, with zero DC component. If the input is a current source, it is called a current-controlled memristor. If it is a voltage source, it is called a voltage-controlled memristor”[5].

Figure 2 shows the theoretical pinched I-V characteristic curve that defines the memristor [6].

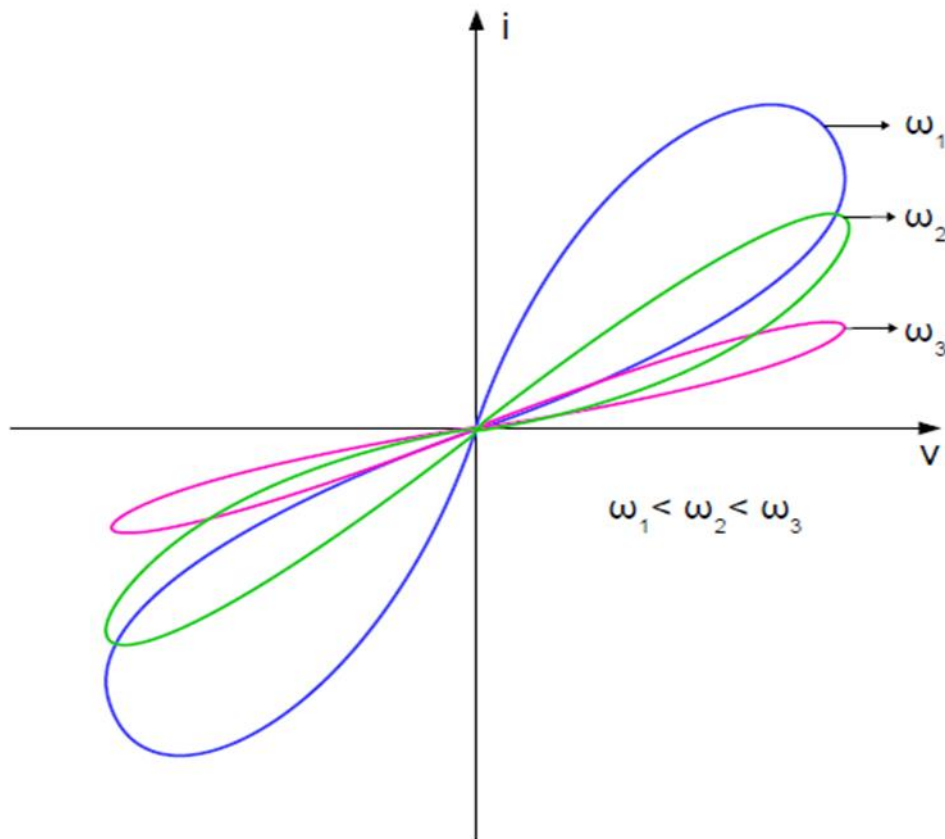


Figure 2. I-V curve characteristics of memristor and frequency effect on the hysteresis loop [6]

The term pinched means that $V(t) = 0$ whenever $i(t) = 0$ and vice versa. In other words, for any given value of current $i(t)$, there will be two corresponding values of voltage $V(t)$ except at $i(t) = 0$. The converse is also true, for any given value of voltage $V(t)$, there will be two corresponding values of current $i(t)$ except at $V(t) = 0$.

Memristor device has simple construction that makes it promising device to research and easy modelling. Memristor device contains three layers i.e., bottom electrode, middle layer, and top electrode. Figure 3 shows memristor cross sectional area of memristor [7].

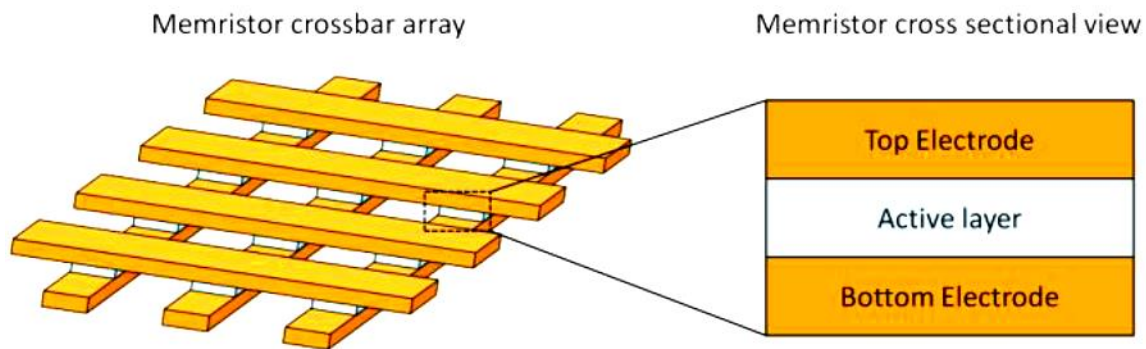


Figure 3. Memristor construction layers (cross sectional view)[7]

Top and bottom electrodes of memristor can be of different metals and conductive polymers, whereas the middle (Active) layer can be a metal oxide, insulator, dielectric or polymer. Figure 2[5] shows different memristor technologies.

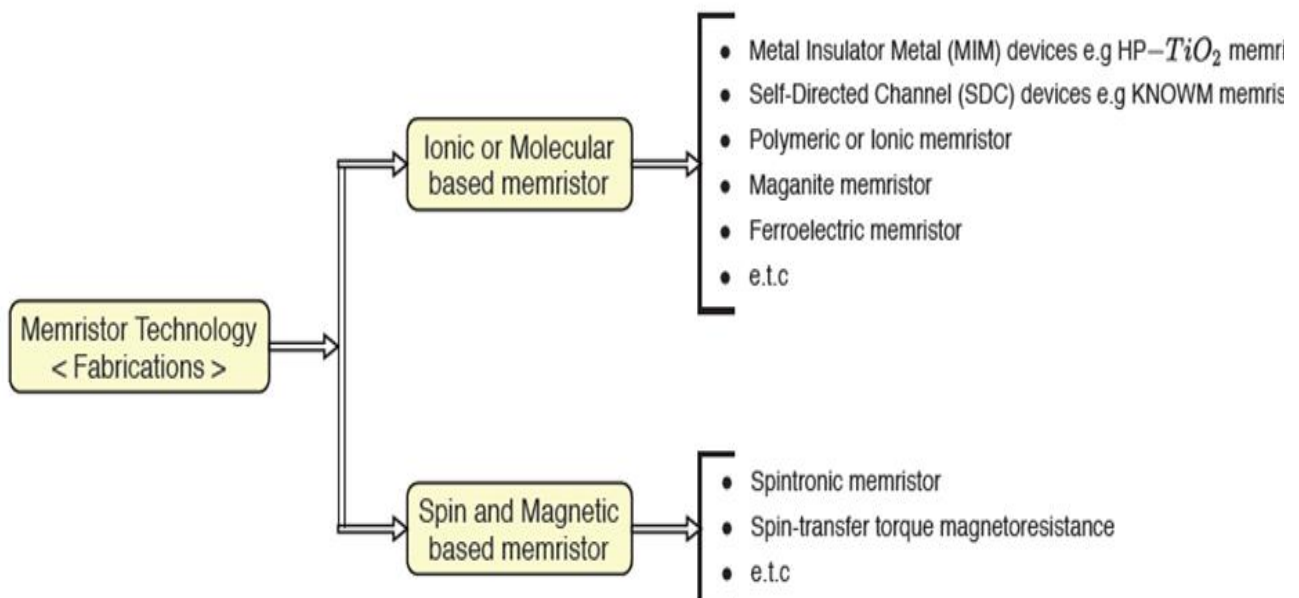


Figure 4. Some memristor fabrications technologies[5]

In this paper we will talk about the most common types (HP and KNOWM) and their mathematical model and other mathematical models presented of the memristor. Adequate mathematical model of the memristor is needed to be implemented in software applications to simulate the performance of actual memristors. There have been many models of the memristor presented starting of HP model. Then, linear drift and nonlinear drift models based on HP model have been presented. The window function used in nonlinear drift model have been showed. Unlike HP model, the Simmons tunnel barrier and the threshold adaptive memristor model (TEAM) have been also mentioned. Based on TEAM model, Knowm memristor model has been presented.

Memristor has many advantages that make it promising device to be used in future electronics like:

- 1- Using the ability of remembering input in many innovative circuits and memory devices.
- 2- Saving chip area by using memristor designed in the metal layer.
- 3- Ability of combining logic operation with memory cells on the same chip and in different places through the chip.

Due to these advantages, many fabrication technologies have been developed to fabricate the memristor. This paper will focus on inkjet technology due to its flexibility, simplicity and cost effective.

This paper is organized as follows: section 2 discusses briefly memristors in market. Section 3 presents different memristor models. Section 4 shows the inkjet fabrication technology. Applications of memristor have presented in section 5. The conclusion is presented in section 6. Finally, Future work in section 7.

2 Memristors in Market

In this section memristor devices found in market will be presented. To the knowledge of the authors, two companies claimed to design and fabricate memristor device namely: HP and Knowm with different structure as following.

2.1 HP Memristor

The researcher team at HP labs presented for the first time an actual physical memristor in 2008. The memristor consisted of a nanometer scale titanium dioxide (TiO_2) thin film, having doped and undoped regions which are middled between two platinum contacts to form metal-insulator-metal (MIM) structure as shown in Figure 5.[8]

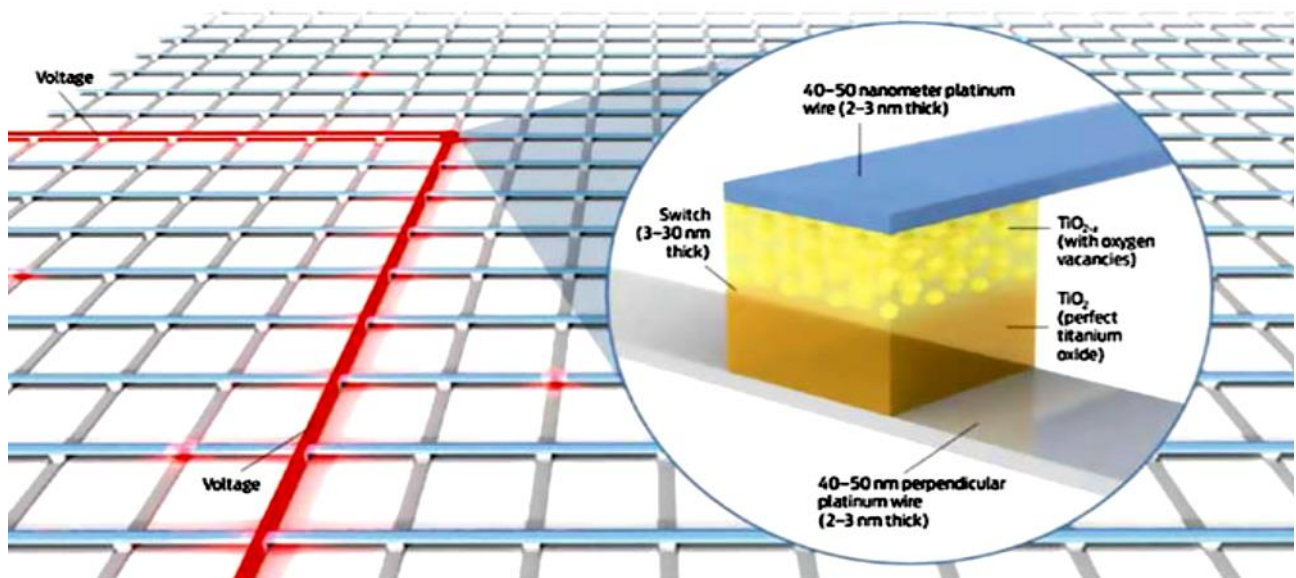


Figure 2. HP memristor working principle[8]

Figure 6 shows the memristor model (based on oxygen vacancies) presented by HP Lab that consists of Pt/TiO₂/Pt structure [3]. The TiO₂ layer that has one side doped with positive charged-rich oxygen vacancies (TiO_{2-x}) and the other side is undoped put between two platinum layers.

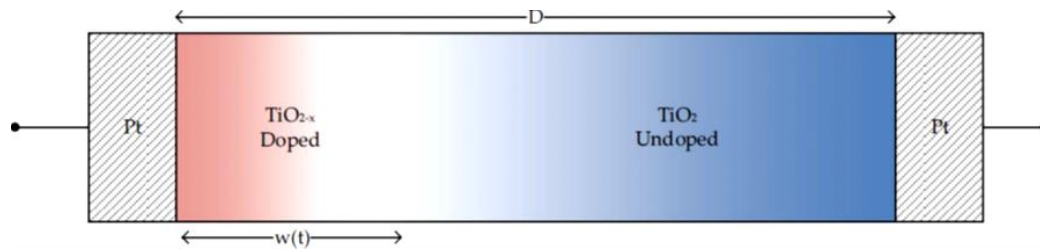


Figure 3. HP memristor Structure [3]

Figure 6 shows the doped (left red region) and undoped (right blue region) regions of the memristor. The width of doped region ($w(t)$) changes depending on the ionic drift between two regions which depends on applied voltage. When the width approaches 0, the memristor goes to a high resistance state (HRS). When the width approaches D , the memristor goes to a low resistance state (LRS). Figure 7 shows the HRS and LRS of memristor according to the width $w(t)$.

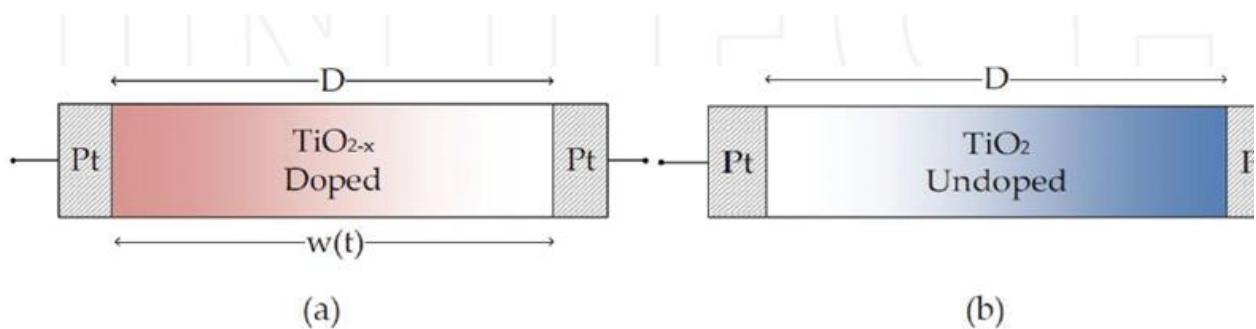


Figure 4. Memristor HRS and LRS states representation. (a) LRS and (b) HRS. [2]

According to this model, HP memristors with bipolar switching can be considered as oxygen-ion conducting cells with valence change memory (VCM) effect. And by applying voltage on the memristor, the actual I-V curve of the HP memristor can be shown in Figure 8.[1]

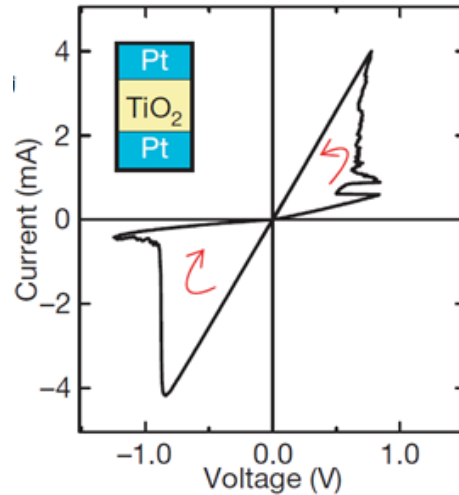


Figure 5. Experimental I-V curves of HP memristor[1]

2.2 Known Memristor

Known and HP memristors have the same operation principle and both based on the redox phenomena[2]. However, Known memristors used the electrochemical metallization memory (ECM) effect and therefore belong to a different branch of memristive cell taxonomy, forming a separate class of self-directed channel (SDC) memristors (as shown before in Figure 4).

Known Inc. produces four versions of memristor: W, C, Sn, and Cr, depending on the contained dopant into the active layer during fabrication. Figure 8 presents the W dopant memristor structure that will be discussed in this paper. This memristor has two states SET and RESET. Setting the memristor on is by applying positive voltage which causes Ag cations to increase and move to the electrodes. Resetting is the opposite when applying negative voltage.

Figure 10 shows actual I-V curve of the Known memristor with W dopant under a sinusoidal control voltage at a frequency of 10 Hz with an amplitude of 0.7 V.[2]

As shown in Figure 10, the I-V curve consists of 4 sections:

At section 1, the memristor is in High Resistive State (HRS) and by increasing positive voltage gradually, the memristor resistance decreases (going from HRS to LRS as shown by the arrow direction) until the voltage reaches threshold value (V_{ON}) at which it converts to Low Resistive State (LRS) i.e. (in SET state) as shown in section 2.

At section 2, it is noticed that there is voltage snapback in the I-V curve in switching processes which can be explained by a discrete change in the quantum states of the system with a change in the ion concentration in the active layer of the device, then there is a progressive voltage at which the SET state is occurred.

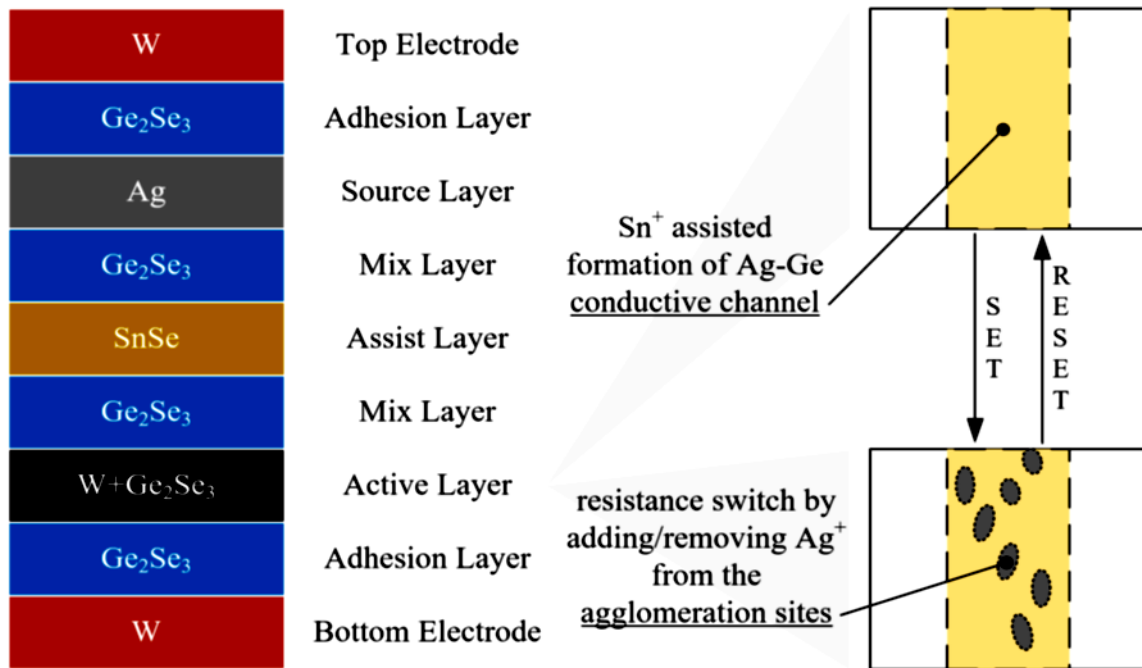


Figure 6. Known Memristor structure[2]

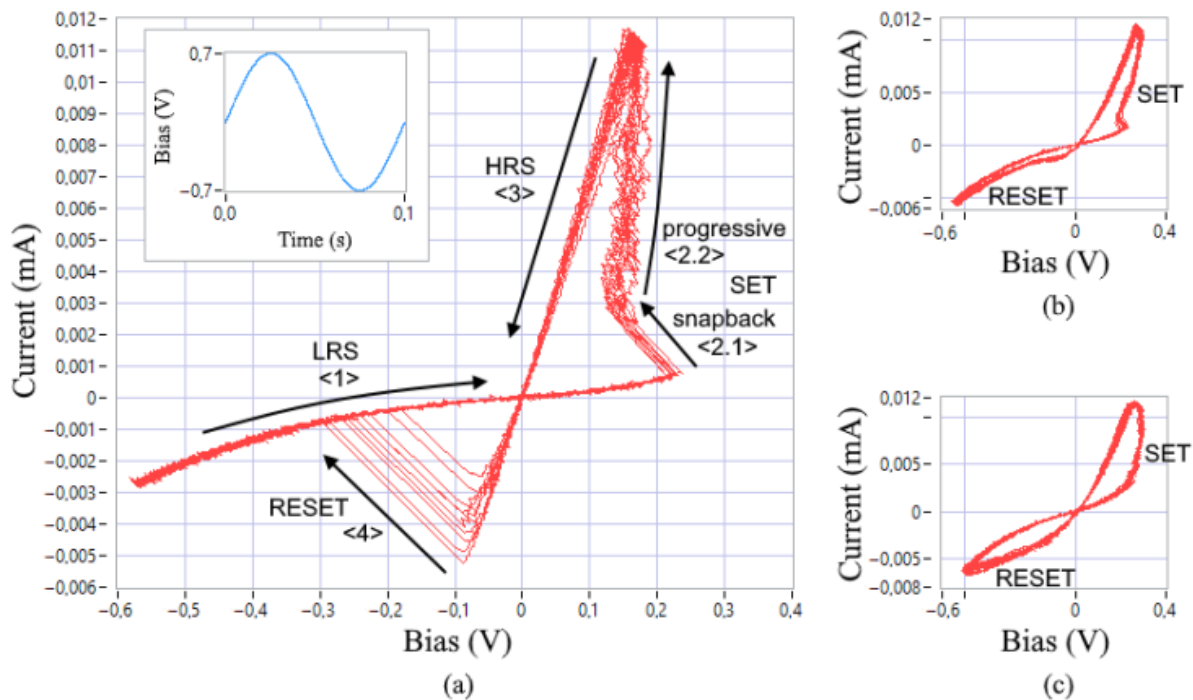


Figure 7. Experimental I-V curves of Known memristor [2]

At section 3, when decreasing applied voltage, the memristor resistance increases (going from LRS to HRS as shown by the arrow direction).By applying negative voltage on memristor, the resistance continues increasing until the voltage reaches threshold value (V_{OFF}) at which it converts to High Resistive state (HRS) i.e.(in RESET state) as shown in section 4.[2]

After talking about physical memristors in market and their structure, the next section will talk about modelling of these memristors.

3 Mathematical Modelling

In this section, models of physical memristors like HP and Knowm are presented. To characterize the memristors model from other non-memristor switching devices, it is done by their current–voltage response (I–V characteristics) indifferent circuits. These characteristics called fingerprints of memristors.

The first fingerprints was published by LEON CHUA determined three main fingerprints:[9], [10]

1. The I–V response of a memristor (with positive memristance) is always a pinched hysteresis loop when subjected to a bipolar periodic input signal without offset.
2. The hysteresis loop area decreases monotonically when the excitation frequency increases.
3. For a fixed-input amplitude, the pinched hysteresis loop shrinks to a single-valued function as the frequency of the input supply tends to infinity.

Another 9 fingerprints including CHUA’s fingerprints was published by a research team at BUT/University of Defense Brno, Czech Republic and made a more clarification of memristors[10].

Later in 2022, a research team at KNOWM Inc. suggested identification method. This method is presented as a general conditions for a wide range of memristive elements. KNOWM research team suggested seven criteria's (fingerprints) for assessing the mathematical modeling[2]

Correspondence of the model’s I-V curve and the switching dynamics in the time domain to the experimental data of real devices.

1. Nonlinearity of the switching function.
2. Suitability for modeling the complementary serial connection of two elements.
3. Ability to set several states of resistance.
4. Dependence of SET (or RESET) switching from the current state of the resistance.
5. Reliable simulation of the memory fading effect.
6. Compact representation of a continuous mathematical model

Identification process of the model to be verified goes through a procedure. The procedure for Identification includes many candidate models and the most suitable one is chosen. Then, comparison between the experimental results of actual element and the proposed model is applied through stages (from stage 1.1 to 1.5 as shown in Figure 11) to choose the adequate model or make modifications to the chosen model to approximate the actual experimental results. [2]

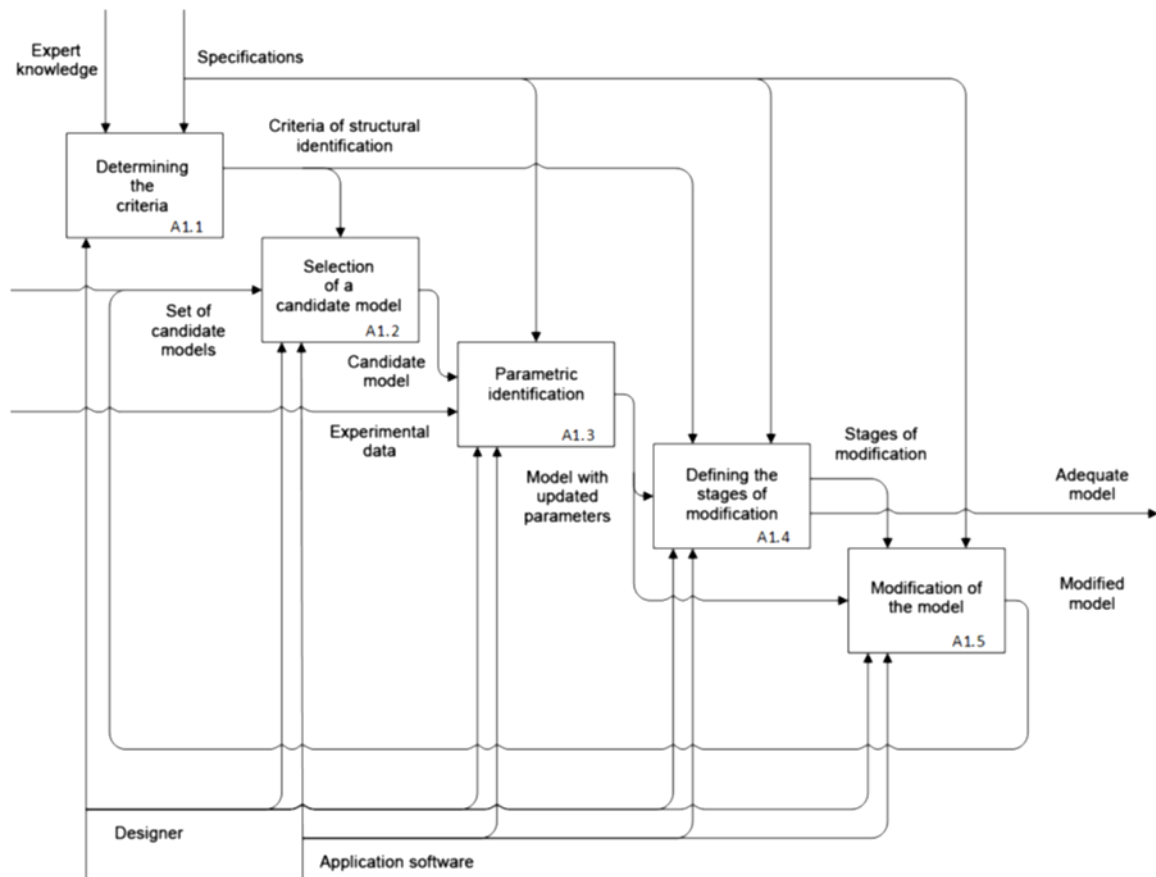


Figure 8. process of memristive element identification[2]

3.1 HP memristor model

HP model is the first one of the memristor. Current controlled HP memristor model is in the following form [1], [11], [12]

$$\left\{ \begin{array}{l} v = R(x)i, \\ R(x) = R_{on}x + R_{off}(1 - x), \\ x' = \frac{\mu_v R_{on}}{D^2} i, \end{array} \right\} \quad (1)$$

where i is the input current, v is the output voltage, R_{ON} and R_{OFF} are the allowable low and high resistances of the memristor ($R_{ON} \ll R_{OFF}$), respectively, $x \in [0, 1]$ is the internal state variable, μ_v is average ion mobility for linear ionic drift memristor, D is thickness for semi-conductor film.

3.1.1 Linear Ion Drift Model:

A uniform electric field across the device is assumed according to HP memristor; thus there is a linear relationship between net electric field and the drift diffusion velocity. [3][13]

The relation between the current and the voltage of the memristor in linear model is defined by the following equations:[14]

$$V(t) = [R_{on}x(t) + R_{off}(1 - x(t))]i(t) \quad (2)$$

$$X(t) = \frac{w(t)}{D} \in (0,1) \quad (3)$$

$$\frac{dx(t)}{dt} = \mu_v \frac{R_{on}}{D^2} i(t) \quad (4)$$

Where R_{on} and R_{off} are the values of the resistance for $w(t) = D$ and $w(t) = 0$, respectively, μ_v is the average drift mobility of the charges

From Eq. (2), the value of memristance can be expressed by

$$M(q(t)) = \frac{V(t)}{i(t)} = R_{on}x(t) + R_{off}(1 - x(t)) \quad (5)$$

By using math equations, the final memristance expression could be presented as follows:

$$M(q(t)) = R_{on}\mu_v \frac{R_{on}}{D^2} q(t) + R_{off} \left(1 - \mu_v \frac{R_{on}}{D^2} q(t) \right) \quad (6)$$

This expression can be written as

$$M(q(t)) = R_{off} \left(1 - \mu_v \frac{R_{on}}{D^2} q(t) \right) \quad (7)$$

if the left side of the total expression is neglected because $R_{on} \ll R_{off}$.

3.1.2 Nonlinear Ion Drift Model

There are assumptions in linear drift and HP models that have been greatly simplified, neglecting some basic laws like:[3]

- Supposing that the state variable (x) of the memristor is proportional to the charge flowing through the memristor
- Assuming that the vacancies have the freedom to move along all length of the memristor.

But the actual studies show that the drift of vacancies is nonlinear in the region near the boundary interfaces. The reason is that even a small excitation signal can create a large electric field causing nonlinear drift of the vacancies near the boundary interfaces in the memristor.

- The state variable (x) never reaches zero, indicating that oxygen vacancies are not present in the memristor.
- Similarly, the doped region cannot cover the entire length of the memristor, because there will be no undoped part and the memristor will not work in this way.

In order to provide nonlinearity for the boundary problems mentioned above, functions called **window function** are introduced. This function is implemented by:

$$\frac{dx(t)}{dt} = \mu_V \frac{R_{on}}{D^2} i(t) f(x(t)) \quad (8)$$

The function $f(x)$ should have zero at the limits of the memristor ($x = 0$ and $x = 1$) and maximum value at the middle of the memristor ($x = 0.5$). An effective window function should satisfy the following conditions for modeling of nonlinearity:[3]

- The function should take account of the boundary situation at the top and bottom electrodes of the memristor.
- The function should provide nonlinear drift across the entire active area of the memristor.
- The function should ensure linkage between the linear and nonlinear drift models.
- The function should be scalable in the interval of $f_{max}(x)$ can be obtained such that $0 \leq f_{max}(x) \leq 1$.
- The function should include the control parameter to set the model.

3.1.2.1 Joglekar's window function Model

Joglekar's window function can be given as[3][13]

$$F(x) = 1 - (2x - 1)^{2p} \quad (9)$$

Where p is the control parameter which changes the flatness of the $f(x)$ curve around its maximum value at $x = 0.5$ and is a positive integer as shown in Figure 12.

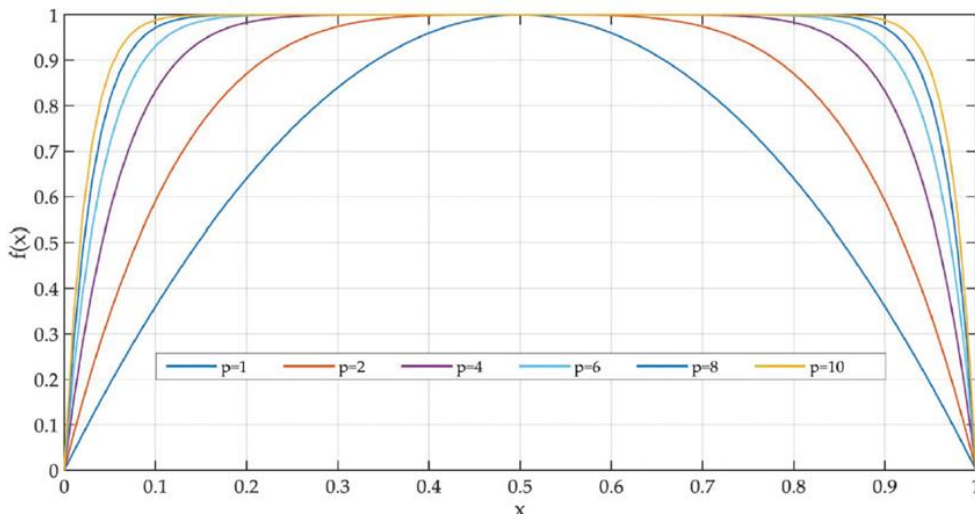


Figure 9. Joglekar's window function for different p values.[3]

The disadvantage of Joglekar's window function is the cling situation of the state variable at the boundaries, and it is difficult to change the window function due to the zero value at both boundaries. That is, the nonlinear drift problem is solved, but the boundary lock is not taken into account.

3.1.2.2 Biolek's window function

Biolek has solved Joglekar's window function errors by introducing a new window function contains step function and expressed as follows:[3][13]

$$f(x) = 1 - (x - \text{stp}(-i))^{2p} \quad (10)$$

$$\text{stp}(i) = \begin{cases} 1, & i \geq 0 \\ 0, & i < 0 \end{cases} \quad (11)$$

Where p is positive integer and i is the memristor current as shown in Figure 13

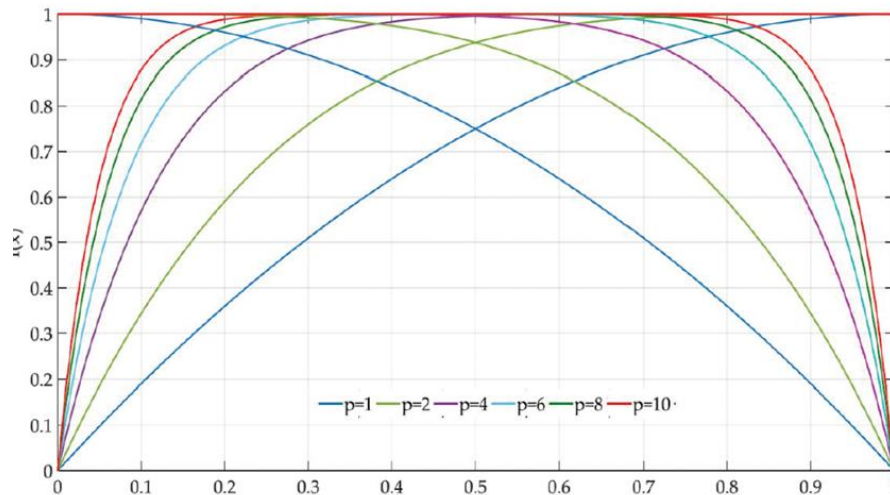


Figure 10. Biolek's window function for different p values[3]

Biolek's window function depends not only on the state variable but also on the current flow through the memristor. This resolved boundary lock problem. But there is another problem of this window function that does not include the scalability factor, so the maximum value of the window function cannot be set to a lower or greater value.

3.1.2.3 Prodromakis's window function

Prodromakis's window function is

$$f(x) = j(1 - [(x - .5)^2 + .75]^p) \quad (12)$$

Where p and j are a positive real number as shown in Figure 14&15

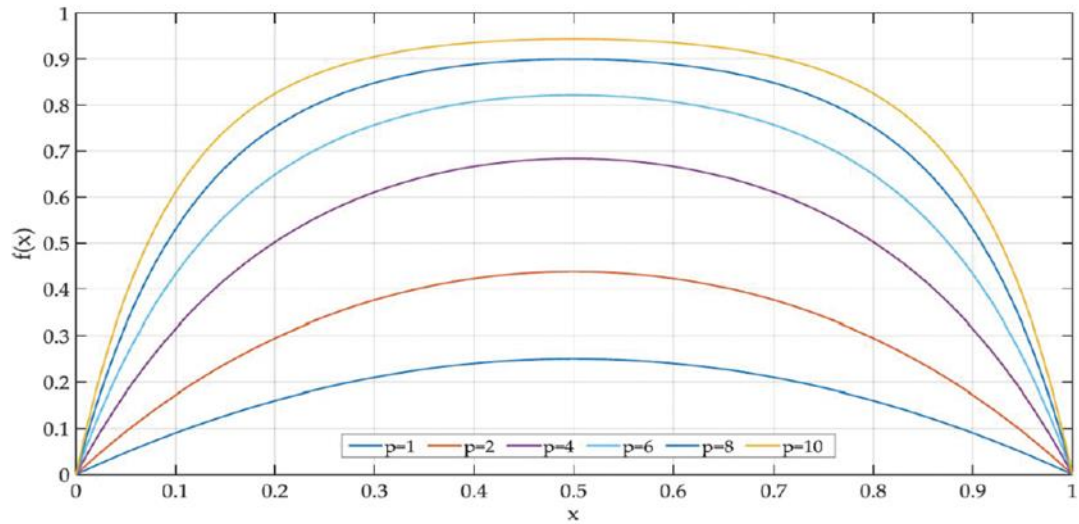


Figure 11. Prodrumakis' window function for $j = 1$ and different p values[3]

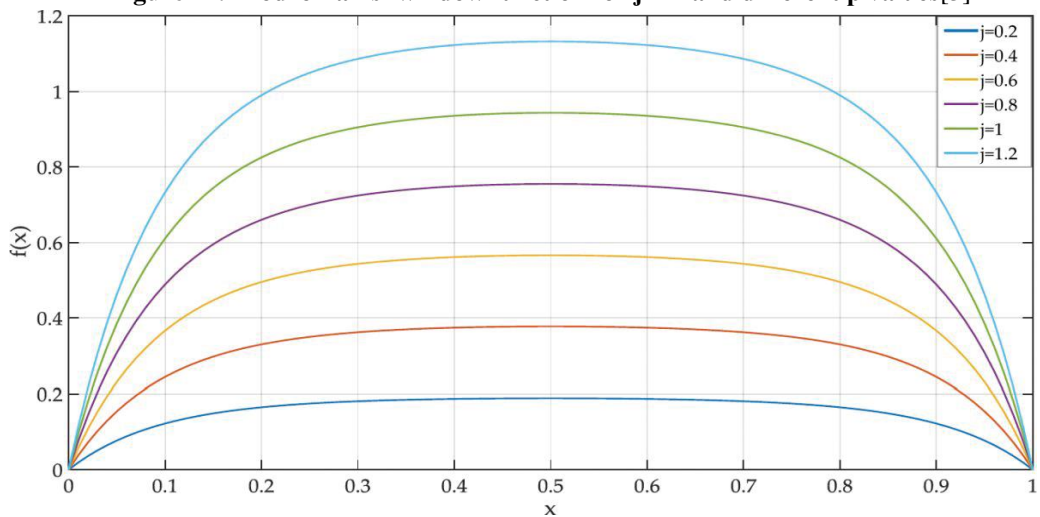


Figure 15. Prodrumakis' window function for $p = 10$ and different j values[3]

Prodrumakis proposes a solution for the scalability problem by providing a connection to the linear dopant drift model for sufficiently large values of p . However, the model built by Prodrumakis still contains the problem of boundary lock.

3.1.2.4 Zha's window function

Zha introduced a new window model so that boundary lock, scalability, and nonlinear effects can be met at the same time.

Zha's window function is expressed as follows:[3]

$$F(x) = j(1 - [.25(x - \text{stp}(-i))^2 + .75]^p) \quad (13)$$

where $\text{stp}(i)$ is given Eq. (11), p and j are positive real numbers as shown in Figures 16&17

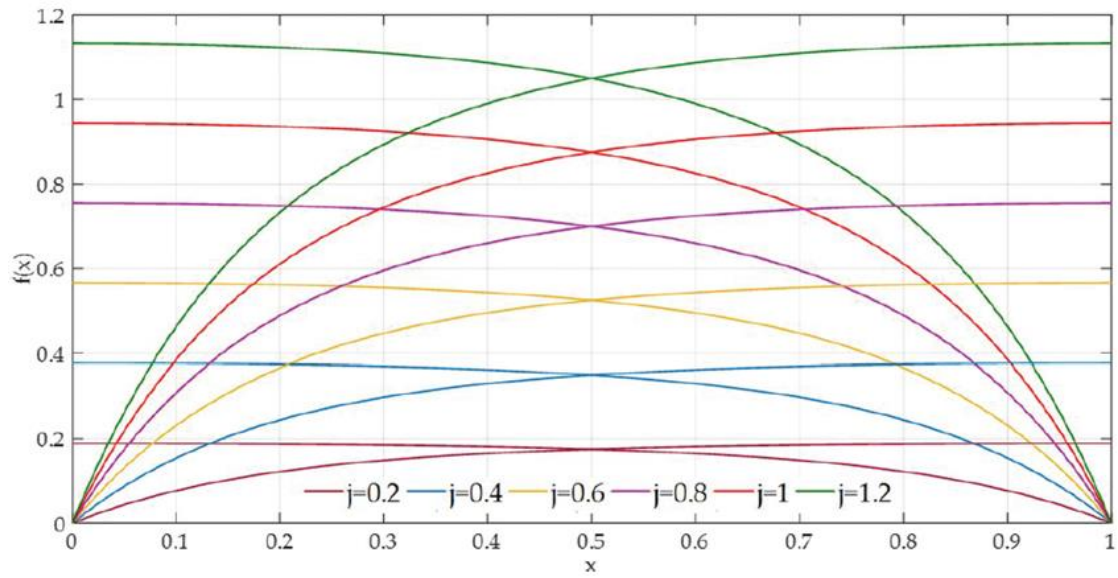


Figure 126. Zha's window function for $p = 10$ and different j values[3]

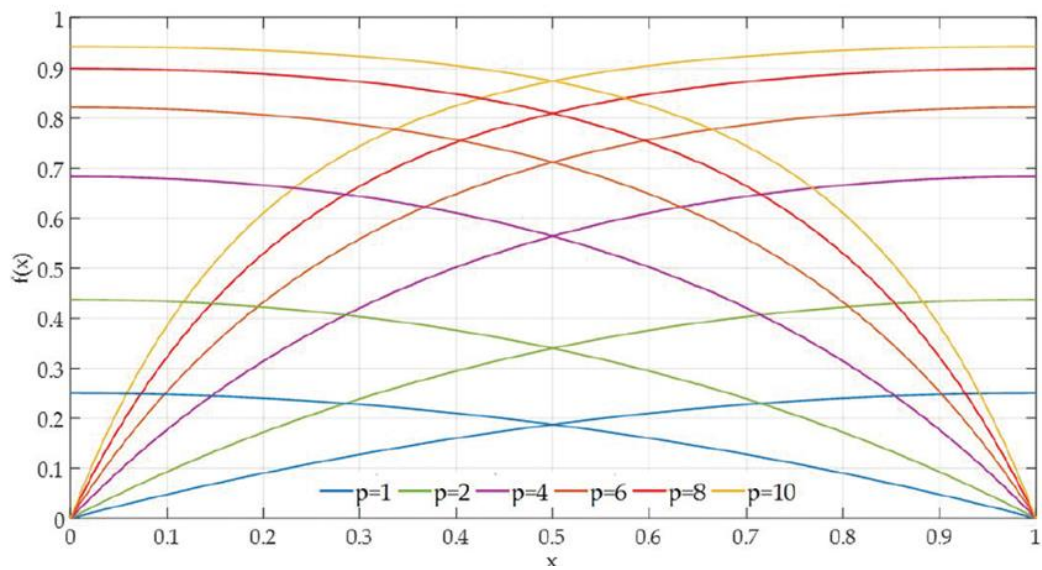


Figure 137. Zha's window function for $j = 1$ and different p values[3]

3.1.2.5 Comparison of window functions

Figure 18 shows all window functions of the nonlinear drift model mentioned above

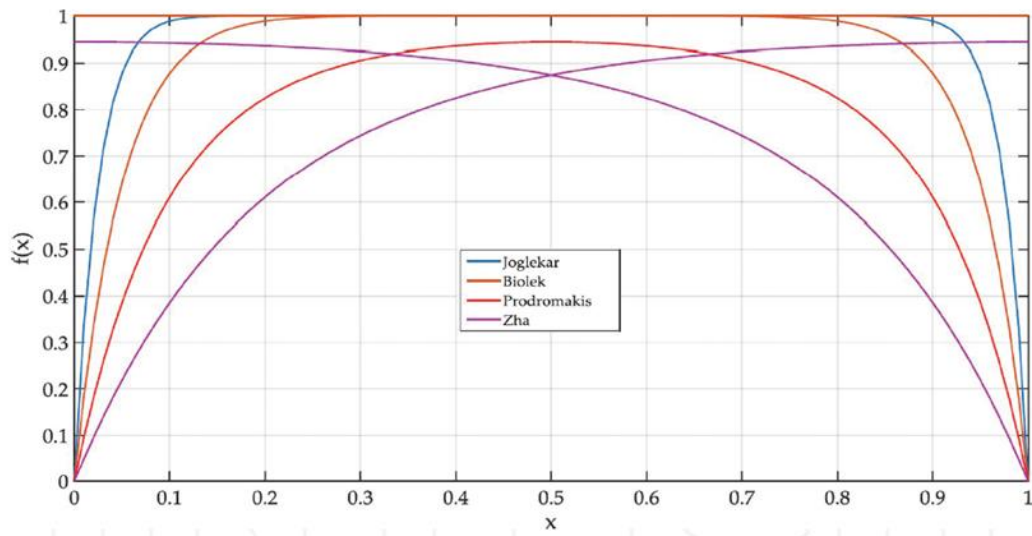


Figure 18. Different window functions for $p = 10$ and $j = 1$ [3]

Figure 19 shows I-V characteristics of the window functions have been plotted

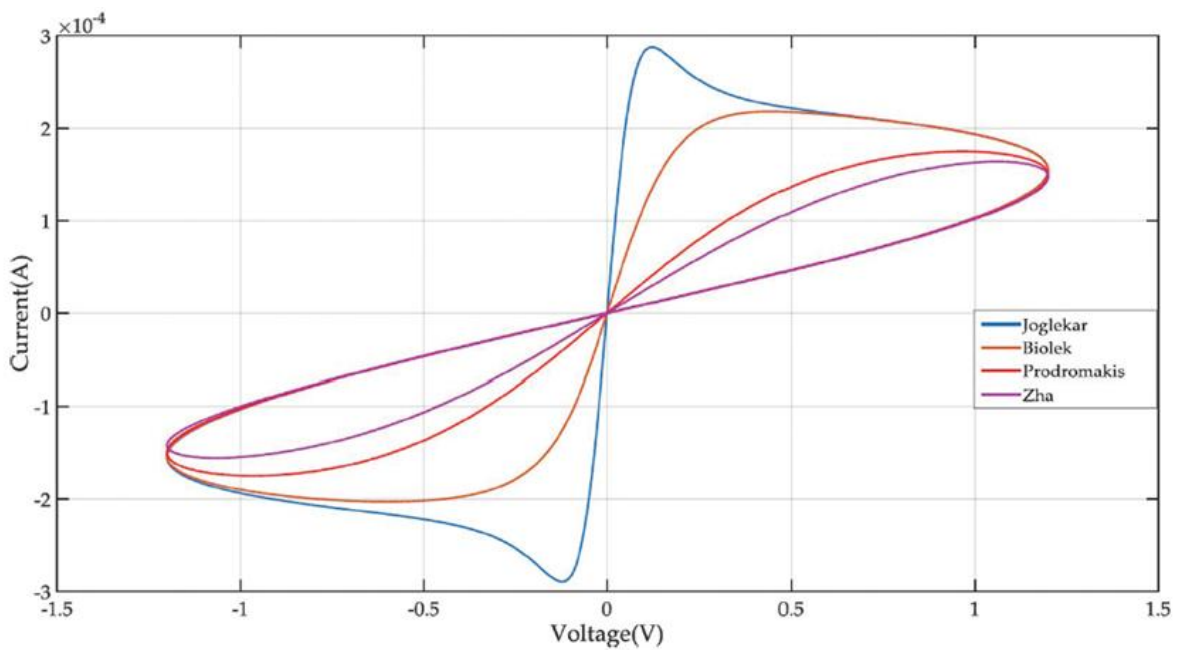


Figure 149. Change of I-V pinched hysteresis loops of the memristor for different window functions[3]

3.2 Simmons tunnel barrier model

Simmons presented a physical memristor model different from memristors based on the HP model. Simmons model consisting of a resistor and an electron tunnel barrier in series but HP models consisted of two regions each of which was modeled as a resistance.

Figure 20 shows Simmons tunnel barrier memristor the structure model, where w is the tunneling barrier and R_s is the channel resistance.[3]

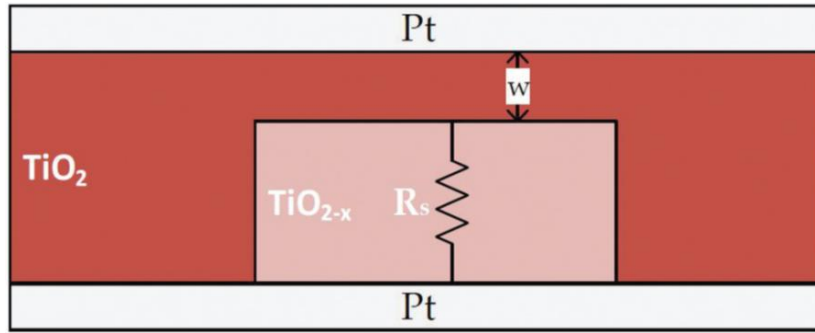


Figure 20 Simmons tunnel barrier model memristor structure.[3]

w is the state variable of the model and can be written as:

$$\frac{dw(t)}{dt} = \begin{cases} f_{off} \sinh\left(\frac{i}{i_{off}}\right) \exp\left[-\exp\left(\frac{w - a_{off}}{w_c} - \frac{|i|}{b}\right) - \frac{w}{w_c}\right], & i > 0 \\ f_{on} \sinh\left(\frac{i}{i_{on}}\right) \exp\left[-\exp\left(\frac{w - a_{on}}{w_c} - \frac{|i|}{b}\right) - \frac{w}{w_c}\right], & i < 0 \end{cases} \quad (14)$$

Where f_{off} , f_{on} , a_{off} , a_{on} , i_{off} , i_{on} , and b are fitting parameters

3.3 Threshold Adaptive Memristor (TEAM) model

TEAM model is a memristor model with several assumptions for analysis simplification and computational efficiency. These assumptions are as follows:

1. There is no change in the status variable for values below a certain threshold value.
2. A polynomial relationship is established between the current of memristor and the internal state drift derivative instead of the exponential dependence.

Taking these assumptions into account, the derivation of the state variable is written as[3]

$$\frac{dw(t)}{dt} = \begin{cases} K_{off} \left(\frac{i(t)}{i_{off}} - 1\right)^{\alpha_{off}} f_{off}(w) & , 0 < i_{off} < i \\ 0 & , i_{on} < i < i_{off} \\ K_{on} \left(\frac{i(t)}{i_{on}} - 1\right)^{\alpha_{on}} f_{on}(w) & , i < i_{on} < 0 \end{cases} \quad (15)$$

Where k_{off} ($k_{off} > 0$), k_{on} ($k_{on} < 0$), α_{off} , and α_{on} are constants, i_{off} and i_{on} are current thresholds, and w is the effective electric tunnel width.

3.4 Models Comparison

Table 1 shows difference between different models[8]

Table 1 model comparison

Model	Linear ion drift	Nonlinear ion drift	Simmons tunneling barrier	TEAM
State variable	$0 \leq w \leq D$	$0 \leq x \leq 1$	$a_{off} \leq x \leq a_{on}$	$x_{on} \leq x \leq x_{off}$
Control mechanism	current	voltage	current	current
I-V relation	obvious	obvious	uncertain	obvious
Generic	No	No	No	yes
Memristance relation	obvious	uncertain	uncertain	obvious
Accuracy	Lowest	Low accuracy	Highest	sufficient
Threshold exists	No	No	Yes	yes

3.5 KNOWN Memristor Model

Known research team presented a new Known memristor model based on a voltage threshold adaptive memristor model (VTEAM) by selecting parameters of generic memristor models and getting the most accurate approximation of actual memristor. This model overcame the previous models' difficulties like simulating snapforward or snapback effects, frequency properties, and switching variability by embedding new chaotic memristor model which led to more approximation of the actual memristor behavior. This model could also represented the switching threshold as a function of the state variable.[2]

Known team suggested many memristor models starting from mean metastable model then generalized mean metastable model and the final model proposed.

3.5.1 Mean Metastable Switch Memristor Model

A metastable memristor can be represented as a set of N switching elements with dynamical evolution over discrete time intervals. The mean metastable switch memristor (MMS) model implements the limiting case when $N \rightarrow \infty$. The change in the number of switches X, scaled from 0 to 1,[2]

$$dX = N_{ON} - N_{OFF} \quad (16)$$

Where the number of switches is represented as:

$$N_{ON} = P_{ON}(1 - X) \quad (17)$$

$$N_{OFF} = P_{OFF}X \quad (18)$$

Switching probabilities when voltage V is applied are given as:

$$P_{ON} = a \frac{1}{1 + e^{-\beta(v - v_{on})}} \quad (19)$$

$$P_{OFF} = a \left(1 - \frac{1}{1 + e^{-\beta(v + v_{off})}} \right) \quad (20)$$

Where V_{ON} is the threshold voltage for switching to the low resistance state, V_{OFF} is the threshold voltage for switching to the high resistance state, $a = dt/\tau$ is the time parameter, and τ is the time constant of the memristor.

Then, the equation of the state variable of the memristor takes the form of:

$$\frac{dx}{dt} = \frac{1}{\tau} \left(\frac{1}{1 + e^{-\beta(v - v_{on})}} (1 - x) - \left(1 - \frac{1}{1 + e^{-\beta(v + v_{off})}} \right) x \right) \quad (21)$$

Furthermore, the conductivity of the memristor is as follows:

$$G = \frac{x}{R_{on}} + \frac{1-x}{R_{off}} \quad (22)$$

3.5.2 Generalized Mean Metastable Switch Memristor Model

MMS model can be generalized to represent the total current through the device which represented by the sum of the currents of the resistive memory element $I_M(V, t)$ (MMS model) and the Schottky diode $I_S(V)$:

$$I = \Phi I_M(V, t) + (1 - \Phi) I_S(V) \quad (23)$$

Where $\Phi \in [0, 1]$. A value of $\Phi = 1$ implies that there is no Schottky diode current.

The $I_S(V)$ current is required to represent the Schottky barrier over the metal semiconductor junction, and in turn, can be decomposed into forward and reverse bias components as follows:

$$I_S = \alpha_f e^{\beta_f V} - \alpha_r e^{\beta_r V} \quad (24)$$

Where α_f and β_f are positive parameters that specify the exponential behavior of the forward and reverse current flowing through the Schottky barrier.

3.5.3 Modification of Memristor Model

To make GMMS meet fingerprints and get adequate model, it goes through three stages of structure modification. At the first stage, it is necessary to introduce a functional dependence of the threshold parameters V_{ON} and V_{OFF} on the internal state variable X . The second stage is aimed at frequency modification of the memristor model. The third stage includes the final modification of the model, taking into account the variability of the SET and RESET switching processes by using the technique

of embedding a chaotic generator into a regular memristor model to introduce variability into the threshold voltage values V_{ON} and V_{OFF} .

The final equations of the modified model of the GMMS memristor is as follows:

$$I = \Phi I_M(V, t) + (1 - \Phi) I_S(V) \quad (25)$$

$$I_S = \alpha_f e^{\beta_f V} - \alpha_r e^{\beta_r V} \quad (26)$$

$$I_M = \left(\frac{X}{R_{ON}} + \frac{1 - X}{R_{off}} \right) V \quad (27)$$

$$\frac{dx}{dt} = \frac{1}{\tau} \left(\frac{1}{1 + e^{-\beta(v - v_{on})}} (1 - x) - \left(1 - \frac{1}{1 + e^{-\beta(v + v_{off})}} \right) x \right) \quad (28)$$

$$\frac{dF}{dt} = a_f \left(\sqrt{\left| \frac{d^2 V}{dt^2} \right| / V} - b_f F \right) \quad (29)$$

$$\frac{d\gamma}{dt} = a_\gamma Z \quad (30)$$

$$\frac{dZ}{dt} = a_Z (c_Z S - b_Z Z + \gamma - \gamma^3) \quad (31)$$

Where γ and Z are state variables, S is an external signal, a_γ and a_Z are time coefficients of the system, b_Z is a feedback coefficient, and c_Z is a signal coefficient. [8]

After talking about memristors modelling, the next section will talk about how to fabricate memristors using Inkjet technology.

4 Memristor Fabrication

After talking about memristor models in the previous section, in this section we will talk about how to fabricate memristors. There are many fabrication methods used to fabricate memristor. They can be divided into non-contact and contact fabrication as shown in Figure 21. [7]. In this paper only Inkjet technology will be focused on.

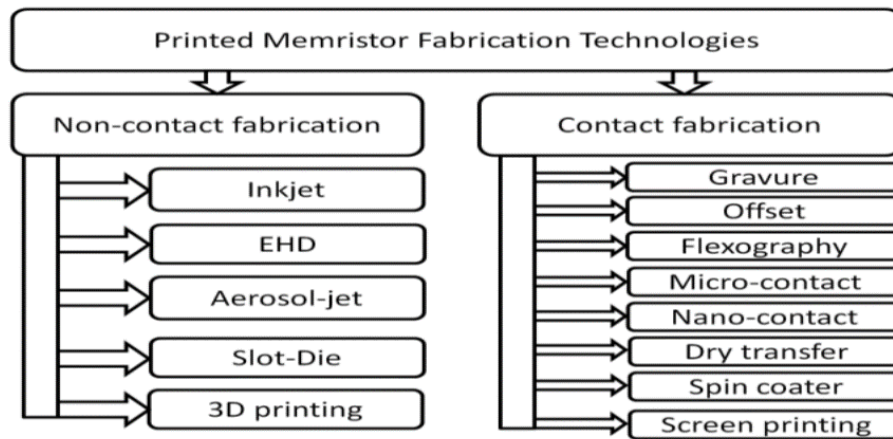


Figure 21. Different memristor fabrication technologies[7]

4.1 Inkjet

Modern applications like neural networks and cognitive computing need flexible and very small size memristors with high density fabrication. Inkjet printing is highly promising to fabricate cation-based memristor (which is called electrochemical metallization cell (ECM) used in HP and Knowm) devices on flexible substrates because it allows deposition of very small volumes of ink rapidly, achieving high pattern precision and resolution with greater reproducibility compared to other techniques.

Inkjet technology has been wide used due to the following reasons:[15]

1. **Flexibility:** Ability to fabricate memristor devices on flexible substrates
2. **Fabrication simplicity:** simple and few steps to fabricate memristor with high precision
3. **Cost effective:** inexpensive fabrication capability compared with conventional semiconductor processing fabrication.

Inkjet technique is the method in which synthesized Silver (Ag) ink (in the suitable range i.e., viscosity, surface tension, conductivity etc.) is used to fabricate metal-insulator-metal (MIM) device to form memristor by jetting Ag ink through printer nozzle at high frequency and deposit on a substrate in the shape of thin films with the help of computer-controlled mechanism. Computer tune parameters to achieve the target output in terms of line width, thickness and fabrication speed. Substrate treatment is very important for the inkjet printing to get uniform lines and strong adhesion. Usually untreated or wrongly treated substrate results in ink spreading or uneven line patterns which make circuit short or open circuit problems specially in small pitch patterns[7]

Then, Enhanced Joule Heating (by applying high current to the device) is applied at a specially optimized hourglass-shaped device pattern to form active oxide medium (Ag₂O) as shown in Figure 22. Joule Heating is used because forming metal oxide needs high post-annealing temperature and the

flexible and thermally fragile substrate cannot withstand this temperature. This makes the annealing temperature is severely limited and stable oxide growth difficult.

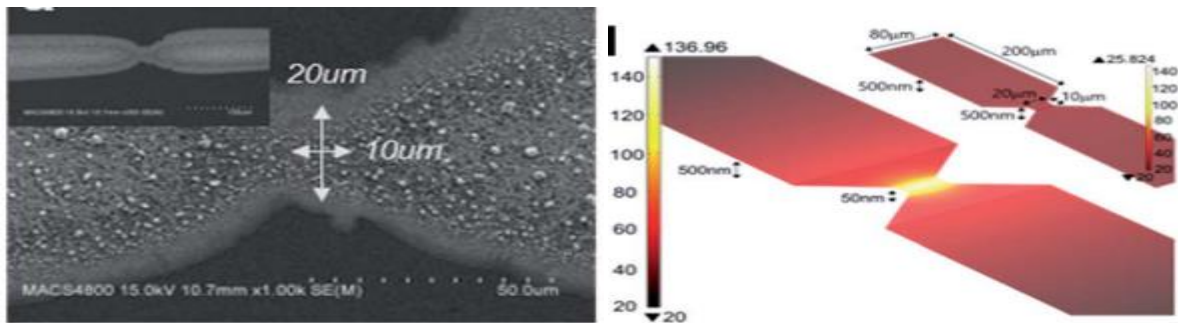


Figure 22. Hourglass shape of memristor device[15]

The resulting Ag/Ag: Ag₂O/Ag stack consists of two electrodes of Ag and one insulator of Ag₂O. This device can be used in resistive switching (SET&RESET) as a memristor according to the size and polarity of the applied electric field.

There are challenges of using Inkjet technology such as:[15]

First is the choice of defect species that can readily migrate within the dielectric layer and switch the electrical conduction behavior of the device.

Second is the need to obtain the materials in the form of jettable ink: the size of the nanoparticles comprising the ink should be smaller than 1/50 of the nozzle orifice to avoid nozzle clogging.

But these challenges can be solved by using Silver (Ag) as follows:

- Silver (Ag) is a metal with high oxidation potential and easily oxidized into cations within the insulator layer where they migrate toward the counter electrode.
- Silver (Ag) can be in the form of nanoparticle ink and can be used easily without clogging the nozzle.

Figure 23 shows inkjet printer:

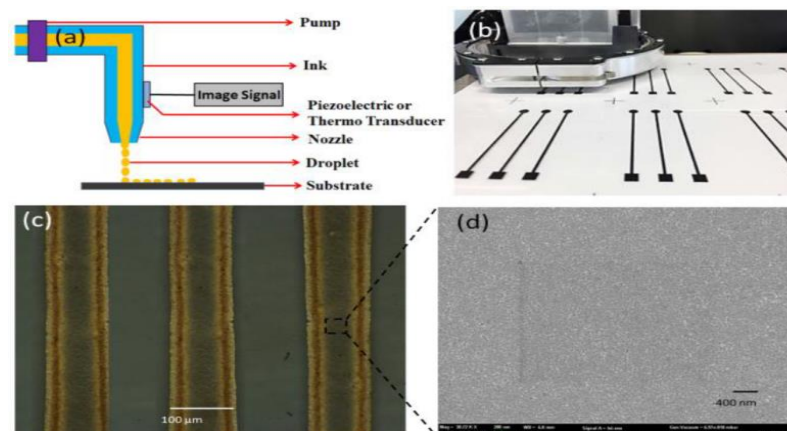


Figure 153 (a) inkjet printer schematic diagram, (b) inkjet printed memristor bottom electrodes, (c) microscopic image of memristor electrodes, (d) SEM image of printed silver electrode.[5]

In [15] a group of researchers applied experiments on two different commercial inks and they are Inktech and Nova centric, denoted as ink A and ink B respectively. Dimatix-2831 inkjet printer with 16 piezo-response nozzles was used for printing, and a polyimide substrate was warmed up to 60°C during printing. According to the datasheet, ink A and ink B were post dried and annealed after printing for 20 minutes at 150° C and 250° C respectively in a convection oven under an atmospheric environment. For the test device to assess the metallic property, 500 nm-long features were printed with a line width of 80 nm which is the smallest based on a 10 pl nozzle cartridge head and 25 nm-drop size. All the I–V characteristics were measured with a semiconductor parameter analyzer HP 4155. And the experiment showed the ability to fabricate a memristor using single metal ink.

Inkjet printers mainly operate in two mechanisms, piezoelectric and thermal. In piezoelectric method the droplet is generated through a vibration of piezo crystal inside the nozzle head whereas, in the thermal inkjet technique a bubble is generated in the nozzle head through applied voltage to generate a droplet.[7]

For another fabrication technologies can be referred to [7].

After talking about memristors fabrication, the next section will talk about the most common applications of memristor.

5 Applications of memristor

Applications of memristor can be divided into two categories crossbar array or discrete as shown in the Figure 24.

5.1 Crossbar array

Crossbar topology is composed of a grid of horizontal and vertical traces. At each intersection (junction), a vertical trace is connected to a horizontal trace by a memristor. The size of each junction is about 2-3 nm (compared to the transistor junctions in the 90 nm technology that is about 60 nm) so it is one of the most promising nanostructures to be used. The crossbar has a large number of memristors so, it can be used to perform a large number of computations like Deep Learning Acceleration. Any memristor at the junction can be programmed or read by applying a voltage to the necessary horizontal and vertical traces while letting the remaining traces float.[16]

Advantages of the crossbar that, it has potentially cheaper and easier fabrication process, scalability, flexibility and its high density.[17]

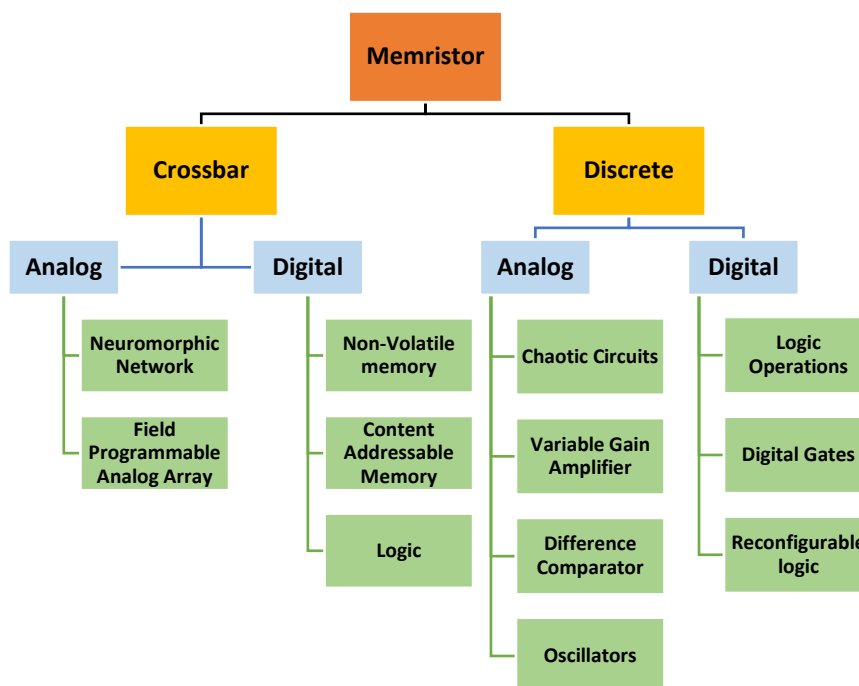


Figure 24. Applications of memristor

5.1.1 Analog

5.1.1.1 Neuromorphic circuits[18]

Crossbars has multi-input and multi-output and behaves like programmable neural networks. The switching characteristics can be trained for pattern classification and neuromorphic computing. Memristor based neurocomputing allows to mimic the computation performed in biological nervous systems.

Memristors can directly implement some functions of biological neurons and synapses, most importantly, synapse-like plasticity, and neuron-like integration and spiking. In these solutions, the information is encoded and transferred in the form of voltage or current spikes.[19]

5.1.1.2 Field Programmable Analog Array

It is designed to perform parallel computing by merging memory, analog and digital computing in single physical fabric to achieve a computing platform for end users

5.1.2 Digital

5.1.2.1 Nonvolatile memory applications

Memristors can keep memory states and data unaffected when power is off because resistance is read with alternating current. So, it can be used to fabricate Non-volatile random-access memory, or NVRAM. There are 3nm Memristors in fabrication now.[20]

Memristors can change between set and reset states according to applied voltage. In bipolar resistance switching case, positive voltage applied to set the memory and a negative voltage to reset the memory to its previous state. In unipolar resistance switching case, the applied voltage should be greater than other two threshold voltages to alter its state.[21]

5.1.2.2 Logic Circuits

Memristors combine information processing and storage in the memory itself so it can be used widely in logic circuits, concerning their nonvolatility, fast switching speed, small area and energy dissipation. Memristor-based logic circuits could be classified as follows:

- Material implication (IMPLY): computation of Boolean functions using imply and reset logic operations;
- Hybrid memristor/CMOS: combination of memristors and CMOS components in Boolean logic and threshold logic computations.
- Programmable interconnects: logic operations in crossbar arrays relying on the use of programmable interconnections between crossbar nanowires.
- Network-based computations: massively parallel computations relying on array-like structures which accommodate networks of memristive components.

5.2 Discrete

5.2.1 Analog

5.2.1.1 Chaotic Circuits

This circuit is complex, sensitive to inputs and difficult to predict behavior so, it produces non-periodic oscillations. The memristor as a nonlinear element is well suitable for encryption and random number generation as chaotic systems. The memristor makes it possible for better control and simpler versions of chaotic systems. Chaotic control is applicable in wide areas like laser physics, fluid mechanics, chemical engineering and electric power systems.[22]

5.2.1.2 Variable Gain Amplifier

In this circuit, the memristor is used as a feedback element which can be controlled with a continuous time automatic gain control (AGC) to act as variable resistor to use it for amplification or attenuation. The analysis and simulation of this circuit is based on a linear vacancy drift memristor model.

5.2.1.3 Difference Comparator

This circuit is based on preserving the memristance value, thus obtaining a programmable resistance that can be used in several circuit configurations. This could be achieved by chopping techniques which has been used to control the charge integrated in the device in order to avoid drift effects.

Memristors are at nanoscale so, their sizes are less than that of a standard resistor implemented in CMOS, which means a significant reduction in silicon area. Moreover, the memristance can be easily programmed through digital pulses.[23]

5.2.1.4 Oscillator

Memristors can be used in RC phase shift oscillators, colpitts Oscillators, Memristor-Based Canonical Oscillators, Memristor-Based Chua Oscillators and other oscillators. Memristor based oscillators are observed as promising candidate for oscillator associative realization and increasing the performance due to memristor's characteristics like nanoscale dimension, low power consumption and electronic programmability.[24],[25]

5.2.2 Digital

Memristors can be used in a discrete scale as logic gates. This can be shown in Figure 25.[26]

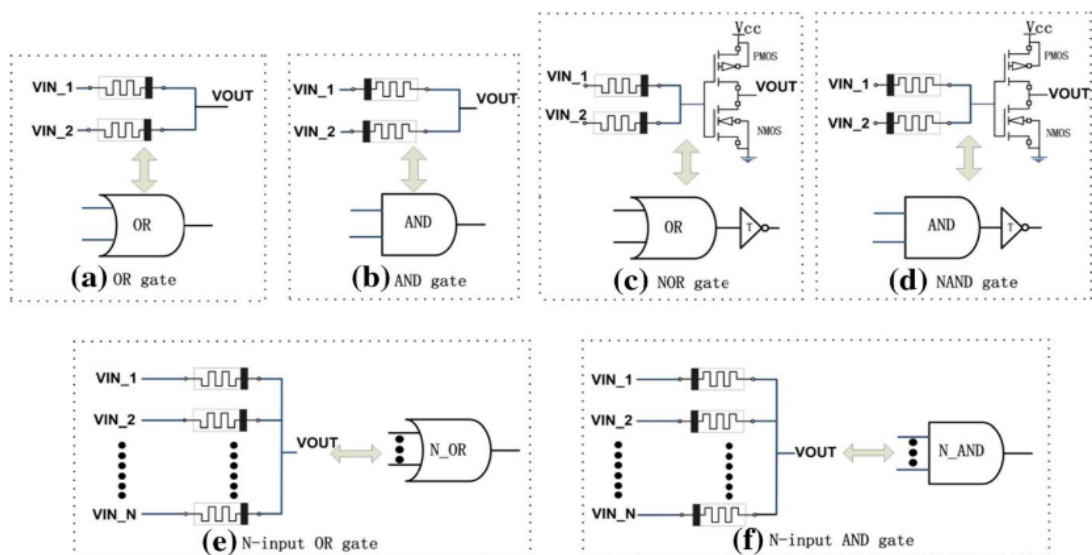


Figure 25. The OR, AND, NOR, NAND gates constructed by memristors[26]

6 Conclusion

This survey presented briefly a description of the fourth passive circuit element, the memristor (M) and its history. Memristors in markets like HP consists of Pt/Tio₂/Pt and KNO₃W (W) dopant type (from four versions of memristor W, C, Sn and Cr of KNO₃W Inc.) have been presented and structure of each of them have been showed. Different Models of memristors have been viewed as linear ion

drift model, nonlinear ion drift model. Different nonlinearity problems have been discussed and window functions (like Joglekar's, Biolek, Prodromakis and Zha window functions) used to solve these problems have been presented. The differences between each of them have been shown. And another models Simmons tunnel barrier model, threshold adaptive memristor [TEAM] and comparison between these models have been shown. Different fabrication technologies have been viewed including two technologies, on-contact fabrication and contact fabrication technology. This survey focused on Inkjet technology for the characteristics and features mentioned above. Different applications of memristive devices have been presented in two categories crossbar array and discrete, each of them divided to digital and analog.

7 Discussion

What can a memristor do?

Memristor element enters into many applications such as Neuromorphic networks and field programmable analog array in analog crossbar array. It also can be used in non-volatile memory, content addressable memory and logic circuit in digital crossbar array. It can be in discrete structure and used in discrete applications. Thus, it caused a leap in electronics world.

8 Future Work

Memristor has a promising future to be used in many future applications. In Artificial Intelligence, simulated memristors can be used as a part of the human brain as a memory. It is also expected for memristor to make a leap in neuromorphic system where memristor can serve as a key element in the implementation of VLSI for neural networks. Memristors can also be used to create new materials namely lithium-based oxides such lithionic. In the electronics field, Memristor can be used as a transition from electronics to Ionics.

References

- [1] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, 2008, doi: 10.1038/nature06932.
- [2] V. Ostrovskii, P. Fedoseev, Y. Bobrova, and D. Butusov, "Structural and parametric identification of known memristors," *Nanomaterials*, vol. 12, no. 1, 2022, doi: 10.3390/nano12010063.
- [3] Y. Oğuz, "Mathematical Modeling of Memristors," *Memristor and Memristive Neural Networks*, no. April, 2018, doi: 10.5772/intechopen.73921.
- [4] R. S. Williams, "A short history of memristor development," *Report*, pp. 1–5, 2012, [Online]. Available: <http://scholar.google.com/scholar?hl=en&btnG=Search&q=intitle:Introduction+to+Nonlinear+Network+Theory#0>
- [5] A. Isah and J. M. Bilbault, "Review on the Basic Circuit Elements and Memristor Interpretation: Analysis, Technology and Applications," *J. Low Power Electron. Appl.*, vol. 12, no. 3, 2022, doi: 10.3390/jlpea12030044.

- [6] V. Keshmiri, "A study of Memristor Models and applications," pp. 1–115, 2014, [Online]. Available: <http://www.diva-portal.org/smash/get/diva2:774476/FULLTEXT01.pdf>
- [7] S. Ali, S. Khan, A. Khan, and A. Bermak, "Memristor Fabrication through Printing Technologies: A Review," *IEEE Access*, vol. 9, pp. 95970–95985, 2021, doi: 10.1109/ACCESS.2021.3094027.
- [8] A. G. Radwan and M. E. Fouda, *On the mathematical modeling of memristor, memcapacitor, and meminductor*. 2015.
- [9] L. Chua, "If it 's pinched it 's a memristor," vol. 104001, doi: 10.1088/0268-1242/29/10/104001.
- [10] D. Biolek, Z. Biolek, V. Biolkova, and Z. Kolka, "Some fingerprints of ideal memristors," *Proc. - IEEE Int. Symp. Circuits Syst.*, pp. 201–204, 2013, doi: 10.1109/ISCAS.2013.6571817.
- [11] J. Sun, L. Yao, X. Zhang, Y. Wang, and G. Cui, "Generalised mathematical model of memristor," *IET Circuits, Devices Syst.*, vol. 10, no. 3, pp. 244–249, 2016, doi: 10.1049/iet-cds.2014.0381.
- [12] H. Search, C. Journals, A. Contact, M. Iopscience, and I. P. Address, "Modelling of nanostructured TiO₂-based memristors," vol. 034001, doi: 10.1088/1674-4926/36/3/034001.
- [13] A. G. Alharbi and M. H. Chowdhury, "Memristor Emulator Circuits," *Memristor Emulator Circuits*, 2021, doi: 10.1007/978-3-030-51882-0.
- [14] Á. Rak and G. Csereny, "Macromodeling of the memristor in SPICE," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 29, no. 4, pp. 632–636, 2010, doi: 10.1109/TCAD.2010.2042900.
- [15] K. J. Yoon *et al.*, "Electrically-generated memristor based on inkjet printed silver nanoparticles," *Nanoscale Adv.*, vol. 1, no. 8, pp. 2990–2998, 2019, doi: 10.1039/c9na00329k.
- [16] N. Nithya, "Materials and Applications of Memristor," no. 5, pp. 171–176, 2020.
- [17] I. Vourkas and G. C. Sirakoulis, *Memristor-Based Nanoelectronic Computing Circuits and Architectures*. 2015. doi: 10.1007/978-3-319-22647-7.
- [18] E. Miranda and J. Suñé, "Memristors for neuromorphic circuits and artificial intelligence applications," *Materials (Basel)*, vol. 13, no. 4, 2020, doi: 10.3390/ma13040938.
- [19] A. Mehonic, A. Sebastian, B. Rajendran, O. Simeone, E. Vasilaki, and A. J. Kenyon, "Memristors—From In-Memory Computing, Deep Learning Acceleration, and Spiking Neural Networks to the Future of Neuromorphic and Bio-Inspired Computing," *Adv. Intell. Syst.*, vol. 2, no. 11, p. 2000085, 2020, doi: 10.1002/aisy.202000085.
- [20] R. Marani, G. Gelao, and A. G. Perri, "A review on memristor applications," no. 1, 2015, [Online]. Available: <http://arxiv.org/abs/1506.06899>
- [21] C. Hodson, "Materials and Applications of ALD," *Processing*, no. July, pp. 171–176, 2009.
- [22] Y. Peng, S. He, and K. Sun, "Chaos in the discrete memristor-based system with fractional-order difference Results in Physics Chaos in the discrete memristor-based system with fractional-order difference," *Results Phys.*, vol. 24, no. March, p. 104106, 2021, doi: 10.1016/j.rinp.2021.104106.
- [23] O. A. Olumodeji and M. Gottardi, "Memristor-based comparator with programmable hysteresis," *2015 11th Conf. Ph.D. Res. Microelectron. Electron. PRIME 2015*, pp. 232–235, 2015, doi: 10.1109/PRIME.2015.7251377.
- [24] G. Wang, M. Cui, B. Cai, X. Wang, and T. Hu, "A chaotic oscillator based on HP memristor model," *Math. Probl. Eng.*, vol. 2015, 2015, doi: 10.1155/2015/561901.
- [25] M. Itoh and L. O. Chua, "Memristor oscillators," *Int. J. Bifurc. Chaos*, vol. 18, no. 11, pp. 3183–3206, 2008, doi: 10.1142/S0218127408022354.
- [26] G. Liu, S. Shen, P. Jin, G. Wang, and Y. Liang, "Design of Memristor - Based Combinational Logic Circuits," *Circuits, Syst. Signal Process.*, vol. 40, no. 12, pp. 5825–5846, 2021, doi: 10.1007/s00034-021-01770-1.