Design and Implementation of inexpensive dual band Echo Sounder

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Abstract– Naval Warning department at Military Technical College (MTC) designed Echo Sounder systems for measuring sea depths. These systems have helped MTC teams achieve significant success in international robotic competitions. However, when students graduate, their knowledge is often lost. This paper documents the process of developing a low noise dual band echo sounder with long range capability using FPGA for future MTC projects.

Two dual band-hydrophones resonate at 50 kHz and 200 kHz were used for transmission and reception to minimize the cost of the project. FPGA is used to generate pulses with 10 Hz period repetition frequency (PRF) which can be controlled remotely from PC using Universal Asynchronous Receiver and Transmitter (UART) protocol. Echo received is attenuated proportional to the delay time. So, a Time Variable Gain (TVG) control was developed to control the amplifier with a totally controlled gain properties using PC. Then, amplified signal was detected using enhanced envelope detection algorithm applied to FPGA. This paper summarizes the results of the project.

Keywords-Dual band, Echo sounder, Low noise, dual channel

I. INTRODUCTION

Echo sounder is based on the principle that transmitting a signal with proper average power and waiting for the reflecting echo from the seabed. Measuring the delay time between the transmission process and the peak detection process of the returned echo to calculate the depth of the sea as shown in (1):

$$\textbf{Distance} = 1/2 * \textbf{velocity} * \textbf{delay} \quad (1)$$

However, Higher frequencies get attenuated, while the lower frequencies can travel long distances in water. The attenuation loss for the ultrasonic signal in water is very high due to high frequency So increasing the average power of the transmitted signal is necessary to achieve long range detection with the help of high sensitivity of the receiver. The intensity of received echo which called echo level (EL) depends on the average power of the transmitted wave (Source Level), the loss in intensity as the sound wave spreads in the water and absorbed by water (Transmission loss), the target strength (TS) as shown in equation (2):

$$EL = SL - 2*TL + TS \quad (2)$$

One method used for solving this problem is increasing the transmission pulse width (τ) which will reduce range resolution as a result. So, increasing the transmission rate per second (PRF) which will increase the average power of transmission is a good solution. Besides reducing the on-chip noise for reception process will help in long range detection capability of the device.

The dual band dual channel printed circuit board (PCB) was designed to minimize the size of the board and reduce the on-chip noise level around the spectrum of 50 and 200 kHz.

II. HARDWARE DESIGN

THE TRANSCEIVER BOARD WAS DESIGNED USING EDA SOFTWARE CONSIDERING THE REDUCTION OF THE ON-CHIP NOISE DUE TO CHIP ELECTROMAGNETIC WHICH RESONANT THE PCB NOISE AROUND CERTAIN FREQUENCIES. OUR DESIGN WAS DIVIDED INTO THREE PARTS.

A. Transmitter module design

Electrical pulses are generated using FPGA before converting them into acoustic pulses with the help of a transducer. These electrical pulses usually have a defined frequency 50 or 200 kHz. This pulse duration is called tau (τ) and is usually in the range 0.1-0.5 ms for better resolution.

Transmitter part consists of two channels. The transmitted signal generated in the FPGA needed to have more average power so increasing the current of these signals and raise the up-down voltage for transducer bias is required. For these requirements MOSFET driver and MOSFET pair are used.

1) MOSFET Driver

A push-pull MOSFET pair is required and to drive these MOSFET transistor pairs, a dual MOSFET driver is used. MD1213 solves this purpose [1]. This MOSFET driver operates at supply voltages between 4.5 and 13V and therefore, compatible with the FPGA board used in this project. MD1213 has separate power connections enabling the output signal L and H levels to be chosen independently from the supply voltages. These connections from component data sheet are shown in figure.

2) MOSFET Pair

The output pulses from the MD1213 MOSFET Driver need to produce High Voltage pulses for transmission. An essential feature of these transistors that they have a low output impedance so that the signals can be successfully injected into the transducer circuits without affecting the matching circuit. Depending on our application MOSFET TC6320 [2] was used. TC6320 is a high voltage, low threshold N and P channel Enhancement-Mode MOSFET Pair. It can operate at high speeds and high voltages. TC6320 has integrated Gate to Source resistor and Gate to Source Zener Diode on both channels. The output voltage can be toggle between + 100 V to -100 V. The connections are shown in figure 1.

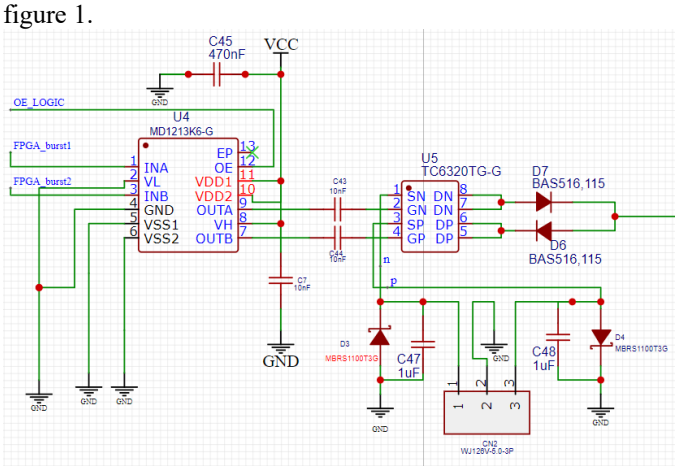

Fig. 1 MOSFETs connections schematic.

3) Transmitter/Receiver Switch

For separating the transmitter and receiver parts from each other during transmission a dual channel high voltage protection transmitter/receiver switch was used. The high voltage protection T/R Switch, MD0100 [3] is a very good solution. This switch is bidirectional and designed for its operation in ultrasonic applications. The connections of the component are shown in figure 2.

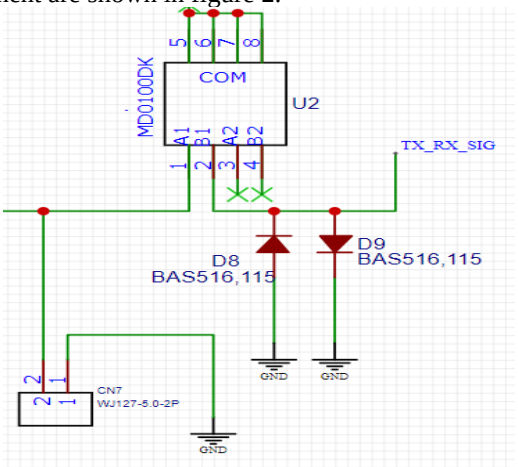

Fig. 2 T/R Switch connections schematic.

B. Receiver module design

Receiver was designed for dual channel dual band signals. Thus, we consider the noise resonance due to electromagnetic coupling and decoupling. The locations of the coupling capacitors are chosen to be closely to the components. Another enhancement was using a low noise variable gain amplifier with its two channels connected in series can be used for providing the TVG to the incoming pulses. Thus, improving the Signal to Noise Ratio (SNR) and dynamic range.

1) Filter design

After the reception of the received signal immersed in noise. It is necessary to design a certain filter to separate the required band from noise. A single state bandpass filter was designed around the transmitted signal frequency.

2) Variable Gain Amplifier

Variable gain amplifiers are easily available but there are some requirements which help in filtering out the unnecessary signals. It is desired that amplifiers can provide a high gain range. The bandwidth should also be large for different gains at different frequencies which in our case is 50 and 200 kHz.

So, Amplifier AD605 [4] is used in this project. AD605 is a low noise, differential-input, dual-channel Variable Gain Amplifier. It fulfills the desired characteristics of gain, noise, and supply voltage. It comprises of two variable gain amplifiers which can be connected in series to get higher gain ranges, up to 96dB and it uses a common gain voltage control (VGN) for both the amplifiers to control the variable gain.

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For controlling the amplifier gain a DAC (Digital-to-Analog Converter) is used to generate TVG digitally using FPGA in a way that first, it increases from 0.01 to its maximum value (3.3V) and then it becomes constant at this value before falling to zero and then repeating again. This gain is totally controlled from PC using LABVIEW software.

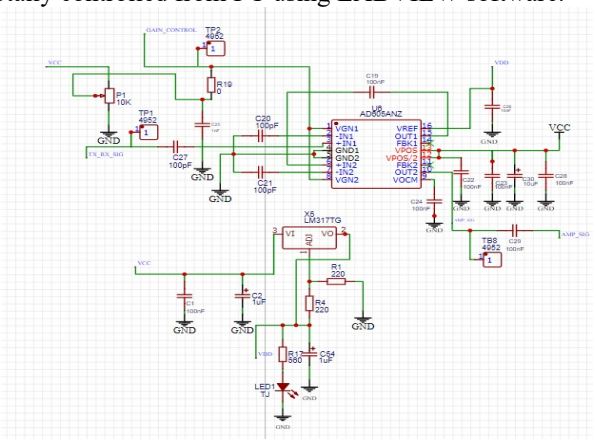

Fig. 3 Dual channel amplifier connections schematic.

3) Analog-To-Digital Conversion.

For measuring the depth of the seabed checking the envelope detection of incoming pulses is required. So, ADC is used to converts analog received signal to digital one on which various process and algorithms can be done using FPGA.

According to Nyquist-Shannon sampling theorem, ADC with high sampling rate speed 5 MHz is used as the high transmission frequency is 200 kHz. Thus, the sampling rate must be at least twice the frequency to avoid the aliasing. The ADC controls pins are controlled by FPAG process. The connections of the component described at data sheet are shown in figure 4.

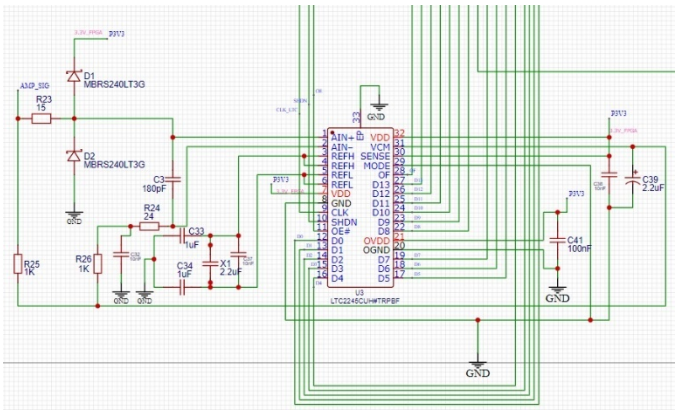

Fig. 4 ADC connections with amplified echo.

III. HARDWARE FABRICATION

After Hardware design has been done, the PCB transceiver card was implemented. The following figure shows the total component schematic used to design the PCB.

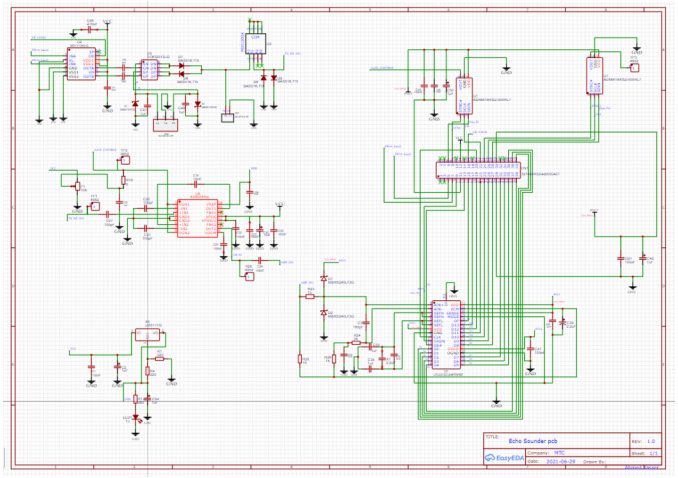

Fig.5 Transceiver schematic using EASY-EDA.

The PCB tracks was calculated to withstand signal power and separated with sufficient space to avoid coupling problems. The following figure shows the PCB layout after reducing the on-chip noise levels.

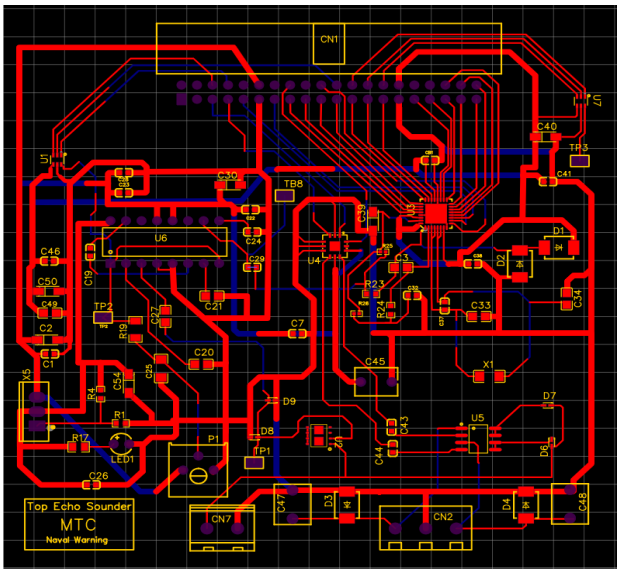

Fig. 6 PCB layers.

A 3D model was generated to imagine the transceiver card shape before implementing it. This model is generated using EASY-EDA software.

Fig. 7 Transceiver board 3D model.

The board was fabricated and tested in the Naval Warning Lab. The components were soldered then each component was tested separately. All components test was done successfully and the transceiver board was ready to transmit desired signals and receive the low-level echo including the white gaussian noise.

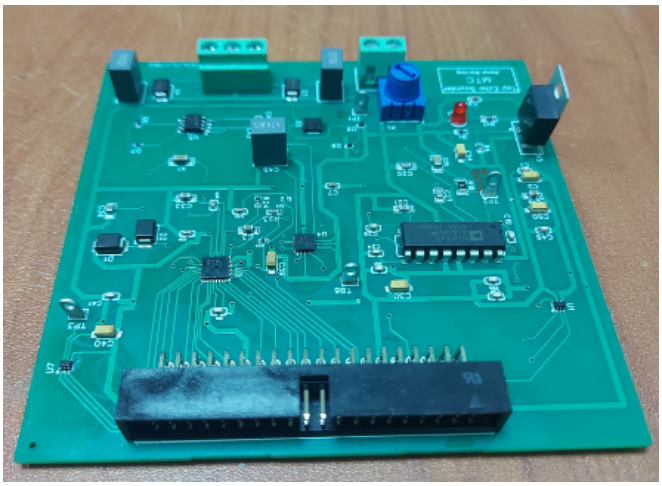

Fig. 8 Fabricated transceiver card.

IV. SOFTWARE IMPLEMENTATION

A. Signal Generation

The generation of the required signals was developed in the FPGA. Dual band frequencies signals with pulse width of 0.4 ms were generated to accomplish a good range resolution with acceptable average power. The transmitted signals are totally controlled by user from PC to use only one band or both channels. Figure 9 shows the signal generation process.

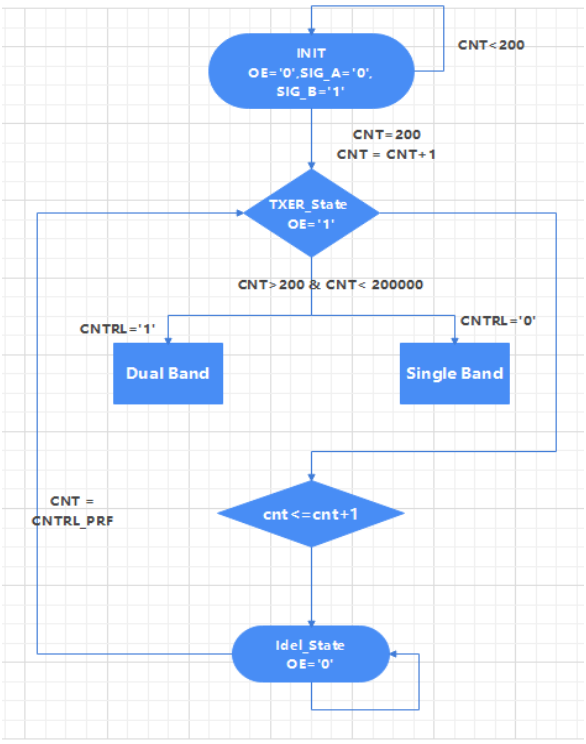

Fig. 9 State machine for signal generation.

B. Time Variable Gain (TVG)

For very low echoes it is required to amplify the received echo with high level of gain. This gain should depend on the attenuation of the sound wave propagates in water. The attenuation mainly depends on the transmitted frequency besides the distance the wave travels. Thus, a time variable gain which amplify the signal depend on the delay of the echo.

The gain was controlled to be constant with any required value from 0 dB to 90 dB or to be time variable gain with specific parameters controlled by user using LABVIEW. The amplifier control signal was generated digitally using FPGA then using DAC to convert it to analog signal. This process is presented as described in fig.10.

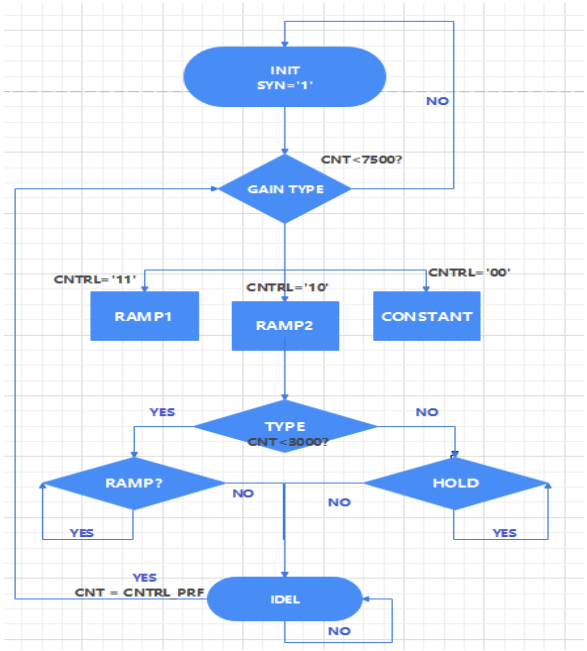

Fig. 10 Gain control signal state machine.

C. Echo detection

After amplification, the echo was converted to digital one using high speed 5 MHz ADC component to perform the required process on the echo signal. The peak echo detection was used besides the envelope detection method to simply detect the peak of the received echo. This method depends on comparing the stored value of the echo with previous one to determine the peak. The multipath echoes from other unrequired targets were rejected by comparing the multiple echoes.

D. Distance Calculation

After detection the peak of the echo, calculating the depth of the seabed is done. First, at transmission a flag signal triggers

a counter to start counting till another flag signal which comes from the envelope detection algorithm process. The counter stores the values then compares this value with other value within the PRF. The delay is calculated and then the depth of the seabed according to (1).

E. UART Protocol

For controlling the transmitted signal and the gain control signal generated by FPGA, it is required to send control commands in real time to FPGA. UART protocol was used to send controlling signal to FPGA. The transmitted protocol consists of 20 byte which fully control the threshold level, gain signal, gain type, transmitted signal parameters, the type of transmission and UART protocol information.

However, controlling signal is necessary for control. The reception protocol is required to present the depth in good user interface, echo signals and any error message during protocol transmission.

The UART module was developed in FPGA and it consists of four main parts: transmitter module, receiver module, transmitted protocol memory and receiver protocol memory. The module was test successfully and ready to be used.

F. FPGA RTL design

All the previous modules were integrated into one main module. Syngenesis is done for DE1-SOC from Altera using Quartus software. The post mapping for area and time was enhanced by the software and the generated jic file was burn into FPGA. The Real time logic for the integrated modules is shown in fig.11.

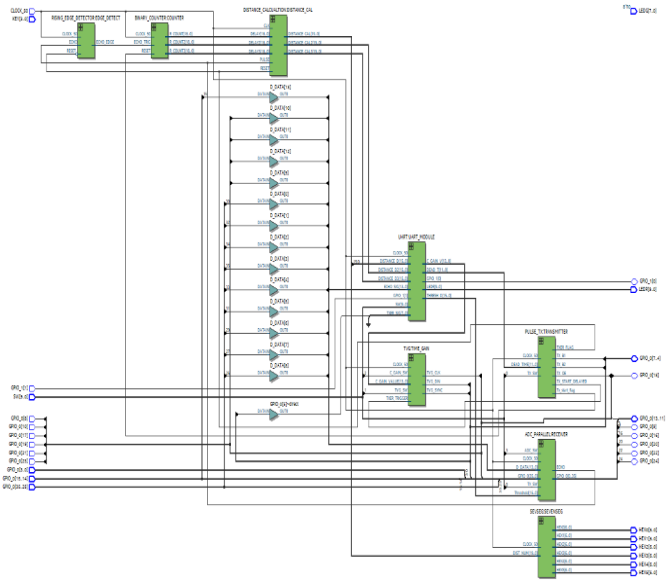

Fig. 11 RTL of integrated modules.

G. LABVIEW Interface.

For good user controlling interface, an enhanced design was developed using LABVIEW software. VISA module presents a solution for serial communications in LABVIEW. This module is used with some changes on the received and transmitted data to form a good user interface.

The front panel includes tabs for UART controlling parameters, echo sounder controlling signals, distances shown in tank view and waveform viewer to present the received echo in real time. Two sliders are used for gain and threshold levels. Gain type and gain values controls are presented in shape of logic switches as shown in fig.12.

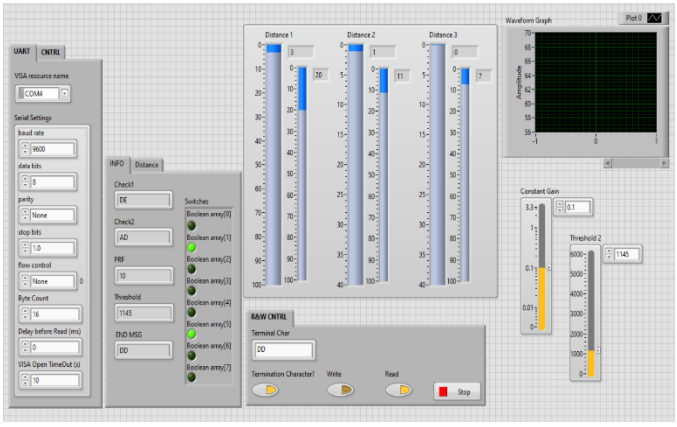

Fig. 12 LABVIEW front panel.

Block diagram panel is the back end of the user interface panel. This panel includes all the required blocks for UART protocol, transmitted control signals, received data and user interface controls. The system was divided into two main modules transmitted protocol and received data as shown in fig.13 and fig.14.

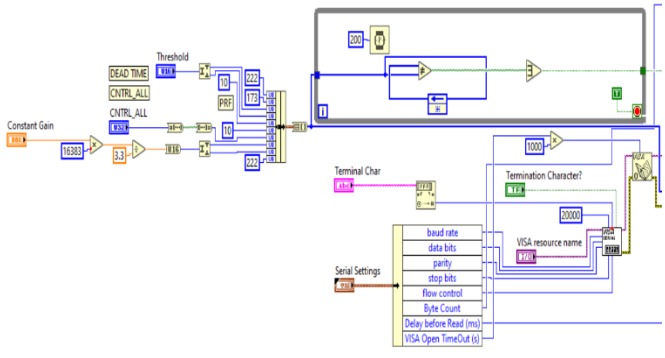

Fig. 13 UART Transmitted protocol blocks in LABVIEW.

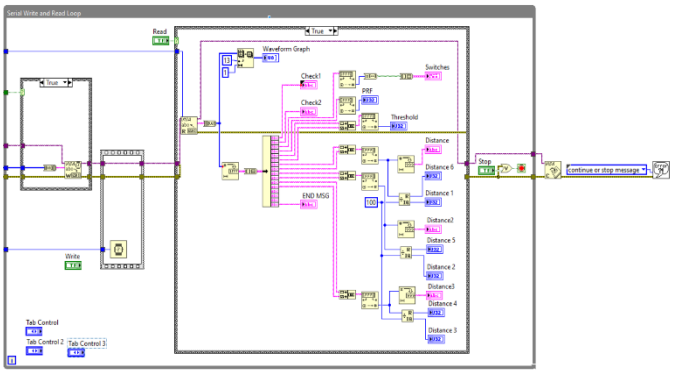

Fig. 14 UART Received protocol blocks in LABVIEW.

V. TANK EXPERIMENT AND TESTING

A. Testing of Transmission

The transmitted burst signals from MD1213 are used as inputs at the gate terminals of the complementary MOSFET pair as shown in figure. The source pins of MOSFET pair are connected to ±30V power supply. The signal was detected using an oscilloscope from GwINSTEK.

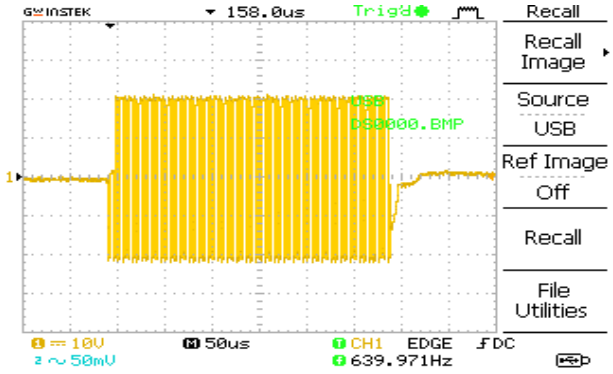

Fig. 15 Transmitted signal measured on oscilloscope.

Testing the band of the transmitted signal was required to prove dual channel transimission. A spectrum analyzer was used to detect both bands as shown in fig.16 and fig.17.

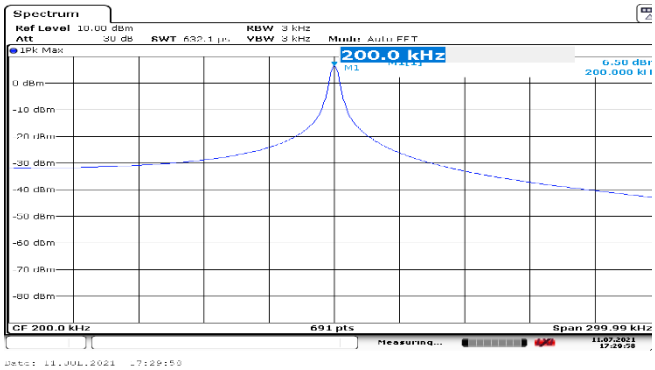

Fig. 17 Spectrum of 200 kHz Transmitted signal.

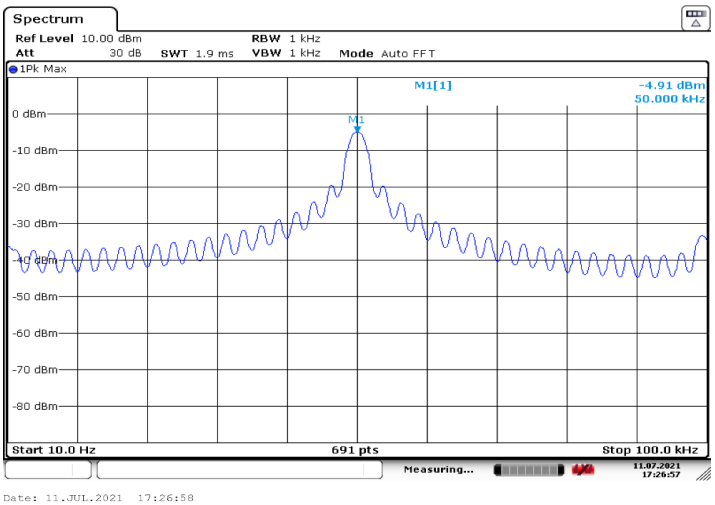

Fig. 18 Spectrum of 50kHz Transmitted signal.

B. TVG Controlling Signal Test

DAC output signal which is used to provide the variable gain to the amplifier was tested on oscilloscope with 10 Hz PRF and signal levels from 0.01V to 3V. The controlling signal was successfully generated using FPGA with the required parameters desired. The following figure shows the test.

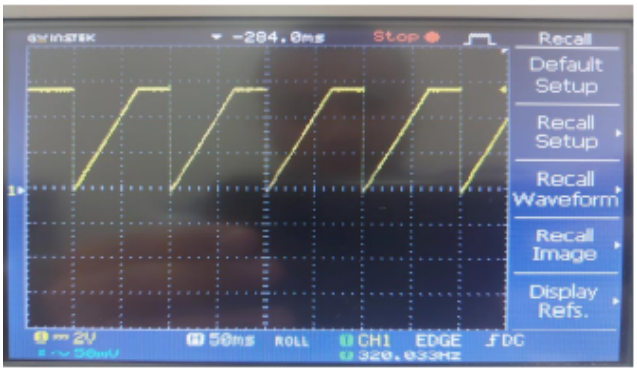

Fig. 19 TVG control signal measured on oscilloscope.

C. *Envelope Detection using ADC and DAC*

The setup was tested for both 50 kHz and 200 kHz pulses. This was done in the same way as in Transmitter part using oscilloscope. The operation of choosing the band is done by the user from PC. The signals have ±30 V up-down levels and was transmitted by the transducer.

Detection of echo from small pool with depth of 70 cm was successfully achieved and detected on the oscilloscope as shown in figure. The multipath problem was presented due to the low level of the water. This multipath echo was eliminated as described before in the envelope detection algorithm used.

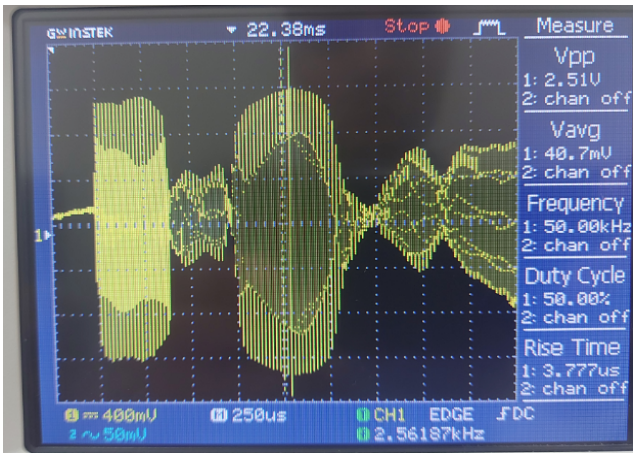

Fig. 20 Echo signal from target measured using oscilloscope.

CONCLUSION

This paper demonstrates the development of a dual band dual channel echo sounder. Noise levels were minimized by keeping the board size small and providing proper ground plane at the bottom layer besides avoiding the coupling effects of the paths of the PCB.

A fully controlled transmission is done using the proper parameters provided by user. These parameters determine the frequency of signals, PRF for transmission, dead time and range resolution. Also, the gain of the amplifier is controlled remotely by user. Thus, improving the Signal to Noise Ratio (SNR) and dynamic range.

The controlled dual channel amplifier, itself offered a very low noise at various gain values. Therefore, preventing any additional electronics noise being added to the echo signal.

Envelope detection of received echo is achieved using FPGA Algorithm. This operation implemented a simple algorithm for extracting the peak values in each cycle of the echo pulses. Tests showed that a very accurate and stable peak detection of pulses with different shapes and amplitudes was possible. Pulses of two different frequencies can be generated and processed by the receiver by user interface.

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