Design of Low Noise-Low Power OTA Using 0.13µm Technology for Infrared Readout Circuits

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***Abstract*— This paper presents the design of operational transconductance amplifier (OTA) as a core building block of the capacitive transimpedance amplifier (CTIA) for the implementation of infrared readout circuit on VLSI chips. The OTA has a two-stage amplifier which achieves low power and low noise. In addition, a voltage reference is designed for biasing the amplifier. Low power dissipation of the OTA is achieved by using of a supply voltage of 1.2 V and transistors operating in the subthreshold region. The designed OTA, built in standard 0.13 µm CMOS technology, dissipates 3.2 µW of power with input referred noise of 52.1 nV/√Hz@1KHz. Also, the OTA has a common mode rejection ratio of 81 dB and input offset voltage of 5.089 µV. This is accomplished by the efficient sizing of the used transistors together with a compensation capacitor.**

Keywords—OTA, CTIA, Low Noise, Subthreshold

I. INTRODUCTION

Recently, the infrared (IR) imaging systems become important for the tactical, industrial, medical and automotive applications. These applications often require imaging of scenes in the 8-14 µm band IR radiation. Due to the object and ambient temperatures, the imaging systems should tolerate undesirable scene disturbances such as sun reflection or laser jamming [1]. The imaging systems must also have minimum power consumption and minimum noise in order to achieve acceptable signal to noise ratio.

The IR detectors are divided into two main categories, first is photon detector and the second is thermal detector. The main different between these two types is the thermal response time which makes the photon detectors faster than the thermal detectors. However, the photon detector need cooling systems which make it more expensive than thermal detectors [2]. Bolometer is one of the thermal detector types which will be used in our application.

There are simple types of IR readout integrated circuit (ROIC) such as source-follower per detector, direct injection, and gate-modulation input which are used in IR ROIC due to its small pixel area and power consumption [2]. While another complex circuit techniques such as buffered direct injection and capacitive transimpedance amplifier (CTIA) have been developed to provide excellent bias control, high injection efficiency, linearity, and better noise performance [2]. The core building block of the CTIA is the OTA which must satisfy low noise and low power consumption as shown in Figure 1.

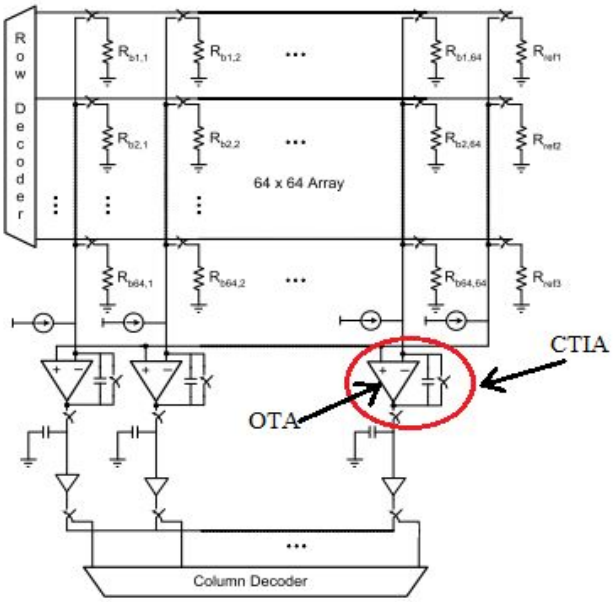

Figure 1 FPA CTIA readout circuit

In the IR focal plane arrays (FPA), illustrated in Figure 1 there are several sources of noise in conventional IR FPA which are originated from the detector and others from the readout electronic component itself. The two main types of the readout electronics noise are thermal and flicker noise which are studied in this paper. Noise can be reduced by either applying noise reduction techniques such as AutoZero, Correlated Double Sampling and Chopper Stabilization technique as an extra circuit [3] or it can be optimized by applying some design rules based on the circuit noise model [4]. The later technique is used in this work.

Duo to rapid progress of technology and scaling large IR FPA up to 1024*1024 pixels, the power consumption became a very important issue. There are several techniques to minimize the power consumption which include bulk driven MOSFETS, floating gates MOSFETS and Subthreshold/Weak Inversion Technique [3]. In this paper all transistors are enforced to work in the subthreshold region.

This work concerns with the design of a low noise OTA as a building block for the CTIA readout circuit technique with

the emphasis on its power consumption and noise performance compared to other works.

II. OP AMP DESIGN

A. *Circuit Topology*

For an application that requires low noise op amps with high gain, good stability, low voltage, and low power consumption, the noise performance is the main consideration [5]. The two-stage op amp topology was chosen to meet these design objectives while keeping focus on the noise performance. Figure 2 shows the circuit schematic of the two-stage op amp. The first stage is the classical differential amplifier which consists of two PMOS transistors as input devices M1 and M2 whose transconductance is g_{m1} which are connected to a current mirror load NMOS transistors M3 and M4. The second stage is a common source amplifier which consists of two transistors M6 and M7 which acts as an output stage that controls the output swing and DC level. The Miller capacitor C_C and the transistor M9 are connected as feedback loop to establish the desired stability and bandwidth. The biasing circuit is a Beta-multiplier reference [6] which consists of M11 and M22 NMOS transistors and M33 and M44 POMS transistors. The resistor R_1 controls the reference current that will flow in the whole circuit. This Beta-multiplier reference circuit biases the two stages of the op amp with almost constant current even if the supply voltage deviates from its original value which is 1.2 volts. Also, the Beta-multiplier circuit needs a start-up circuit to ensure that it works correctly and current flows through the two branches of the circuit. The start-up circuit consists of transistors M21, M23 and M24.

B. *Noise Optimization*

The flicker noise and the thermal noise of the two stage amplifier are respectively given by [7], [3]:

$$V_{feq}^2 = 2V_{f1}^2\left[1+\left(\frac{K_{AN}}{K_{AP}}\right).\left(\frac{L_1}{L_3}\right)^2\right] \quad (1)$$

$$V_{teq}^2 = 2V_{t1}^2\left(1+\sqrt{\frac{K_{PN}}{K_{pp}}.\frac{W_3}{W_1}.\frac{L_1}{L_3}}\right) \quad (2)$$

Where:

$V_{f\_eq}^2$ is the equivalent flicker noise voltage density,

$V_{t\_eq}^2$ is the equivalent thermal noise voltage,

K_{AP} and K_{AN} are the flicker noise coefficients for PMOS and NMOS transistors, respectively.

K_{PP} and K_{PN} are the thermal noise coefficients for PMOS and NMOS transistors, respectively.

L_1 and L_3 are the channel lengths of the transistors M1 and M3, respectively.

W_1 and W_3 are the channel widths of M1 and M3 transistors respectively.

Based on (1) and (2) there are four design keys that can be used to reduce the noise:

1) Using PMOS transistors as input pairs M1 and M2 since $K_{AP} >> K_{AN}$ [3].
2) Ensuring that $W_{1,2} >> W_{3,4}$.
3) Ensuring that $L_{1,2} << L_{3,4}$.
4) Optimization of the sizes and aspect ratios of the MOSFETs.

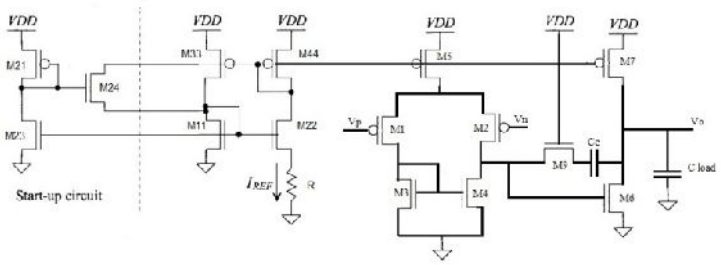

Figure 2 Schematic of overall circuit

C. *Power consumption minimization*

The ideal transistor I-V model assumes that the current only flows from source to drain when $v_{GS} > v_t$. In real transistors, current does not abruptly cut off below threshold, but rather drops off exponentially [8] as shown in Figure 3. In this case the drain current is:

$$I_D = I_{D0}\exp\left(\frac{v_{GS}-v_t}{nV_T}\right).\left(1-\exp\left[\frac{-v_{DS}}{V_T}\right]\right) \quad (3)$$

As v_{DS} is very small in subthreshold region; (3) can be simplified as:

$$I_D = I_{D0}\exp\left(\frac{v_{GS}-v_t}{nV_T}\right) \quad (4)$$

And

$$I_{D0} = \mu.C_{ox}.\frac{W}{L}.V_T^2.e^{1.8} \quad (5)$$

Where:

I_D is the drain current,

W is the transistor width,

L is channel length of transistor,

I_{D0} is the characteristic current,

v_{GS} is the gate-source voltage drop,

v_{DS} is the drain-source voltage drop,

v_t is the threshold voltage of the transistor,

V_T is the thermal voltage (V_T=KT/q),

K is Boltzmann's constant ,

T is the ambient temperature in Kelvins,

q is the charge of electron,

n is inclination of the curve in weak inversion shown in Figure 3,

μ is the mobility of electrons or holes carriers,

C_{ox} is the oxide capacitance per unit area,

$e^{1.8}$ is empirical term.

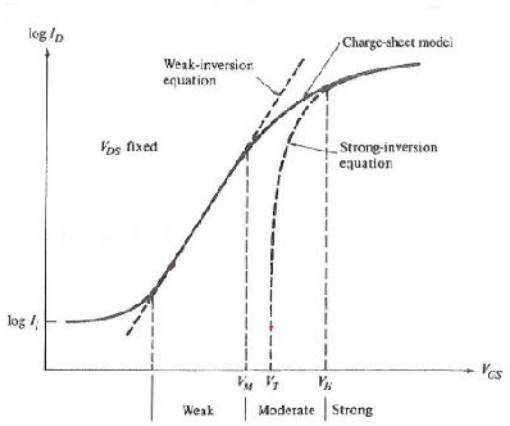

Figure 3 subthreshold region of the MOSFET

This current called subthreshold current and in this case the transistor is operating at the so-called weak inversion region or subthreshold region.

Also, the transconductance of a transistor operating in weak inversion region is [3]:

$$g_m = \frac{I_D}{nV_T} \quad (6)$$

The point at which a transistor enters the weak inversion region is approximately [3]:

$$v_{GS} \leq v_t + V_T \quad (7)$$

The transistor will be saturated in weak inversion when [3]:

$$v_{DS} \geq 3V_T \quad (8)$$

So equations (7) and (8) must be satisfied to ensure that the transistors are operating in the weak inversion region.

D. Op amp specifications

The op amp which is used in the CTIA readout circuits must consume minimum power to be compatible for portable IR cameras. In addition it should have minimum noise and acceptable gain. As the frame rates of the IR cameras range from 30 Hz to 60 Hz the very wide bandwidth of the op amp is not required, so we need only the sufficient bandwidth for this range. Also the OTA should have a good common mode rejection ratio (CMRR) to reject the bolometer dark current.

In accordance, the target specifications of the presented design are specified as outlined in TABLE I**.**

TABLE I TARGET SPECIFICATIONS

Parameters	Target Value
DC Power Consumption	< 3 μW
DC open loop gain	> 70 dB
Total input referred noise @ 1KHz	< 100 nV/√Hz
Phase margin	> 60°
Unity gain band width	> 500 KHz
F 3dB frequency	> 100 Hz
CMRR	> 80 dB
Input Offset voltage	< 1 mV
Slew rate	> 0.01 v/μsec

E. Design steps of the OTA

According to requirement of low power and low noise op amp, the device sizes and biasing conditions will be designed using the following steps:

Step 1: The desired phase margin will be used for selection of the minimum value for Cc, i.e. for a 60° phase margin we use the following relationship [7]:

$$C_c = 0.22C_L \quad (9)$$

Step 2: Choosing the total bias current of the two-stages of the OTA according to the required power consumption:

$$I_{bias} = \frac{P_{diss}}{V_{DD}} \quad (10)$$

Step 3: Determining the 1st stage bias current from the slew rate (SR) requirement[7]:

$$I_{D5} = SR \times C_c \quad (11)$$

So the current that will flow in each branch of the 1st stage of differential amplifier will be:

$$I_{D1} = I_{D2} = \frac{I_{D5}}{2} \quad (12)$$

Hence the 2nd stage bias current is given by:

$$I_{D7} = I_{bias} - I_{D5} \quad (13)$$

Step 4: Setting the gate-source voltage v_{GS} of the transistors operating in subthreshold region. From (7) v_{GS} can be determined knowing that the threshold voltage v_t is a technology parameter.

Step 5: Determining the aspect ratios of transistors M1, M2, M3, M4 and M5 using (4) and (5) such that it operates in the subthreshold region.

Step 6: Determining the aspect ratios of transistors M6 and M7. For the 60° phase margin, the location of output pole is assumed to be placed at 2.2 times unity gain bandwidth [7], so the transconductance g_{m6} can be given by:

$$g_{m6} = 2.2g_{m2}\left(\frac{C_L}{C_c}\right) \quad (14)$$

$$S_6 = S_4 \cdot \frac{g_{m6}}{g_{m4}} \quad (15)$$

$$S_7 = S_5 \cdot \frac{I_7}{I_5} \quad (16)$$

Where: S=W/L

Also, increasing g_{m6} will improve the stability of the OTA, this is called pole splitting [9].

Step 8: Right half plane (RHP) zero Compensation of the OTA: The RHP Zero introduces negative phase shift or phase lag in the transfer function of op amp which makes the stability be more difficult, so connecting a resistor (R_z) in the feedback series with the compensation capacitor C_c will be a suitable solution. The RHP Zero for the two-stage amplifier is given as[9]:

$$\omega_z = \frac{-1}{C_c\left(\frac{1}{g_{m6}} - R_z\right)} \quad (17)$$

From (17) the value of R_z will control the RHP Zero and equal $1/g_{m6}$ to eliminate it. Now, the resistance R_z will be replaced by a transistor M9 so the aspect ratio of M9 can be determined by:

$$R_z = r_{ds9} = \frac{1}{\mu_n C_{ox} S_9 V_{eff}} \quad (18)$$

$$S_9 = \frac{1}{R_z \mu_n C_{ox} V_{eff}} \quad (19)$$

F. Beta-multiplier voltage reference design

The OTA is designed first with an ideal current source; this "golden" current source assumes that the current does not change with the variation of supply voltage V_{DD}. Now, we need to design a transistor based voltage reference that generate a reference current with minimum sensitivity to the variation of V_{DD}. Figure.4 shows such a circuit that is designed specifically for this purpose. The right part of the circuit is a self biased current mirror. The current in the right branch that flow in M22 and M44 is mirrored in the left branch in transistors M11 and M33 and vice versa so this circuit is called a "self biased" circuit. As the currents in the right and left branches are replicas for each other; the resistor R is inserted into the circuit to control the reference current. From Figure.4 we can write:

$$V_{GS11} = V_{GS22} + I_{ref} \times R \quad (20)$$

$$V_{GS} = \sqrt{\frac{2 I_D}{\beta}} + v_t \quad (21)$$

For saturated transistor,

Where $\beta = \mu . C_{ox} . \frac{W}{L}$

So from **(20)** V_{GS11} must be greater than V_{GS22} and $\beta_{11} < \beta_{22}$, let $\beta_{22} = K\ \beta_{11}$ which is satisfied by $W_{22} = K \times W_{11}$, where K is constant. Here we "multiply-up" M11's β in M22 so that less gate-source voltage is needed to conduct I_{ref}, so this circuit called a Beta-multiplier voltage reference circuit. The reference current I_{ref} is expressed in [10] as:

$$I_{ref} = \frac{2}{R^2 \beta_{11}}\left(1 - \frac{1}{\sqrt{K}}\right)^2 \quad (22)$$

Here, note that (neglecting the finite output resistance of MOSFETs) the reference current I_{ref} is independent of V_{DD}. Solving for R, and assuming K= 3, R can be expressed as:

$$R = \frac{1}{\sqrt{2\beta_{11} I_{ref}}} \quad (23)$$

Knowing the desired reference current and the process parameters then the value of the resistance R can be determined. Also, the aspect ratios of M11, M22, M33 and M44 can be obtained using equations (4) and (5).

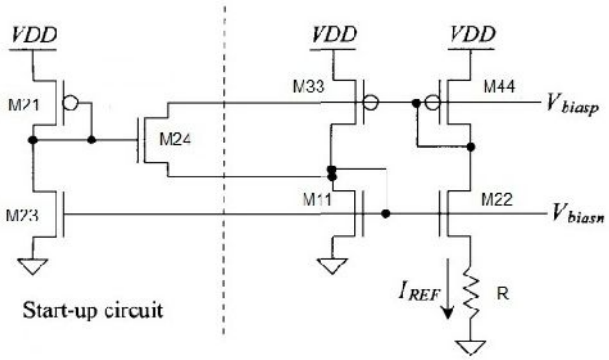

Figure.4 beta-multiplier voltage reference

Now, let's turn our attention to the start-up circuit shown in Figure.4 An important issue in any self biased circuit is that it has two different operating points one is just described and the other is the degenerate bias point [10] which occurs when the gates of M11/M22 are connected at ground while the gates of M33/M44 are at V_{DD}. At this situation all transistors carry zero current and may remain off because the loop support a zero current in both branches. The start-up problem can be solved by the M21, M23 and M24 transistors. As the gates of M11/M22 are at ground the gate of M23 is grounded and it is off, the gate of M21 is between V_{DD} and V_{t21} and as a result M24 which operates as a switch turns on and leaks current into the gates of M11/M22 from the gates of M33/M44 then M23 turns on and M24 turns off. Note that during normal operation the start-up circuit should not affect the Beta-multiplier's operation.

III. SIMULATION RESULTS

The OTA is designed in standard TSMC 0.13 µm CMOS process and simulated using CADENCE® software. Employing the above equations and design procedures then using some iteration on the tool, low power and low noise OTA has been designed with aspect ratios as shown in TABLE II.

TABLE II THE DESIGN ASPECT RATIOS

Device	Type	Aspect ratio W/L (µm)
M1,M2	P	100 / 0.26
M3,M4	N	11.1 / 18.1
M5	P	2.1 / 0.26
M6	N	10.6 / 0.26
M7	P	16.4 / 0.26
M9	N	0.26 / 2.7
M11	N	64 / 20
M22	N	3*64 / 20
M33,M44	P	63 / 20
M21	P	0.3 / 20
M23	N	50 / 0.26
M24	N	0.26 / 20

According to the simulation results, the open loop gain of operational amplifier is 73.6dB, unity gain bandwidth is 382.7 KHz, phase margin (PM) is 61°, gain margin 42dB as shown in the AC response in Figure 5.

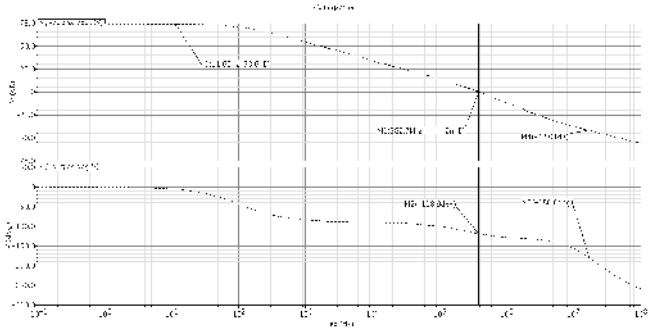

Figure 5 AC response of OTA

Also, the input referred noise is 52.1 nV/√Hz and the output noise is 13.39 µV/√Hz measured at 1KHz as shown in Figure 6 and Figure 7.

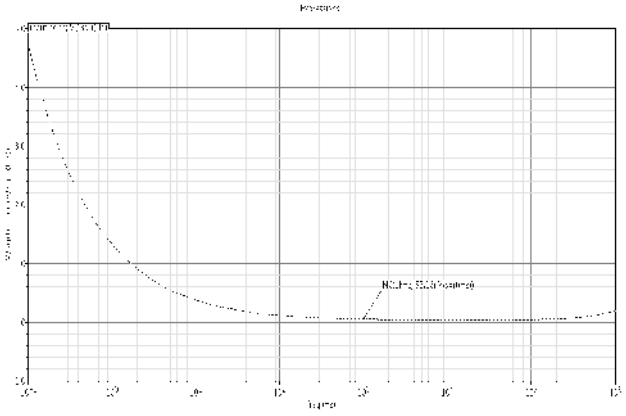

Figure 6 Input referred noise

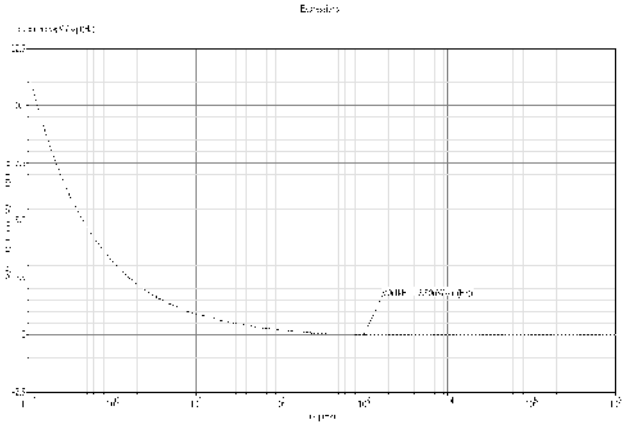

Figure 7 Output noise

The total power consumption of the designed OTA is 3.24 µW including the two-stage amplifier and the beta-multiplier voltage reference, while the power consumption of the two-stage amplifier without voltage reference is only 2.33 µW.

The designed beta-multiplier voltage reference achieves 8.59 nA/Volt reference current variations with the supply voltage V_{DD} changes as illustrated in Figure 8.

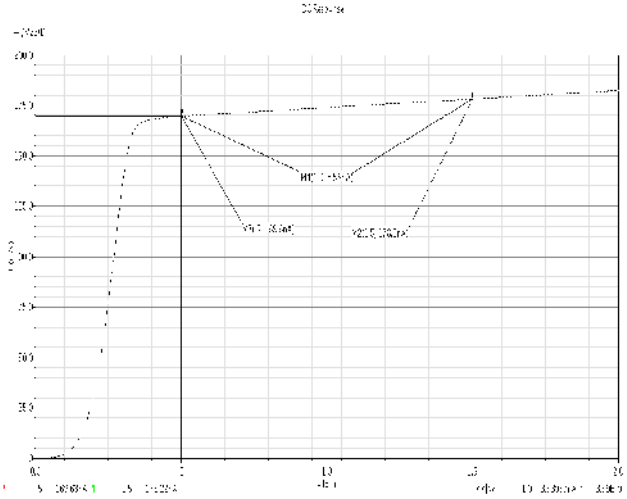

Figure 8 Reference current variation with V_{DD}

The simulation results of the designed OTA are compared to similar designs which are published in[11], [12] and [13]. These comparisons are summarized in TABLE III.

TABLE III SIMULATION RESULTS AND COMPARISIONS

parameter	[11]	[12]	[13]	This work
Supply voltage (V)	5	5	±1.5	1.2
DC Power Consumption(W)	NA	0.28m	1.43m	3.24 µ
DC open loop gain(dB)	75.75	NA	74	73.6
Total input referred noise @ 1KHz (nV/√Hz)	NA	Output: 11µ@ 1MHz	95	52.1
Phase margin(deg)	NA	NA	62°	61°
Unity gain band width (Hz)	NA	NA	1M	383.1 K
F 3dB frequency(Hz)	5 M	NA	NA	105
CMRR (dB)	108.9	NA	NA	81
Input Offset voltage (V)	26m	NA	2.52m	5.089 µ
Slew rate (v/µsec)	NA	1	+0.6 , -0.9	±0.0029

IV. CONCLUSION

An operational transconductance amplifier (OTA) has been designed and simulated. The design achieves low power and low noise requirements. A voltage reference has been designed for biasing the amplifier. The design of the low noise and the low power OTA has been explained. The detailed design procedures of the OTA are described. The voltage reference of the OTA is described and designed. The designed OTA was built in standard 0.13 µm CMOS technology, dissipates 3.2 µW of power with input referred noise of 52.1 nV/√Hz@1KHz. Also, the OTA has a common mode rejection ratio of 81 dB and input offset voltage of 5.089 µV.

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