

Military Technical College
Kobry El-Kobbah,
Cairo, Egypt



7th International Conference
on Electrical Engineering
ICEENG 2010

Finite-Difference Time-Domain Analysis and Design of Transition Interconnects in Microstrip-to-Microstrip Package

By

Hussein H. M. Ghouz*

Abstract:

In this paper, a new transition between GaAs chip (Microstrip) and Aluminum motherboard (Microstrip) with a single interconnect and one common ground has been analyzed and investigated using Finite-Difference Time-Domain method. The objective is to optimize the package performance over a wide frequency band up to 50 GHz. This is carried out by performing a parametric analysis to study the effects of the transition interconnect (discontinuity) on the overall package performance. The scattering parameters of interconnect are used as a performance measure of package under investigation. Good results have been obtained up 50 GHz; S_{12}/S_{21} and S_{11}/S_{22} are about -0.4 and -20 dB respectively.

Keywords:

High frequency interconnects in MMIC packages, finite-difference time-domain "FDTD", and Flip-Chip

* College of Engineering, Arab Academy for Science, Technology and Maritime Transport, Cairo, Egypt

1. Introduction:

Flip-Chip technique (Via/bump interconnects) is considered as a technologically wise leading the progress in multi-chip module packages [1-5]. It has been widely used in many applications including electronic and MMIC circuit packaging (Monolithic Microwave Integrated Circuit). Several chips circuits can be mounted together to the motherboard using flip chip technology to increase density, improve system performance, and reduce cost.

Transition in flip chip package involves the use of metallic via holes/bumps to transmit the signal between the chip and the motherboard. These interconnects are considered the main discontinuity which results in partial loss, reflection and possibly distortion of the signal. In addition, coupling between multiple interconnections as well as signal lines are also form another main problem in using the flip chip technique. The compatibility between the flip chip and the planar transmission lines determines the overall match between the integrated circuit and the package. The simplicity of microstrip, its low loss, makes it attractive with the flip chip package as main motherboard and/or chip circuit.

In this paper, a single via hole is used to connect the signal lines in a microstrip package with one common ground mounted on single and multiple substrates as shown in Fig. 1. The microstrip lines shown in Fig.2 are used in our analysis as reference microstrip lines to feed the microstrip package.

A brief summary of the FDTD method has been presented in section II. This includes source excitation model, choice of reference structures, FDTD simulation parameters, boundary conditions and frequency dependent parameters. Simulation assumptions, package dimensions, and non-uniform FDTD grids are presented in section III. The scattering parameters of via transition for different chip and motherboard substrate types as well as via dimensions have been also computed and investigated, and they illustrated in this section. Finally, the paper is concluded in the last section.

2. Theory

Finite-Difference Time-Domain method is well known since 1966 [6]. This method is very attractive for analysis and modeling most of the electromagnetic problems especially active and passive microwave planar circuits [7-10]. It is based on the second order difference form of the space and time of partial derivative operators in Maxwell's curl equations. Using these difference equations, along with the appreciate boundary conditions and proper source excitation, the fields within the assumed computational domain can be obtained and updated as function of time. The main drawback of this method is the implementation of absorbing boundary condition (ABC) which used to terminate the computational domain [11-12]. This problem has been solved using the

perfect matched layers (ABC-PML) [13]. In fact FDTD method can be used to model any arbitrary three-dimension structure by simply assigning the values of electrical permittivity, permeability, and conductivities to each electric and magnetic field components in FDTD lattice. The constitutive parameters of each medium are interpreted by the FDTD algorithm as local coefficients. This makes FDTD algorithm is more convenient to handle any arbitrary multi-layers structure with fully satisfying the continuity of the tangential field components at the boundaries between two different media. Today, the advances in the computer technology (progress in multi-chip module), especially parallel processing, made the FDTD code more conveniently executable on this parallel machine. This dramatically reduced the required CPU time from order of hours to order of mints. The reader can refer to [14-16] for more details about FDTD method.

To understand how to apply the FDTD method to **MS-to-MS** package shown in Fig.1, we should discuss the following:

- Source excitation model
- Reference microstrip structures
- FDTD simulation parameters
- Absorbing Boundary Condition
- Frequency Dependent parameters

Source excitation model: for many uniform guided structures, the electric field distribution at the source plane are initially known, and can therefore be used to excite the package under investigation. However, for many others, in particular most planar circuits, the exact field distributions are not well known in advance. In this case, a quasi-static TEM mode assumption may be used as an initial guess to excite a reference structure in order to get the spatial field distributions at source plane of package input. The choice of the reference structure depends on the geometry of the package under investigation. Thus, a finite length section of transmission line with the same cross section and dielectric layers as the package under investigation is used as a reference structure. In addition, the length of this reference structure should be long enough such that the dominate mode will be developed at its output. Therefore, a gaussain pulse is used to modulate these spatial distribution functions of field components at the source plane to excite the package as

$$E_x(x, y, t) = \varphi_x(x, y, t = t_o) \exp\left[-(t - t_o)^2 / T^2\right] \quad (1)$$

$$E_y(x, y, t) = \varphi_y(x, y, t = t_o) \exp\left[-(t - t_o)^2 / T^2\right] \quad (2)$$

Where,

$\varphi_x(x, y, t = t_o)$ The spatial distribution function of the transverse electric field intensity $E_x(x, y, t=t_o)$ obtained from the air-reference structure

$\varphi_y(x, y, t = t_0)$ The spatial distribution function of the transverse electric field intensity $E_y(x, y, t=t_0)$ obtained from the air-reference structure
 t_0 Time center of the Gaussian pulse
 T The Gaussian pulse width

Equations (1) and (2), are the source excitation at the source plane (x-y plane) of the MS-to-MS package.

Reference microstrip structures: in our FDTD analysis, three main microstrip lines are considered as reference structures. These are Refms₁, Refms₂ and Refms₃ as shown in Fig. 2. The first microstrip line is a single substrate ($r_1 = r_2 = 9.8$ and $W_1 = 240 \times 10^{-6}$ m, $h = 280 \times 10^{-6}$ m), and it has a characteristic impedance of order 54 Ω . The second microstrip line is multi-substrates ($r_1 = 9.8$, $r_2 = 12.9$, and $W_1 = 240 \times 10^{-6}$ m, $h = 280 \times 10^{-6}$ m), and it has a characteristic impedance of order 48 Ω . The third microstrip line is a single substrate ($r_2 = 9.8$, $W_2 = 144 \times 10^{-6}$ m, and $h = h_2 = 140 \times 10^{-6}$ m), and it has a characteristic impedance of order 48 Ω . These reference structures are used to **extract the reflected fields** due to via interconnect from the incident fields at the package input port. To minimize effect of reflection/radiation loss due to the air-dielectric discontinuity on the lunched gaussian pulse in MS₁-to-MS₂ package, MS₂-to-MS₁ package, and the reference structures, two additional reference structures are considered. These are RefmsAir₁ and RefmsAir₂. They are used to excite the MS₁-to-MS₂ package and MS₂-to-MS₁ package, and the other reference microstrip lines (single and multi substrates).

FDTD parameters: dimensions of the assumed package under investigation are presented in table (1). This includes the line widths of MS₁ and MS₂, the dielectric constant of substrate (single/multi), substrate heights and characteristic impedance. The designed FDTD simulation parameters are presented in Table (2). The designed three dimensions FDTD-mesh including uniform and non-uniform grids is shown in Fig.4. A second order non-uniform function which provides smooth transition from low dense mesh to high dense mesh is used as was reported by Ghouz in[2]. Furthermore, the ground and the strip conductors are assumed to be perfect conductors with zero thickness. Also, ideal substrates are considered (no dielectric loss). To save memory and CPU-time required to execute our codes, a perfect magnetic wall (PMC) at center of the package is used.

Absorbing Boundary Condition: in our FDTD simulation, a perfect matched layer is used to terminate the assumed computational domain. The number of matched layers NP=6, and the reflection coefficient is of order 10^{-6} . The reader can refer to [13] for a details about ABC-PML.

Frequency Dependent parameters: the frequency dependent parameters based on the time-domain response of the package are used to investigate and model the effects of the discontinuity on the overall package performance. The most important frequency parameter is scattering parameters (S-Parameters). Propagation constant $\beta(\omega)$, effective

dielectric constant $\epsilon_{eff}(\omega)$, and characteristic impedance $Z_o(\omega)$ of the reference structures are also very important frequency parameters in modeling the discontinuity.

First, for a transmission line model of via hole shown in Fig3, the modified S-parameters reported by Ghouz in [2] are given by:

$$S_{ij}(\omega) = \sqrt{\frac{V_i^-(z_i, \omega) \times I_i^-(z_i, \omega)}{V_j^+(z_j, \omega) \times I_j^+(z_j, \omega)}} \quad (3)$$

Where,

V_i^- denotes the reflected voltage at the package port-i

V_j^+ denotes the incident voltage at the package port-j

I_i^- denotes the reflected current at the package port-i

I_j^+ denotes the incident current at the package port-j

Second, the frequency parameters of the reference structures are [2]:

$$\beta(\omega) = \frac{1}{(z_j - z_i)} \left\{ \phi_i(\omega, z_i) - \phi_j(\omega, z_j) \right\} \quad (4)$$

$$\epsilon_{eff}(\omega) = \frac{\beta^2(\omega, z_i, z_j)}{\omega^2} \quad (5)$$

$$Z_o(\omega) = \frac{FT[V_{in}^{ref}(z_i, t)] \cdot e^{-j\omega\Delta t / 2}}{\sqrt{FT[I_{in}^{ref}(z_{i-1}, t)] \cdot FT[I_{in}^{ref}(z_i, t)]}} \quad (6)$$

Where,

$\phi_i(\omega, z_i)$ denotes the phase of electric field of reference structure at the space location z_i .

$\phi_j(\omega, z_j)$ denotes the phase of electric field of reference structure at the space location z_j .

$V_{in}^{ref}(z_i, t)$ denotes the voltage of reference structure at the input port z_i .

$I_{in}^{ref}(z_i, t)$ denotes the current of reference structure at the input port z_i .

$I_{in}^{ref}(z_{i-1}, t)$ denotes the current of reference structure at the input port z_{i-1} .

3. Simulation Results

In our FDTD simulation, two code types have been developed on MatLab to investigate the effects of discontinuity on the overall package performance. The first code type is used to simulate the MS-package shown in Fig.1 (package code). The second code type

is used to simulate the reference microstrip structures shown in Fig.2 (reference code). Each code is divided into two modules, FDTD-module and Frequency-module (FD-MD & FR-MD).

The FD-MD of first code computes gaussian pulse response of the MS-package for different substrate types and via dimensions. The second MatLab code FD-MD computes the gaussian response of the reference structure corresponding to the MS transition package (transition from MS₁ to MS₂ and vice versa). The FR-MD of the package code uses gaussian response of both reference structure and the MS-package to compute the scattering parameters of the package over a wide frequency range up to 50 GHz (S-parameters defined in Eq.(3)). Effective dielectric constant, propagation constant and characteristic impedance of the reference microstrip structures are computed using the FR-MD of the reference code (Eq.(4) through Eq.(6)). These parameters are compared with the analytical formulas of microstrip line to verify our codes.

Results of our simulation are presented in Fig.5 through Fig.10. Effective dielectric constant and propagation constant of the reference microstrip structures, including air-substrate, single substrate, and multi-substrates, are illustrated in Fig.(5-a) and Fig.(5-b) respectively. It is clear that from the figures, effective dielectric constant and propagation constant are monotonic increasing function of frequency. The case of **air-substrate** is used to verify our codes. Fig. 6 shows the characteristic impedance of reference structures versus frequency. It is clear that excellent matching is achieved between Refms₂ and Refms₃, and good match is achieved with Refms₁. This means that for single substrate MS-package, the transition from MS₁ to MS₂ is in good match with the transition from MS₂ to MS₁. On the other hand, excellent match is achieved in case of multi-substrate transition MS-package. These results have been verified analytically using the design equations of microstrip line [17].

Figure (7-a) shows the S-parameters of the single substrate MS-package. It is clear from the figure that the transition between two microstrip lines with one common ground is asymmetric. In fact, this is due to the matching between lines as well as the nature of interconnect geometry. The via hole in MS-package acts as a via interconnect in MS₁-to-MS₂ transition while it acts as a bump interconnect in MS₂-to-MS₁ transition. The same effect has been obtained in case of multi-substrates MS-package as shown in Fig.(7-b). The magnitude of transmission loss (S₁₂ & S₂₁) of single substrate and multi-substrates MS- package is presented in Fig.8. Excellent values of S₁₂ & S₂₁ have been obtained up to 50 GHz (about -0.4 dB). The effects of the interconnect dimensions (cross-section) have been computed and presented in Fig.9. Enhanced S-parameters for smaller cross-section is achieved. Effect of reflection loss, due to dielectric discontinuity, on the package performance is computed and the results are depicted in Fig.10. It is clear that this effect dominates at higher frequencies. In addition, in case of multi-substrates, effect of reflection loss at lower frequencies is neglected up to 10 GHz.

This is due to the effect of substrates' resonance at the via proximity. Finally, the general and accurate equivalent circuit model of the transition interconnects proposed by Ghouz and reported in [2] can be used to compute the circuit components using the obtained S-parameters along with the propagation constant of the reference microstrip structure.

4. Conclusion

Performance of a new MS-package has been evaluated and presented in this paper. The MS-package has two main configurations: *single-substrate* MS-package and *multi-substrates* MS-package. Each one has single via/bump interconnect and one common ground. The first configuration is used for transition from *MS motherboard* to another *MS motherboard*. On the other hand, the second configuration represents transition from *MS-chip* to *MS motherboard*. In these package configurations, no need to use ground interconnects which in turn eliminate coupling between signal and ground interconnects. Based on the simulation results, the smaller the interconnect dimensions the lower the reflection loss. However, via height as well as the line widths is controlled by the fabrication process and the matching conditions. Furthermore, the via cross section is used as controlling parameter to enhance the overall package performance. Good results of s-parameters have been obtained up to 50 GHz. The present transition has many useful applications in MMIC circuit packages. Future work will include the effects of both conductor loss and substrate loss on the MS-package performance.

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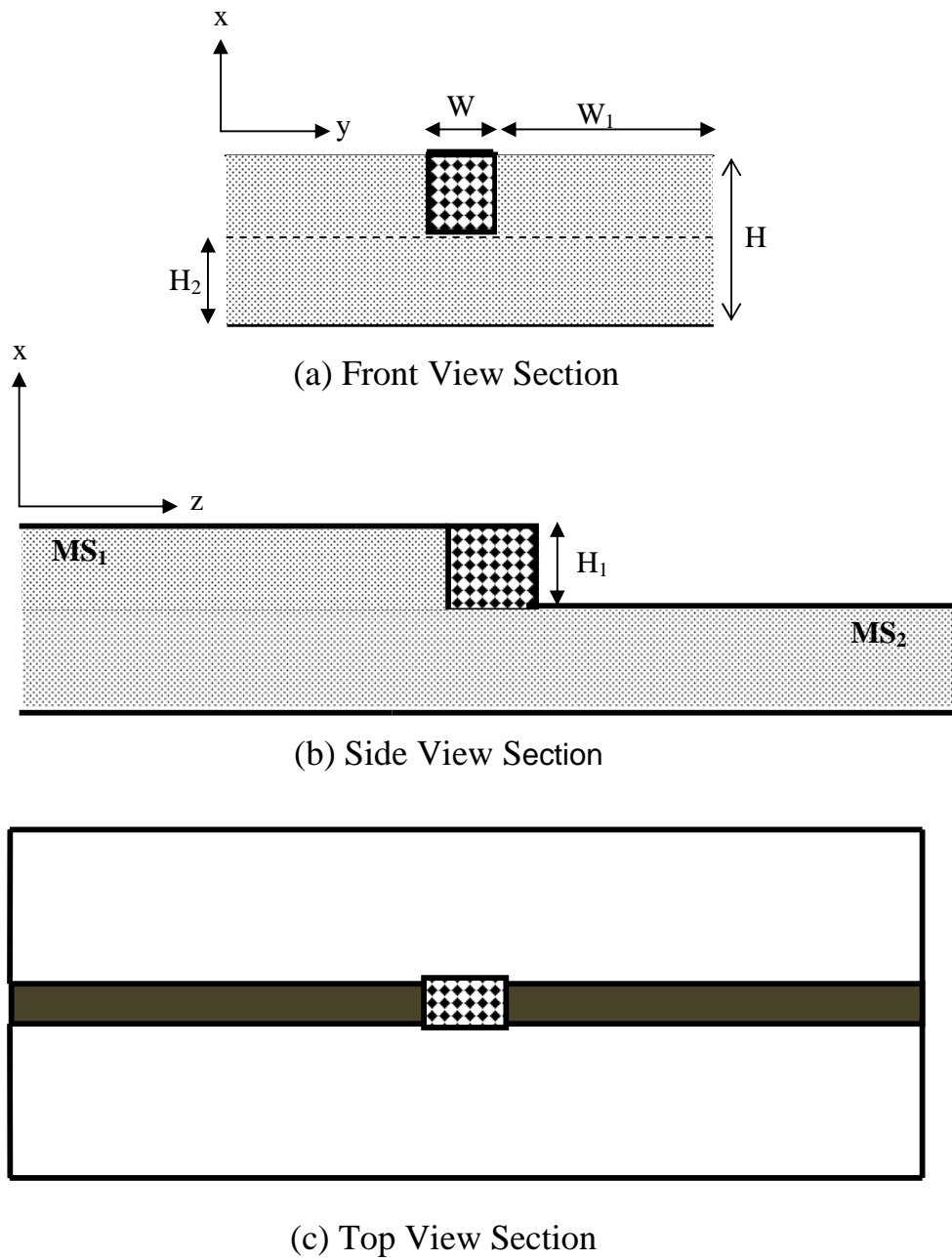


Figure (1): Single via transition interconnect

- Single layer substrate: Transition between Two motherboards
- Multi-layers substrate: Transition between MS_1 GaAs chip and MS_2 Aluminum motherboard

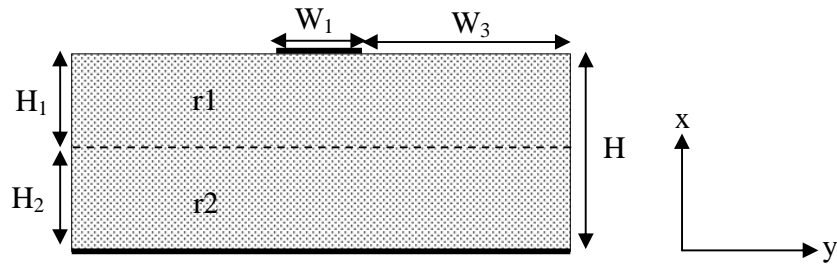


Figure (2-a): Reference Microstrip Structure for MS_1 -to- MS_2 Package

- $r_1 = r_2 = 9.8$, single substrate "Refms₁"
- $r_1 = 12.9$ and $r_2 = 9.8$, multi-substrate "Refms₂"
- $r_1 = r_2 = 1$, Air-substrate "RefmsAir₁"

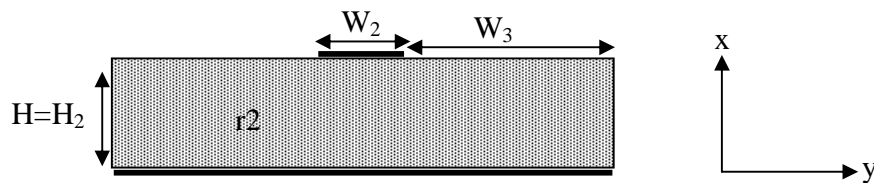


Figure (2-b): Reference Microstrip Structure for MS_2 -to- MS_1 Package

- $r_2 = 9.8$, single substrate "Refms₃"
- $r_2 = 1$, Air-substrate "RefmsAir₂"

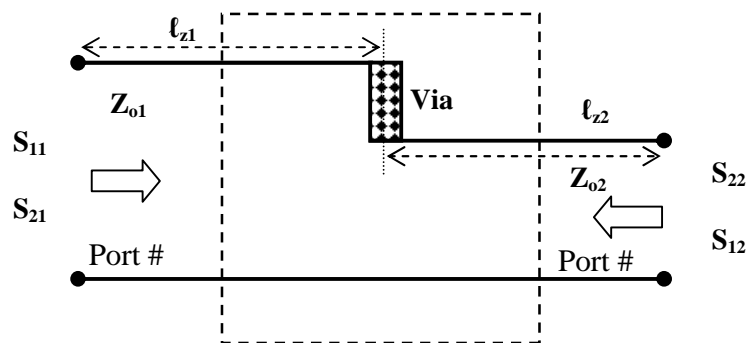


Figure (3): Transmission line model of Via hole transition

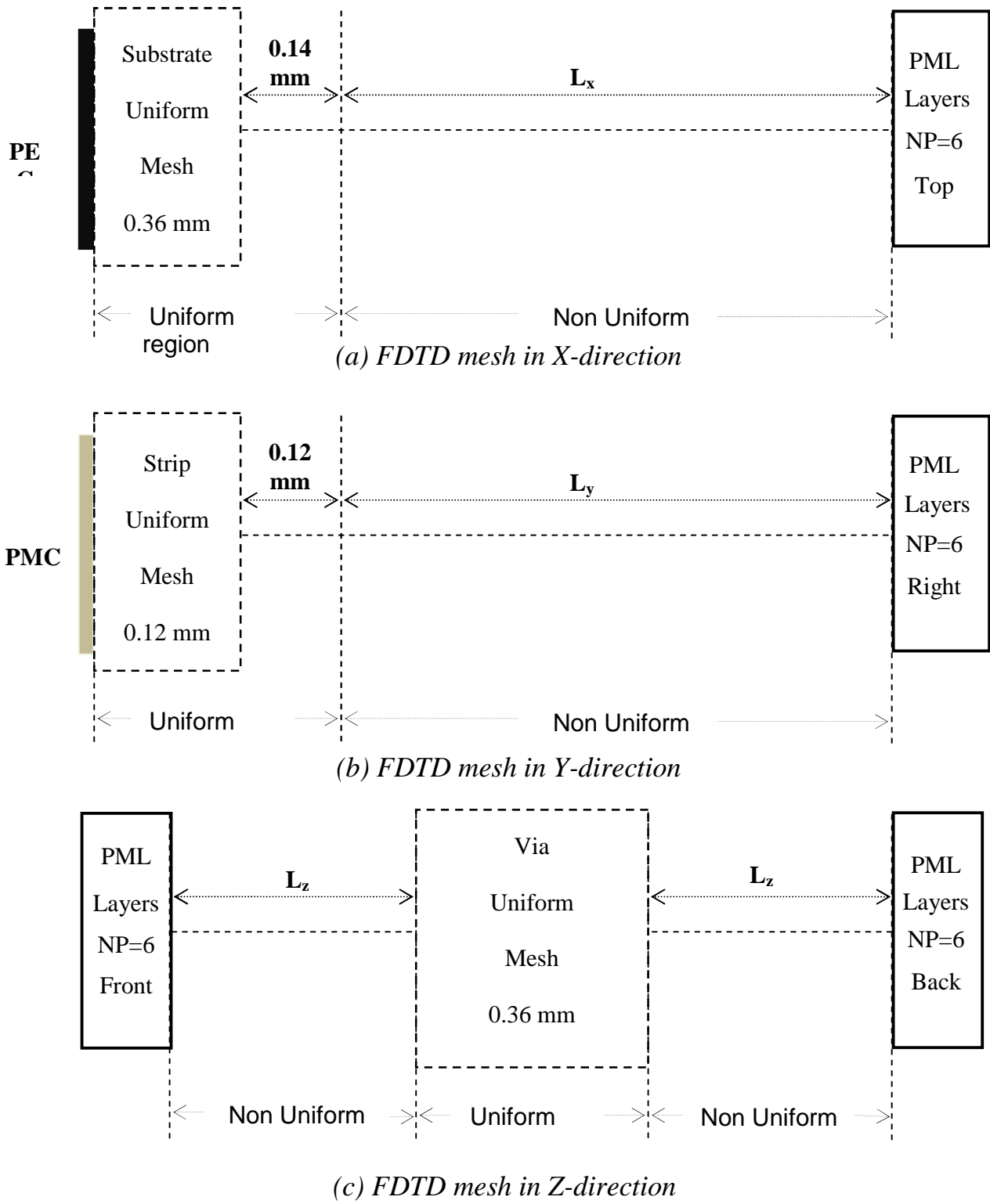


Figure (4): The 3-D FDTD mesh of MS₁-to-MS₂ / MS₂-to-MS₁ package

Table (1): Parameters dimensions of MS-to-MS package and reference structures

	Line Widths in micron	Substrate heights in micron	Dielectric constant # 1 CPW/MS	Dielectric constant # 2 CPW/MS	Characteristic Impedances Z_{oi} in Ohm
Single substrate	240/144	280/140	9.8	-	$Z_{AV1}=48$ $Z_{AV3}=53$
Multi-substrates	240/144	280/140	12.9	9.8	$Z_{AV2}=48$

Table (2): FDTD simulation parameters

Space Parameters in micrometers	Source excitation Parameters Gaussian pulse	FDTD Meshing Parameters
$D_{xo} = 14$	$\Delta t = \text{time step} = 2.4188 \times 10^{-14}$	Non-uniform in x-direction with $L_x = 2.4$ mm (x-mesh) See Fig.4-a
$D_{yo} = 12$	$t_0 = T/2 \approx 900$ time steps $= 2.1769 \times 10^{-12}$ Pulse center	Non-uniform in y-direction with $L_y = 1.2$ mm (y-mesh) See Fig.4-b
$D_{zo} = 12$	$F_{\max} \approx 100$ GHz	Non-uniform in z-direction with $L_z = 3.3$ mm (z-mesh) See Fig.4-c
$D_{\max} = \frac{\min}{50} = 60$		
The required time steps to get the output pulse at the MS_1 -to- MS_2 package's output is about 6000 time steps		
FDTD Computational Domain cells = 85 x 50 x 185		

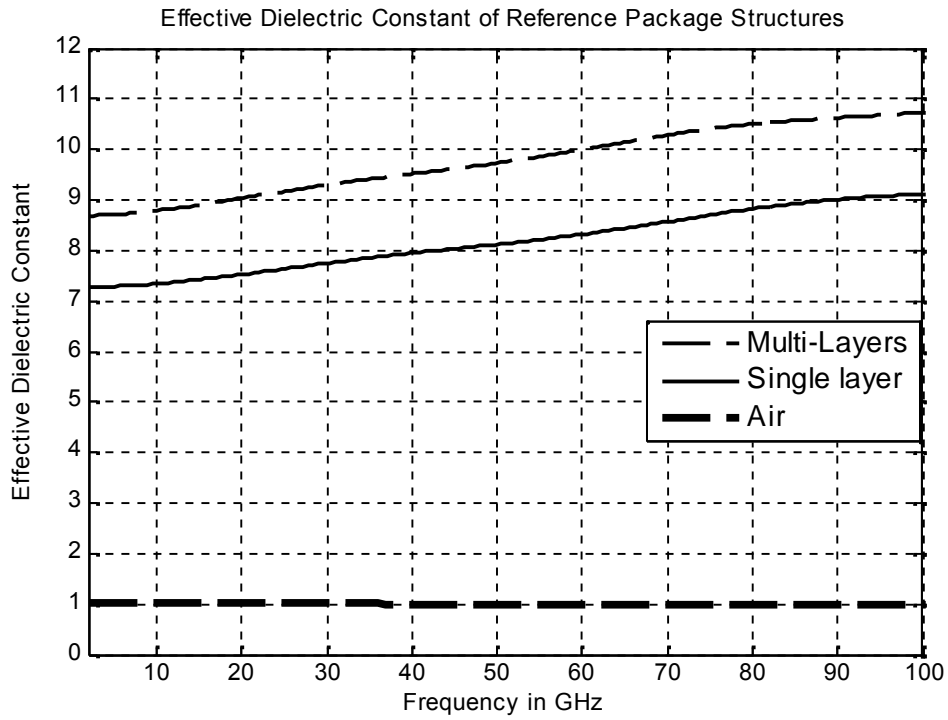


Figure (5-a): Effective Dielectric constant of single and multi-layers reference microstrip structures

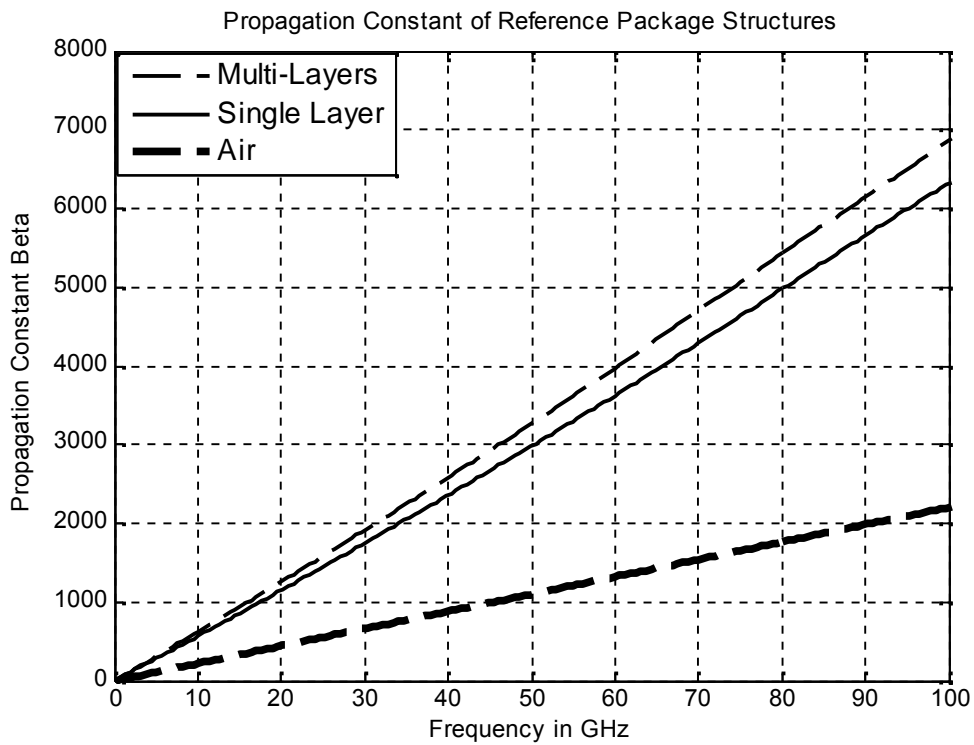


Figure (5-b): Propagation constant of single and multi-layers reference microstrip structures

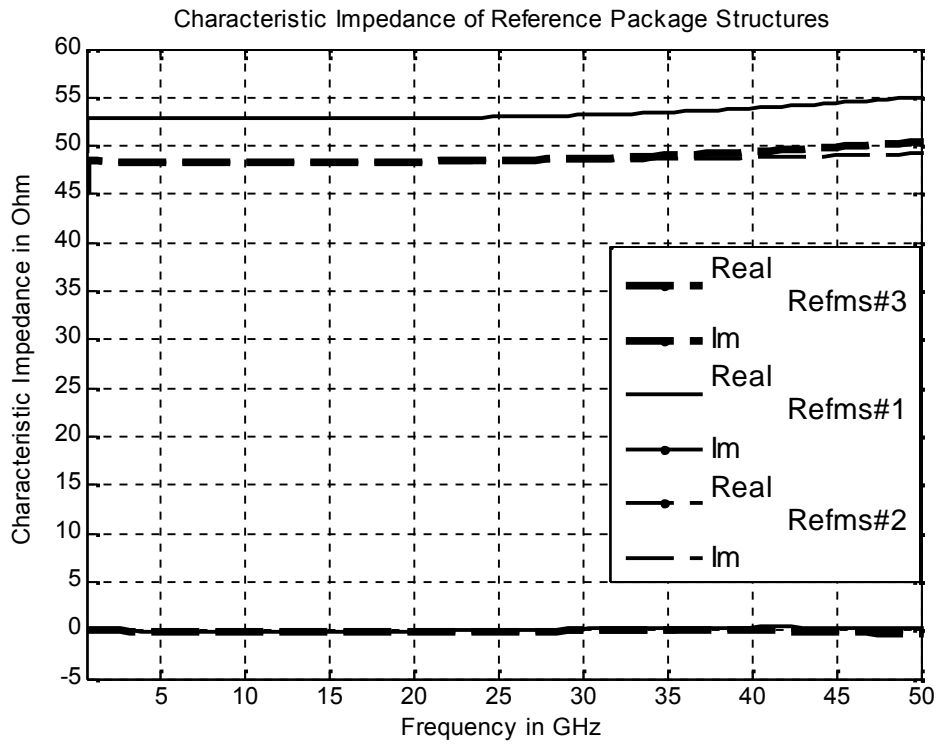


Figure (6): Characteristic impedances of single and multi-layers reference microstrip structures

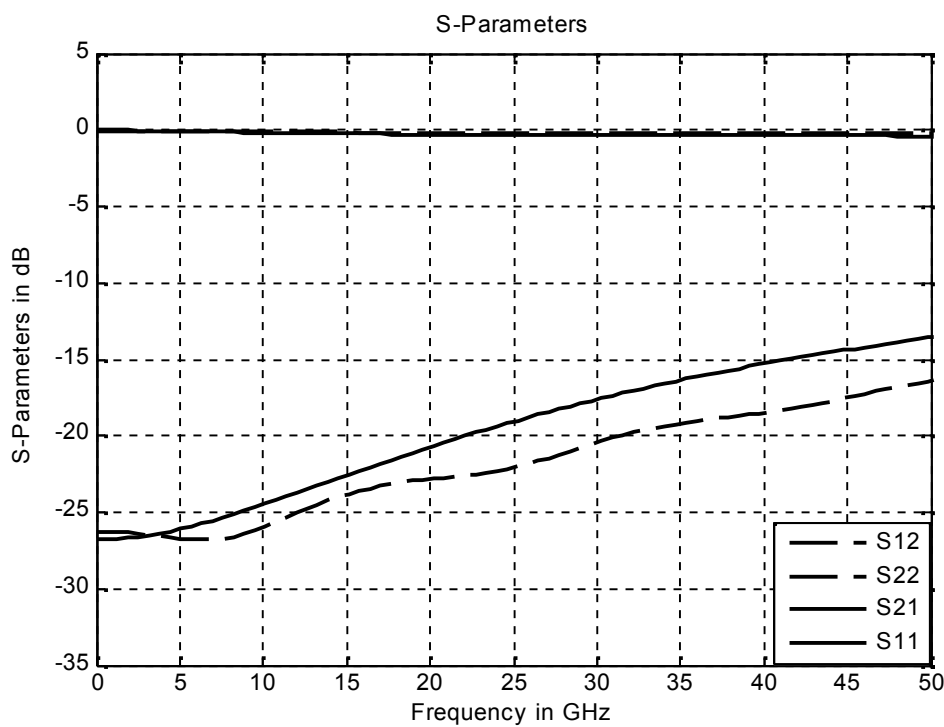


Figure (7-a): S-Parameters of single substrate MS-package Via transition

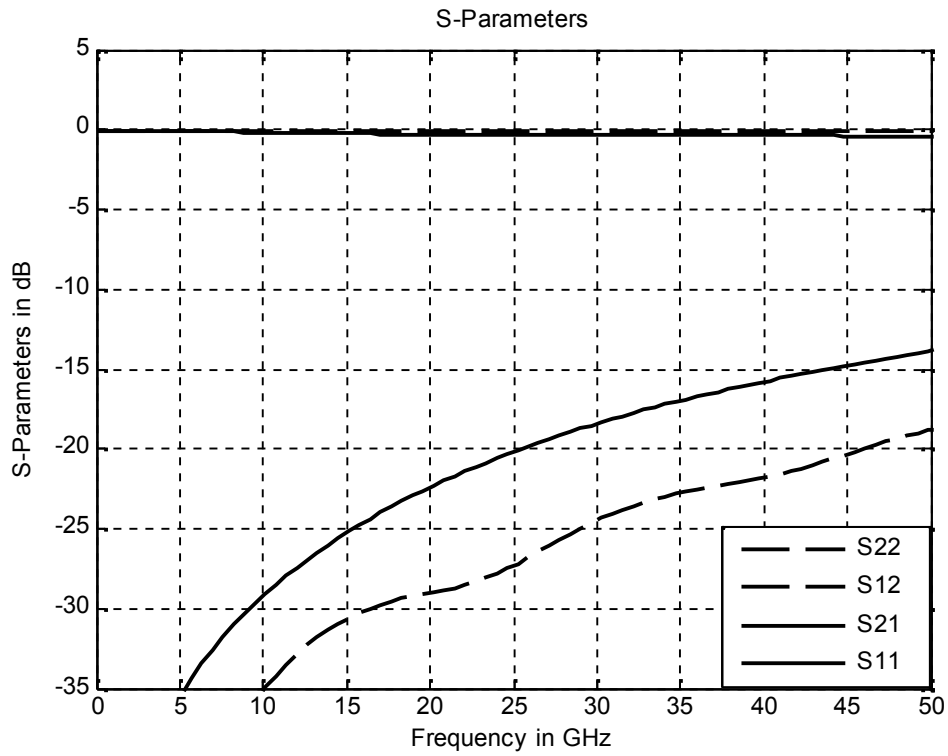


Figure (7-b): S-Parameters of Multi- substrates MS-package Via transition

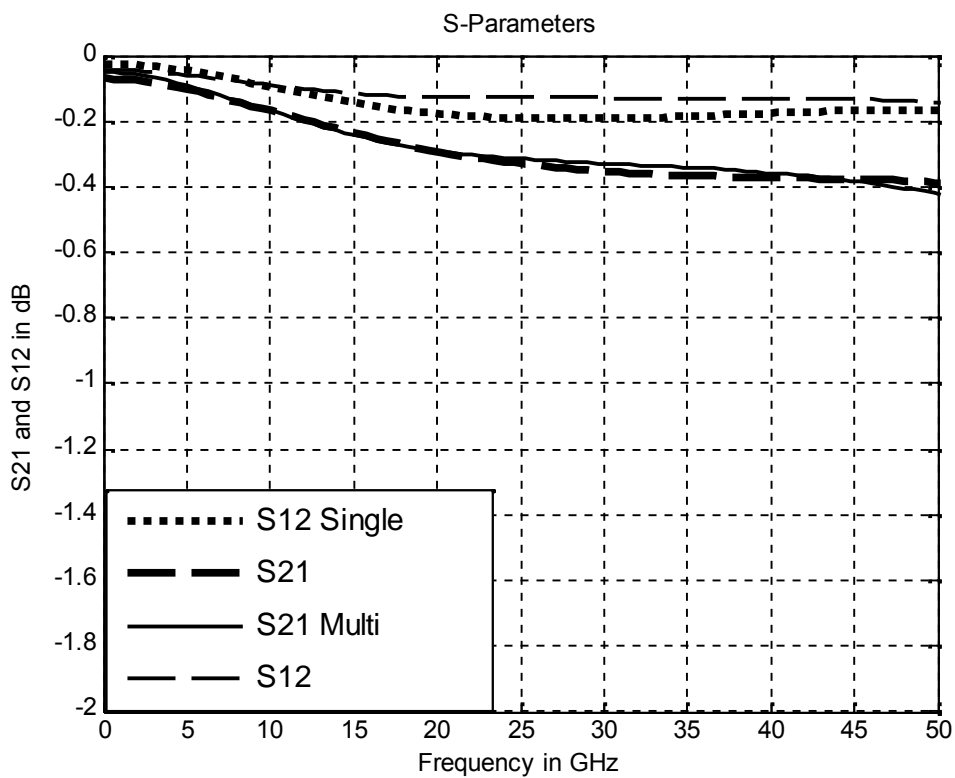


Figure (8): S21 and S12 of single and Multi- substrates MS-package Via transition

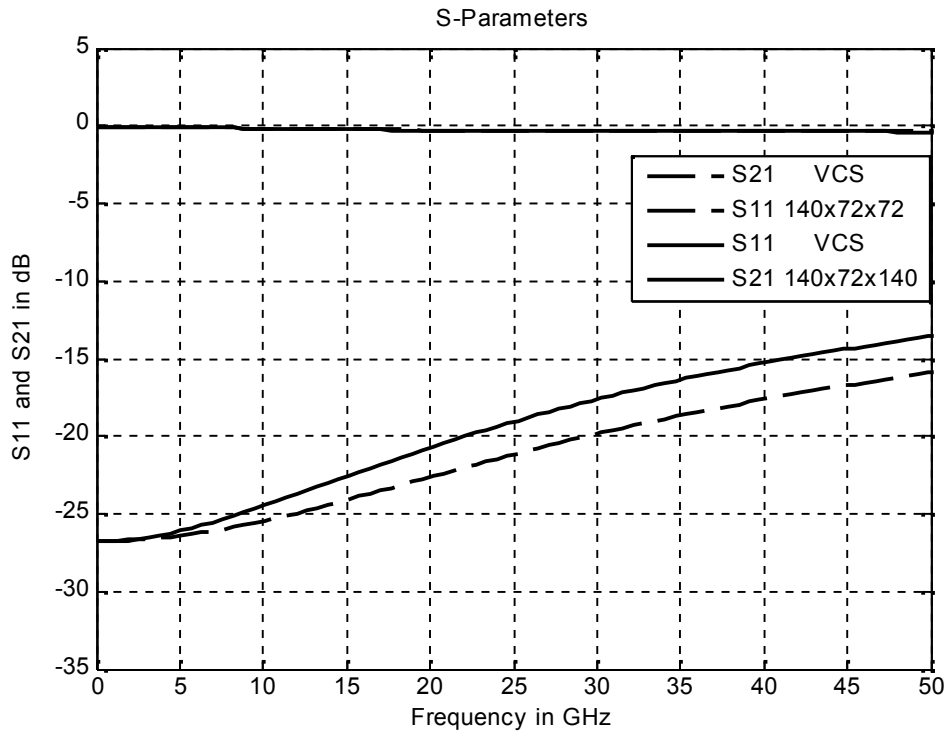


Figure (9-a): S-Parameters of single substrate MS-package Via transition for different Via cross-section

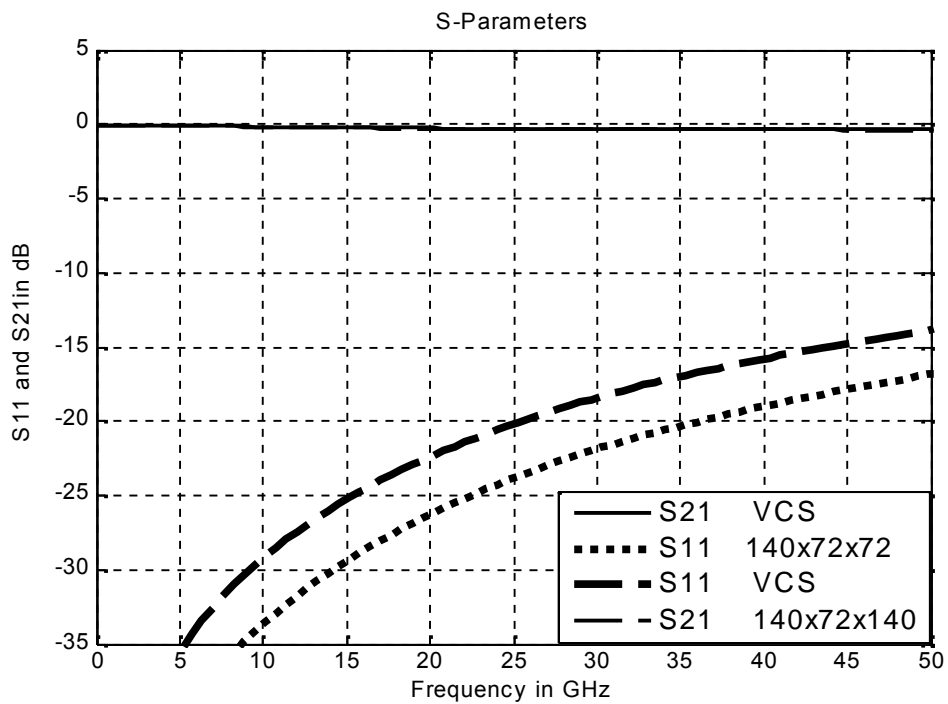


Figure (9-b): S-Parameters of multi-substrate MS-package Via transition for different Via cross-section

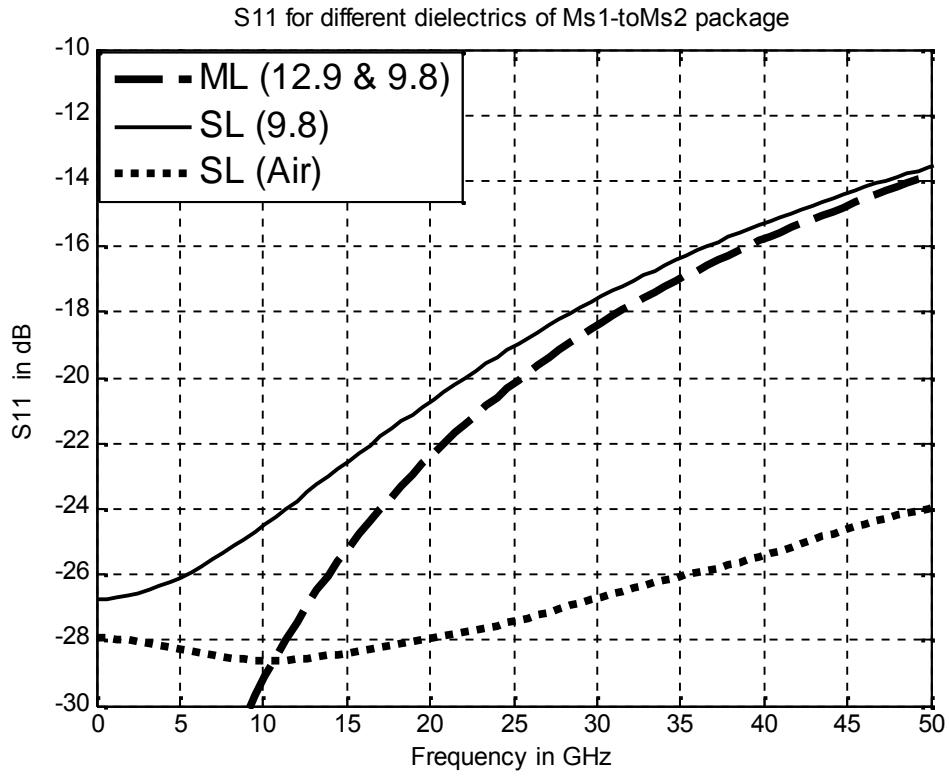


Figure (10): S11 of the Via transition for different dielectric constants of chip and motherboard