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# Finite-Difference Time-Domain Analysis and Design of Transition Interconnects in Coplanar-to-Microstrip Package

By

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## Abstract:

This paper presents analysis, investigation, and design of a new transition between CPW GaAs chip and Aluminum MS motherboard with single via interconnect and one common CPW-ground. Finite-Difference Time-Domain method "FDTD" is used as our computational electromagnetic technique. The FDTD Gaussian pulse responses of the package in presence and absence of interconnect characterized its electromagnetic features using the Fourier Transformation. In frequency domain, these responses give an accurate computation of the scattering parameters of the discontinuity over a wide band of frequencies. The main objective of this paper is to use these parameters to investigate and evaluate the overall package performance as function of substrate type of chip and motherboard as well as interconnect geometry. The interconnect geometry has a great impact on the overall package performance. Optimization of the package performance can be achieved by reconfiguring the interconnect geometry. Excellent S-parameters of the package have been obtained up to 30 GHz; S<sub>11</sub>/S<sub>22</sub> and S<sub>21</sub>/S<sub>12</sub> are of order -20 dB and - 0.4 dB respectively.

## <u>Keywords:</u>

High frequency interconnects in MMIC packages and finite-difference time-domain "FDTD"

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# 1. Introduction:

Planar transmission lines offer several advantages in MIC "Microwave Integrated Circuit" and MMIC "Monolithic Microwave Integrated Circuit" circuits' applications [1-2]. These advantages are the ease of parallel and series insertion of both passive and active components, the high circuit density, and low cost. Planar circuits include coplanar waveguide "CPW", microstrip "MS", and Stripline "SL". To transmit the signal between the chip and the motherboard, metallic interconnect "via holes/bumps" should be used. This results in partial loss, reflection and possibly distortion of the signal. In addition, coupling between multiple interconnections as well as signal lines is also form another main problem.

In this paper, a single via hole is used to connect the signal lines of CPW-chip and microstrip-motherboard in CPW-to-MS package with one common CPW-ground mounted on two different substrates. Finite-difference time-domain "FDTD" method is used to analyze and investigate the package performance. The objective is to study and minimize the effect of transition interconnect on the overall package performance. Reference coplanar and microstrip structures, explain next, are used in FDTD analysis to feed the CPW-to-MS package.

This paper is organized in four main sections. A brief discussion of the principles and concept of FDTD method is presented in section 2. Source excitation model, absorbing boundary conditions "ABC", FDTD non-uniform grids, frequency dependent parameters are also explained and presented in this section. FDTD simulation assumptions and Dimensions of package under investigation are presented in section 3. The S-parameters of CPW-to-MS and MS-to-CPW packages are computed, and they are also presented in section 3. Finally, section 4, concludes the present paper.

## 2. Theory

Finite-Difference Time-Domain method is one of most popular method used to analyze and model Non-closed form analytical solution of many electromagnetic problems [6-9]. This is carried out by solving the two Maxwell's curl equations for both electric and magnetic fields ( $\mathbf{E} \& \mathbf{H}$ ) within a specific domain as function of space and time as well as the constitutive parameters of problem under investigation. The main drawback of this method is the implementation of absorbing boundary condition (ABC) which used to terminate the computational domain [10-11]. This problem has been solved using the perfect matched layers (ABC-PML) [12]. The reader can refer to [13-15] for more details about FDTD method.

To apply the FDTD method to **CPW-MS** package shown in Fig.1, we should discuss the following:

- Source excitation model
- Reference microstrip structures
- FDTD simulation parameters
- Absorbing Boundary Condition
- Frequency Dependent parameters

**Source excitation model**: for many guided structures, in particular, most planar circuits, the exact field distributions are not well known in advance. In this case, a quasi-static TEM mode assumption may be used as an initial guess to excite a reference structure in order to get the spatial field distributions at source plane of package input. The choice of the reference structure depends on the geometry of the package under investigation. Thus, a finite length section of transmission line with the same cross section and dielectric layers as the package under investigation is used as a reference structure. In addition, the length of this reference structure should be long enough such that the dominate mode will be developed at its output. Therefore, a gaussain pulse is used to modulate these spatial distribution functions of field components at the source plane to excite the package as [8]:

$$\boldsymbol{E}_{x}(\boldsymbol{x},\boldsymbol{y},\boldsymbol{t}) = \boldsymbol{\varphi}_{x}(\boldsymbol{x},\boldsymbol{y},\boldsymbol{t}=\boldsymbol{t}_{o}) \exp\left[-\left(\boldsymbol{t}-\boldsymbol{t}_{o}\right)^{2}/\boldsymbol{T}^{2}\right]$$
(1)

$$E_{y}(x, y, t) = \varphi_{y}(x, y, t = t_{o}) \exp\left[-\left(t - t_{o}\right)^{2} / T^{2}\right]$$
(2)

Where,

$\varphi_x(x, y, t = t_o)$	The spatial distribution function of the transverse electric field				
	intensity $E_x(x, y, t=t_o)$ obtained from the air-reference structure				
$\varphi_{y}(x, y, t = t_{o})$	The spatial distribution function of the transverse electric field				
	intensity $E_y(x, y, t=t_o)$ obtained from the air-reference structure				
to	Time center of the Gaussian pulse				
Т	The Gaussian pulse width				

Equations (1) and (2), represent the source excitation of the CPW-to-MS package at its source plane (x-y plane).

**Reference microstrip structures:** in our FDTD analysis, four main planar lines are considered as reference structures. These are Refcpw<sub>1</sub>, Refcpw<sub>2</sub>, Refms<sub>1</sub>, and Refms<sub>2</sub> as shown in Fig. 2. The first coplanar line is a single substrate ( $_{r1}=_{r2}=9.8$  and  $W_1=240 \times 10^{-06}$  m, h=360x10<sup>-06</sup> m), and it has a characteristic impedance of order 50. The second coplanar line is multi-substrates ( $_{r1}=9.8$ ,  $_{r2}=12.9$ , and  $W_1=240 \times 10^{-06}$  m, h=360x10<sup>-06</sup> m), and it has a characteristic impedance of order 44. The first microstrip line is a single substrate ( $_{r2}=9.8$ ,  $W_2=144 \times 10^{-06}$  m, and h=360x10<sup>-06</sup> m), and it has a characteristic impedance of m), and it has a characteristic impedance of m).

( $_{r1}=9.8$ ,  $_{r2}=12.9$ , and  $W_2=144 \times 10^{-06}$  m, h=360x10<sup>-06</sup> m), and it has a characteristic impedance of order 48 . These reference structures are used to **extract the reflected fields** due to via interconnect from the incident fields at the package input port. To minimize effect of reflection loss due to the air-dielectric discontinuity on the lunched gaussain pulse in CPW-to-MS package, MS-to-CPW package, and the reference structures, two additional air-reference structures are considered. These are RefcpwAir and RefmsAir. They are used to excite the CPW-to-MS package, MS-to-CPW package, and the other reference microstrip lines (single and multi substrates).

**FDTD parameters:** dimensions of the assumed CPW-to-MS package under investigation are presented in table (1). This includes the widths of CPW and MS lines, the dielectric constant of substrate (single/multi), substrate heights and characteristic impedance. The designed FDTD simulation parameters are presented in Table (2). The three dimensions FDTD-mesh including uniform and non-uniform grids is shown in Fig.4. A second order non-uniform function which provides smooth transition from low dense mesh to high dense mesh is used as proposed by Ghouz, and reported in [8]. Furthermore, the ground and the strip conductors are assumed to be perfect conductors with zero thickness. Also, ideal substrates are considered (no dielectric loss). Due to the symmetry of the CPW-MS package, a perfect magnetic wall is used at the strip center. This reduces the required CPU-time and memory to execute our codes.

**Absorbing Boundary Condition:** in our FDTD simulation, a perfect matched layer is used to terminate the assumed computational domain. The number of matched layers NP=6, and the reflection coefficient is of order  $10^{-06}$ . The reader can refer to [12] for a details about ABC-PML.

**Frequency Dependent parameters:** frequency dependent parameters based on the time-domain response of the package are used to investigate and model the effects of the discontinuity on the overall package performance. The most important frequency parameter is scattering parameters (S-Parameters). Propagation constant  $\beta(\omega)$ , effective dielectric constant  $\varepsilon_{eff}(\omega)$ , and characteristic impedance  $Z_o(\omega)$  of the reference structures are also very important frequency parameters in modeling the discontinuity.

First, for a transmission line model of a via hole shown in Fig3, the modified S-parameters reported by Ghouz in [8] are given by:

$$S_{ij}(\omega) = \sqrt{\frac{V_i^-(z_i, \omega) \times I_i^-(z_i, \omega)}{V_j^+(z_j, \omega) \times I_j^+(z_j, \omega)}}$$
(3)

Where,

Vi	denotes the reflected voltage at the package port-i
$V_j^+$	denotes the incident voltage at the package port-j
$I_i^-$	denotes the reflected current at the package port-i

#### denotes the incident current at the package port-j

Second, the frequency parameters of the reference structures are [8]:

$$\beta(\boldsymbol{\omega}) = \frac{1}{\left(z_{j} - z_{i}\right)} \left\{ \phi_{i}(\boldsymbol{\omega}, z_{i}) - \phi_{j}(\boldsymbol{\omega}, z_{j}) \right\}$$
(4)

$$\varepsilon_{eff}(\omega) = \frac{\beta^2(\omega, z_i, z_j)}{\omega^2}$$
(5)

$$Z_{o}(\omega) = \frac{FT \left[ V_{in}^{ref}(z_{i},t) \right] e^{-j\omega\Delta t/2}}{\sqrt{FT \left[ I_{in}^{ref}(z_{i-1},t) \right] FT \left[ I_{in}^{ref}(z_{i},t) \right]}}$$
(6)

Where.

 $I_i^+$ 

denotes the phase of electric field of reference structure at the space  $_{i}(, Z_{i})$ location z<sub>i</sub>.

 $_{i}(, z_{j})$ denotes the phase of electric field of reference structure at the space location z<sub>i</sub>.

denotes the voltage of reference structure at the input port  $z_i$ .

denotes the current of reference structure at the input port  $z_i$ .

denotes the current of reference structure at the input port  $z_{i-1}$ .

#### 3. Simulation Results

In our FDTD simulation, three code types have been developed on MatLab to analyze and investigate the effects of discontinuity on the overall package performance. The first code type is used to simulate the CPW-to-MS -package shown in Fig.1. The second code type is used to simulate the reference CPW structures shown in Fig. (2-a). The third one is used to simulate the reference MS structures shown in Fig. (2-b). Each code is divided into two modules, FDTD-module and Frequency-module (FD-MD & FR-MD).

The FD-MD of first code computes gaussain pulse response of the (CPW-to-MS)/(MSto-CPW) package for different substrate types and via dimensions. The FD-MD of both second and third codes computes the gaussain responses of the reference structures corresponding to the CPW/MS transition package. The FR-M D of the package code uses gaussain response of both reference structures and the (CPW-to-MS)/(MS-to-CPW) package to compute the scattering parameters of the package over a wide frequency range up to 50 GHz (S-parameters defined in Eq.(3)). Effective dielectric constant, propagation constant and characteristic impedance of the reference structures are computed versus frequency using the FR-MD of the second and third codes (Eq.(4) through Eq.(6)). These parameters are compared with the analytical formulas of

coplanar and microstrip lines to verify our codes. Results of our simulation are presented in Fig.5 through Fig.10. Propagation constant and effective dielectric constant of the reference coplanar and microstrip structures versus frequency are illustrated in Fig.5. . It is clear that from the figures, effective dielectric constant and propagation constant are monotonic increasing function of frequency. The case of **air-substrate** is used to verify our codes. To minimize the effect of reflection loss due to mismatch between the signal lines in the package, characteristic impedances of coplanar and microstrip structures should be designed as 50 lines. These impedances are plotted versus frequency, and they are depicted in Fig.6. It is clear that from Fig. (6-a), excellent match between the line strips has been obtained in case of single substrate (CPW<sub>1</sub>& MS<sub>1</sub>). Good match between the signal lines is achieved in case of multi-substrates (CPW<sub>2</sub> & MS<sub>2</sub>) as shown in Fig. (6-b).

The S-parameters of the package are depicted in Fig.7. Good performance has been achieved up to 20 GHz. In addition, the package has better performance in case of multisubstrates than single-substrate at low microwave frequencies up to 5 GHz. This is due to the fact that substrate radiation loss decreases as the effective dielectric constant of the substrate increases (see Fig.5). On the other hand, as frequency increases, degradation of the package performance results due to mismatch between the signal lines (see Fig.6). The package performance is investigated for different gap width and via cross sections, and the S-parameters are presented in Fig. 8 and Fig.9 respectively. The smaller the cross section of via the better the package performance is achieved. Furthermore, the wider the gap width the lower the reflection due to the via. In case of single substrate, there exists an optimum value of the gap width where, minimum via reflection can be achieved at certain frequency range as it is clear from Fig.9.

The CPW-to-MS package performance can be controlled and greatly enhanced over a wide frequency band in case of either single or multiple substrates using two main parameters. These are via cross "CS" section and gap width "Gap". Fortunately, these via parameters are free from the fabrication constraints. The results of package performance optimization are depicted in Fig.10. It is clear that the package performance is greatly enhanced by about 13 to 6 dB up to 45 GHz. Therefore, the wider the width of the gap the less the mutual coupling between the signal line (via interconnect) and the ground is achieved.

# 4. Conclusion

Performance of a proposed CPW-to-MS transition with a single via interconnect and one common ground has been analyzed and investigated for different substrate types and interconnect dimensions using FDTD method. The CPW-to-MS package has two main configurations: single-substrate CPW-to-MS package and multi-substrates CPW-to-MS

package. The first configuration represents transition from CPW motherboard to MS motherboard and vice versa. On the other hand, the second package configuration represents transition from CPW-chip to MS-motherboard. In these package configurations, no need to use ground interconnects which in turn eliminate coupling between signal and ground interconnects. Based on the simulation results, the smaller the via's dimensions the lower the via's reflection. However, the via's height as well as the line widths is controlled by the fabrication process and the matching conditions. Furthermore, the via's cross section and the ground gap width have a great impact on the package performance. To optimize the package performance, the gap width is of order is one strip width " $W_{min}$ ", and the via's cross section is about ( $W_{min} X W_{min}/5$ ), where,  $W_{min}$  is the smallest line width of either CPW or MS line. It has been reported by Ghouz in [8], a circuit model of transition interconnect can be developed using the obtained S-parameters over a wide frequency band. This greatly simplifies the analysis of complex package. Future work will include analysis and investigation of transition interconnects in Coplanar-to-Stripline package for single and multi-layers substrate.

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(c) Top View Section

*Figure (1):* Single Via transition interconnect between CPW GaAs chip and MS Aluminum motherboard



Figure (3): Transmission line model of Via transition



Figure (4): The 3-D FDTD mesh of CPW-to-MS package

Line	Slot	Via/Sub.	Gap	Dielectric	Dielectric	Z <sub>oi</sub>
Widths	Width	heights	Width	Constant	Constant	in
in	in	in	in	# 1	#2	Ohm
micron	micron	micron	micron	CPW/MS	CPW/MS	CPW/MS
						Z <sub>AV1</sub> =50
240/288	120	180/360	120	9.8	-	Z <sub>AV3</sub> =52
						Z <sub>AV1</sub> =45
240/288	120	180/360	120	12.9	9.8	Z <sub>AV3</sub> =48

Table (1): Parameters dimensions of CPW-to-MS package and reference structures

Table (2): FDTD simulation parameters

Space Parameters	Gaussian pulse Parameters	FDTD Meshing Parameters				
$D_{xo} = 0.012mm$	$\Delta t = \text{time step} = 2.3094 \text{x} 10^{-14}$	Non-uniform in x-direction with $L_x = 1.12 \text{ mm}$ Fig.3-a				
$D_{yo} = 0.012 mm$	$t_o=T/2 \approx 1800$ time steps = 4.1569x10 <sup>-11</sup> Pulse center	Non-uniform in y-direction with $L_y = 1.5 \text{ mm}$ Fig.3-b				
$D_{zo} = 0.012mm$	F <sub>max</sub> ≈50 GHz	Non-uniform in z-direction with $L_z = 3.0 \text{ mm}$ Fig.3-c				
$D_{max} = _{min} / 40 = 0.15 mm$						
The required time steps to get the output pulse at the CPW-to-MS package's output is about 8000 time steps						
FDTD Computational Domain cells $= 80 \times 40 \times 106$						



Figure (5-a): Propagation Constants of reference microstrip and coplanar structures



Figure (5-b): Effective dielectric constants of reference microstrip and coplanar structures





Figure (6-a): Characteristic impedance of reference microstrip and coplanar structures



Figure (6-b): Characteristic impedance of reference microstrip and coplanar structures



**S-Parameters** 

Figure (7-a): S-parameters of single Via in CPW-to-MS package on single substrate



Figure (7-b): S-parameters of single Via in CPW-to-MS package on multi-substrates





*Figure (8-a):* S-parameters of CPW-to-MS package on single substrate for different via cross-sections  $"CS_3 < CS_2 < CS_1"$ 



*Figure (8-b):* S-parameters of MS-to-CPW package on single substrates for different Via cross-sections  $"CS_3 < CS_2 < CS_1"$ 



*Figure (9-a):* S-parameters of CPW-to-MS package on single substrate for different Gap " $Gap_1 < Gap_2 < Gap_3$ "



Figure (9-b):S-parameters of MS-to-CPW package on single substrate for different Gap





*Figure (10-a):* S-parameters of CPW-to-MS package on multi substrates for  $Gap_2 = 0.18$  mm and  $CS_3 = 0.24 \times 0.048 \text{ mm}^2$ 



**Figure** (10-b): S-parameters of CPW-to-MS package on multi-substrates for  $Gap_3 = 0.24 \text{ mm}$  and  $CS_3 = 0.24 \text{ x} 0.048 \text{ mm}^2$