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# Low Power Current-Mode Threshold Logic Gate Using Nano-Technology Double-Gate MOSFETs

*By*

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***Abstract:***

This paper presents a new low voltage low power current mode threshold logic (CMTL) circuits using DGMOSFETs. The ultimate feature of the double gate transistor is using the top and bottom gates in the design of the logic circuits that reduces the number of the transistors. The total number of the transistors required to implement the CMTL circuits and the power dissipation is almost reduced by half by using the DGMOSFET. OR, AND, MAJ logic gates are designed using DGMOSFETs and simulated using HSPICE. The results for the proposed 45 nm DGMOSFET logic circuits with 1 V supply voltage show low power dissipation, smaller power delay product and less number of device.

***Keywords:***

DGMOSFET Circuits, Low Power Circuits, Threshold Logic Gate.

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## ***1. Introduction:***

The demand for high density, low power consumption, high-speed and low cost of the logic circuits requires aggressive scaling of the CMOS transistors. as the CMOS scaling is approaching the limit imposed by gate oxide tunneling, double-gate MOSFET (DGMOSFET) is becoming the promising candidate to replace CMOS technology. The advantages introduced by DGMOSFET are excellent scalability, naturally steep subthreshold slope, near-ideal subthreshold slope, high drive current and transconductance, and low subthreshold intrinsic capacitance [1-2]. Threshold Logic (TL) as a powerful alternative to traditional AND,OR,NAND logic gates was introduced over four decades ago. It capable of realizising complex Boolean function with a smaller number of logic gate than the traditional logic gate based design [1]. Recently many of threshold logic gate circuits have been proposed [2]-[5]. Such as capacitive threshold logic [2], differential current-switch threshold logic [3], single electron tunneling [4], and resonant tunneling diodes [5].

The output of a linear TL is given by:

$$f(X) = 1 \Leftrightarrow \sum_{i=1}^{n} w_i X_i \geq T \quad (1)$$

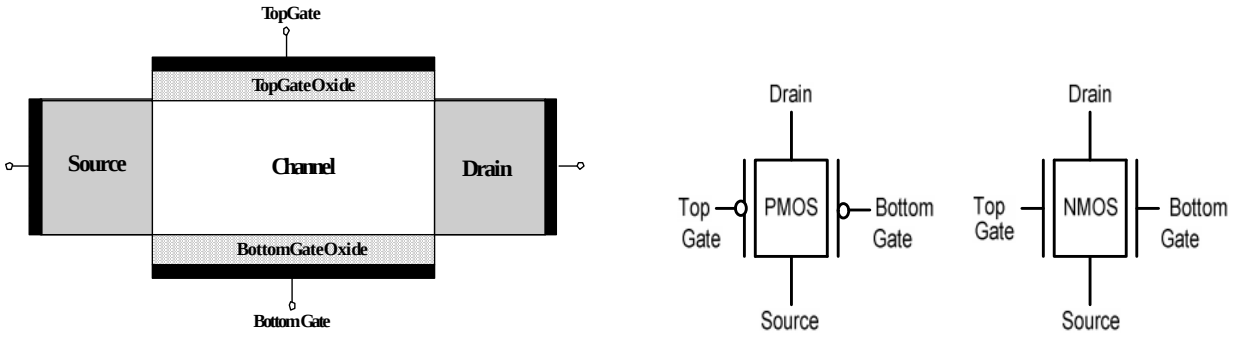
$$f(X) = 0 \Leftrightarrow Otherwise \quad (2)$$

where the inputs are X1, X2,…., Xn,, and each input having a weight of w1, w2,….., wn respectively.

In this paper we proposed new threshold logic gate circuits based on nanoscale DGMOSFET device. The two gates for DG device provide the TL circuits based on nanoscale DGMOSFET device advantages over other circuits, such as: 1) Suitable for high fan-in gate implementation. 2) Low power dissipation. 3) Reduce the number of transistors, so reduce area/size of the chip.

## ***2. DGMOSFET DEVICE FEATURES:***

DGMOSFET is well recognized as the most promising candidate to extend the scaling limits for classical COMS technologies beyond 45-nm technology node [8]. The two gates of DG device provide effective control of short-channel effects without aggressively scaling down the gate-oxide thickness and increasing the channel doping density [9].The DGMOSFET device can be employed either with two gates tied together or independently driven [8]. It can also be exploited to reduce the number of transistors for implementing logic functions [9]. DGMOSFET schematic circuit diagram and symbols are shown in Fig. 1.



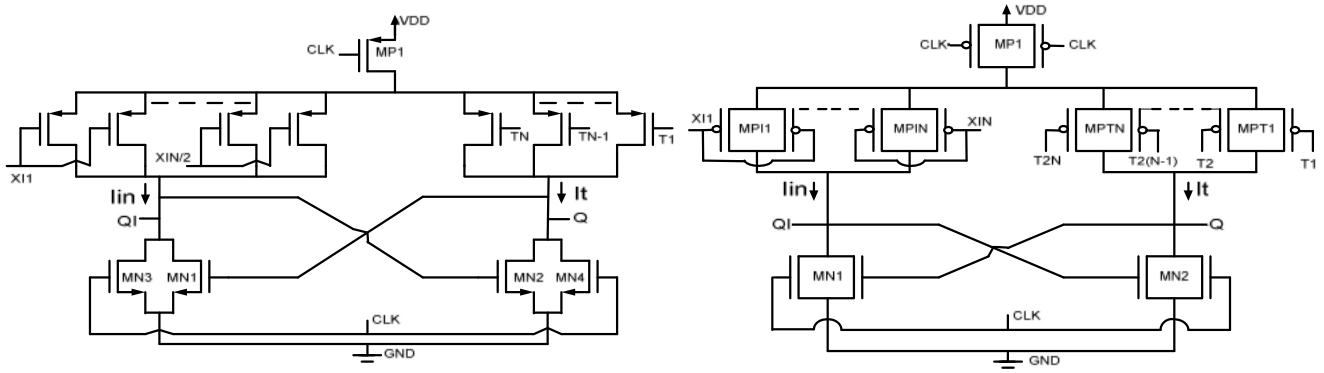

(a) (b)

Fig.1. (a) Schematic circuit diagram of DGMOSFET.
(b) DGMOSFET circuit symbols.

## 3. PROPOSED DGMOSFET TLG:

Fig. 2a shows the discharge current mode threshold logic (DCMTL) gate using CMOS technology [10]. A set of PMOS transistors are used for the inputs, and an identical set of PMOS transistors are used for the threshold. Transistors MN1 and MN2 form cross coupled half latch structure that translates the current difference into voltage swing at node Q and QI. MN3 and MN4 are discharged transistors. The transistor MP1 is used to eliminate the static power dissipation in equalize phase. The basic operation of this circuit can be explained as follows: the current (Iin) through input PMOS transistors (input set) are controlled by the input voltage. Also, the current (It) through the threshold transistors is controlled by the threshold voltage. When the CLK is high the transistor MP1 is turned off and the transistors MN3 and MN4 are turned ON and the nodes Q and QI are discharged to GND. When the CLK goes Low, transistor MP1 turns on raising the source node voltage of both input/threshold set of PMOS transistors. In the same time, the transistors MN3 and MN4 are turned off and the circuit begins evaluation. So, if the threshold current (It) is greater than the input current (Iin), then the node voltage Q begins

to rise faster than the node voltage at QI. Hence, the output node Q is driven high and QI is driven low. Fig. 2b shows the implementation of DCMTL circuit (shown Fig.2a) using double gate MOSFET transistors. We use the advantage of two gates of DGMOSFET to reduce the number of transistors used. So, we reduce the number of transistors by almost half. As an example in the conventional CMOS design, we need 37 transistors to build 8-input threshold logic circuit while we need only 19 transistors to build the same circuit using DGMOSFET. This means we save a lot of area and power dissipation. An improved circuit called equalized current mode threshold logic (ECMTL) gate proposed in [10] using CMOS technology is shown in Fig. 3a, and our implementation using DGMOSFETs is shown in Fig. 3b. The circuit has a set of DGPMOS transistors [MPI1-MPIN], and an identical set of transistors [MPT1-MPTN] that used for threshold. By using latch structure formed by back-back connected inverters (MP1/MN1 and MP2/MN2) the power dissipation problems in evaluate phase can be avoided. Transistors MN3 and MN4 are turned on, in equalized phase (when CLK goes high), so the output nodes Q, QI and the drain nodes of input/threshold set of PMOS transistors are equalized. When the CLK goes low, MP3 turns on raising the source node voltage of both input/ threshold set of transistors, in the same time the transistors MN3 and MN4 are turned off, and the circuit begins to evaluate.




(a) (b)

Fig.2. (a) DCMTL proposed in [6]. (b) DCMTL implemented using DGMOSFETs.

## IV. LOGIC GATES REALIZATION USING DGECMTL

### A. OR Gate Realization

To realiz OR/NOR gate, the top and bottom gates of each DG-PMOS input transistor are tied together to become one of the logic gate inputs. So, for N number of DG-PMOS transistors we have 2N gates and N input logic gate. For threshold set, we connected (2N-1) of the gates to GND (low voltage), and only one gate to VDD (high voltage). The current through DG-PMOS transistor with the gate terminal at a higher voltage is smaller than the current through DG-PMOS transistor with the gate terminal at GND.

So, if at least one of the inputs to the OR gate is high, then there two gates from input set connected to VDD while only one gate from threshold set connected to $V_{DD}$. This means the current (It) through the threshold transistors is greater than the current (Iin) through input DG-PMOS transistors set. Hence, the output node Q is driven high (OR gate) and the output node QI is low (NOR gate). In case of all inputs to the OR gate are Low, the current (Iin) through input PMOS transistors set is greater than the current (It) through the threshold transistors. Hence the output node Q is driven low (OR gate) and the output node QI is high (NOR gate).

### B. AND Gate Realization

To realiz AND/NAND gate, the top and bottom gates of each DG-PMOS input transistor are tied together to became one of the logic gate inputs. For threshold set, we connected (2N-1) of the gates to VDD (high), and only one gate to GND (low). So, if at least one of the inputs to the AND gate is low, then there two gates from input set connected to GND while only one gate from threshold set connected to GND. This means the current (Iin) through input DG-PMOS transistor sets is greater than the current (It) through the threshold transistors. Hence, the output node Q is driven low (AND gate) and the output node QI is high (NAND gate). In case of all inputs to the AND gate are high, the current (It) through the threshold transistors is greater than the current (Iin) through input PMOS transistors set. Hence, the output node Q is driven high (AND gate) and the output node QI is low (NAND gate).

### C. MAJ. Gate Realization

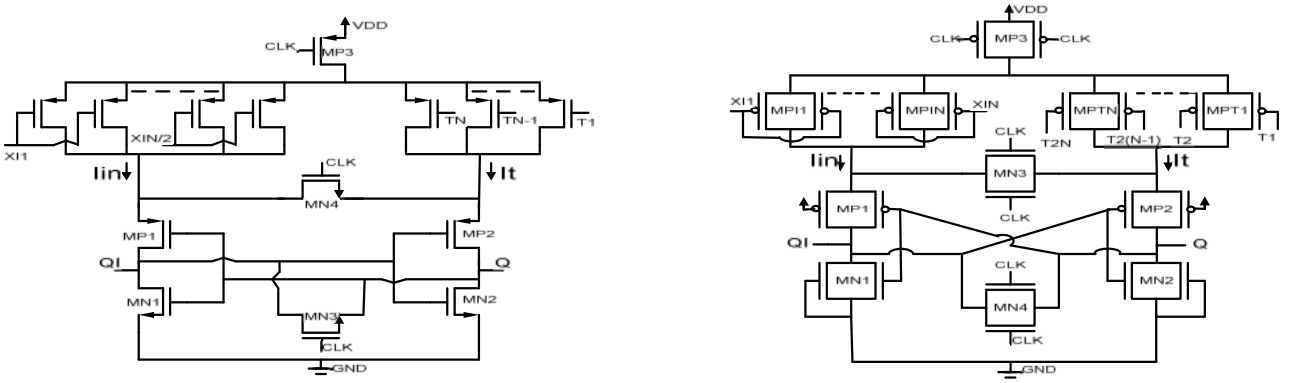
To realiz majority/minority gate, the top and bottom gates of each DG-PMOS input transistor are tied together to become one of the logic gate inputs. For threshold set, we connected (N-1) of the gates to VDD (high), and (N +1) of the gates to GND (low). So, if at least (N/2) of the inputs to the majority gate are high, then the current (It) through the threshold transistors is greater than the current (Iin) through input DG-PMOS transistor sets. Hence, the output node Q is driven high (MAJ gate) and the output node QI is low (MIN gate). In case of all inputs to the majority gate are low, the current (Iin) through input PMOS transistor sets is greater than the current (It) through the threshold transistors. Hence, the output node Q is driven low (MAJ gate) and the output node QI is high (MIN gate).

## 5. NEW PROPOSED DG-ECMTL CIRCUIT

To save more area, and reduce the power dissipation, we proposed the new DG-ECMTL circuit is shown in Fig. 4. This circuit is a variant of the circuit in Fig. 3b in which we use the DGMOSFET as independent gate driven for input transistor sets (we do not tied the two gates together). So, if we use N of DGMOSFET for input transistor sets, then

we have 2N of inputs logic gate. For example, to build any 8 inputs logic gate using the circuit in Fig. 3b, we need 8 DGMOSFET for input transistor sets and the same number for threshold set (16 DGMOSFETs) but in case of the new circuit, we need 4 DGMOFETs for input transistors set and 4 DGMOSFETs for threshold set. But to ensure correct operation when the number of inputs at the high/Low value equals the number of threshold transistors at the high/ Low, we add extra transistor with half of normal input transistor size as shown in Fig. 4. So, we need only 10 transistors instead of 16.

## 6. LOGIC GATES REALIZATION USING A NEW DGECMTL




(a) (b)

Fig.3. (a) ECMTL proposed in [6]. (b) ECMTL implemented using DGMOSFETs.

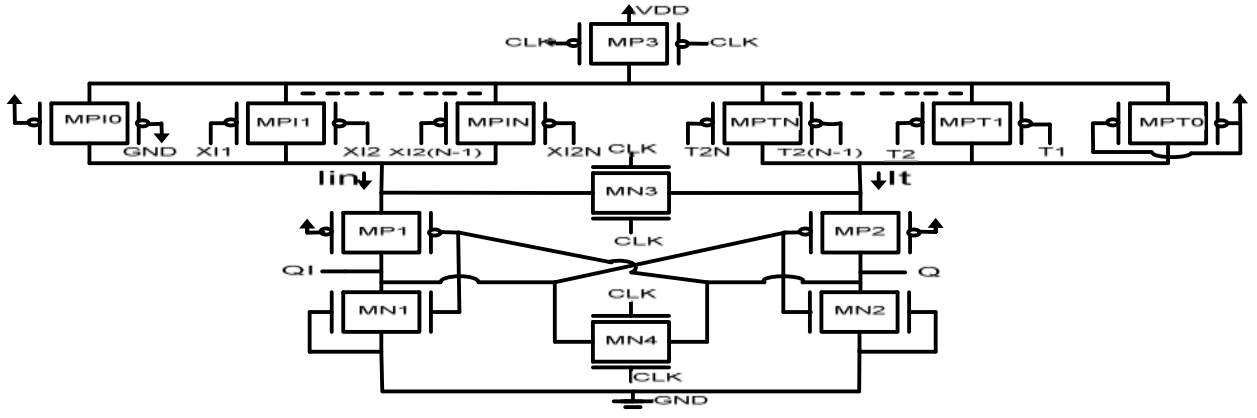



Fig.4. Proposed a new DGECMTL gate

### A . OR Gate Realization

To realiz OR/NOR gate, for threshold transistor sets we connected (2N) of the gates to GND (low voltage). The current through DGPMOS transistor with the gate terminal at a higher voltage is smaller than the current through DG-PMOS transistor with the gate

terminal at GND. So, if at least one of the inputs to the OR gate is high, then there is one gate from input set connected to $V_{DD}$ while there is no any gate from threshold set connected to VDD. This means of normal input transistor size as shown in Fig.4. So we need only 10 transistors insited of 16 the current (It) through the threshold transistors is greater than the current (Iin) through input PMOS transistors set. Hence, the output node Q is driven high (OR gate) and the output node QI is low (NOR gate). In case of all inputs to the OR gate are Low, the current (Iin) through input PMOS transistor sets is greater than the current (It) through the threshold transistors (greater by the extra half transistor (MPI0)). Hence, the output node Q is driven low (OR gate) and the output node QI is high (NOR gate).

**B. AND Gate Realization**

To realiz AND/NAND gate, for threshold set, we connected (2N-1) of the gates to VDD (high voltage), and only one gate to GND (low voltage). So, if at least one of the inputs to the AND gate is low, then there is one gate from input set connected to GND, and one gate from threshold set connected to GND. This means the current (Iin) through input PMOS transistors set is greater than the current (It) through the threshold transistors (greater by the extra half transistor (MPI0)). Hence, the output node Q is driven low (AND gate) and the output node QI is high (NAND gate). In case of all inputs to the AND gate are high, the current (It) through the threshold transistors is greater than the current (Iin) through input PMOS transistor sets. Hence, the output node Q is driven high (AND gate) and the output node QI is low (NAND gate).

**C. MAJ. Gate Realization**

To realiz majority/minority gate, for threshold set, we connected (N-1) of the gates to VDD, and (N +1)of the gates to GND. So, if at least N (half of the inputs) of the inputs to the majority gate are high, then the current (It) through the threshold transistors is greater than the current (Iin) through input PMOS transistor sets. Hence, the output node Q is driven high (MAJ gate) and the output node QI is low (MIN gate). In case of (N-1) inputs to the majority gate are high, the current (Iin) through input PMOS transistor sets is greater than the current (It) through the threshold transistors (greater by the extra half transistor (MPI0)). Hence, the output node Q is driven low (MAJ gate) and the output node QI is high (MIN gate).

## 7. SIMULATION RESULTS

To ensure correct operation and performance of the proposed DG-CMTL gate circuits, we have build a 8-inputs threshold gate and simulated using HSPICE program. The parameters for 45-nm DGMOSFET are shown in table I [11]. The supply voltage is 1V, The load capacitance at output node is 10 fF, and the clock frequency is 100 MHz. The simulation results for DG-ECMTL shown in Fig. 3b is illustrated in Fig. 5, and the simulation results for the proposed DG-ECMTL shown in Fig. 4 is illustrated in Fig. 6. The results indicate a proper operation of the logic gates with the proposed

DGMOSFET with less number of transistors. Fig. 7 shows the realization of the logic gates with different inputs. It is also indicate a correct operation of the proposed DGMOSFET logic gates.

Table II summarizes the simulated characteristics of the two DG-ECMTL gates. It shows that the proposed circuit shown in Fig. 4 has lower power dissipation, smaller power delay product and less number of device than the proposed circuit shown in Fig. 3. As power dissipation comparison between the logic gates, OR has a largest power dissipation.

**Table I. Transistors sizes (L=45-nm for all transistors)**

| | **Fig.3b w(nm)** | **Fig.4 w(nm)** |
|---|---|---|
| **MPI1- MPIN MPT1-MPTN** | **180** | **180** |
| **MPI0,MPT0** | **-** | **90** |
| **MP1-MP3** | **960** | **480** |
| **MN1-MN3** | **480** | **240** |

**Fig.5. Simulation result of DGECMTL(Fig.3b)**

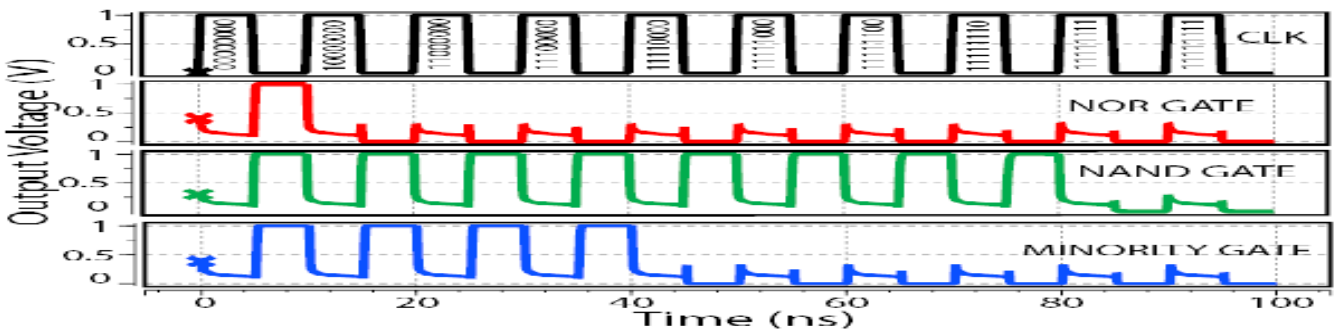


**Fig.6. Simulation result of Proposed DGECMTL(Fig.4)**

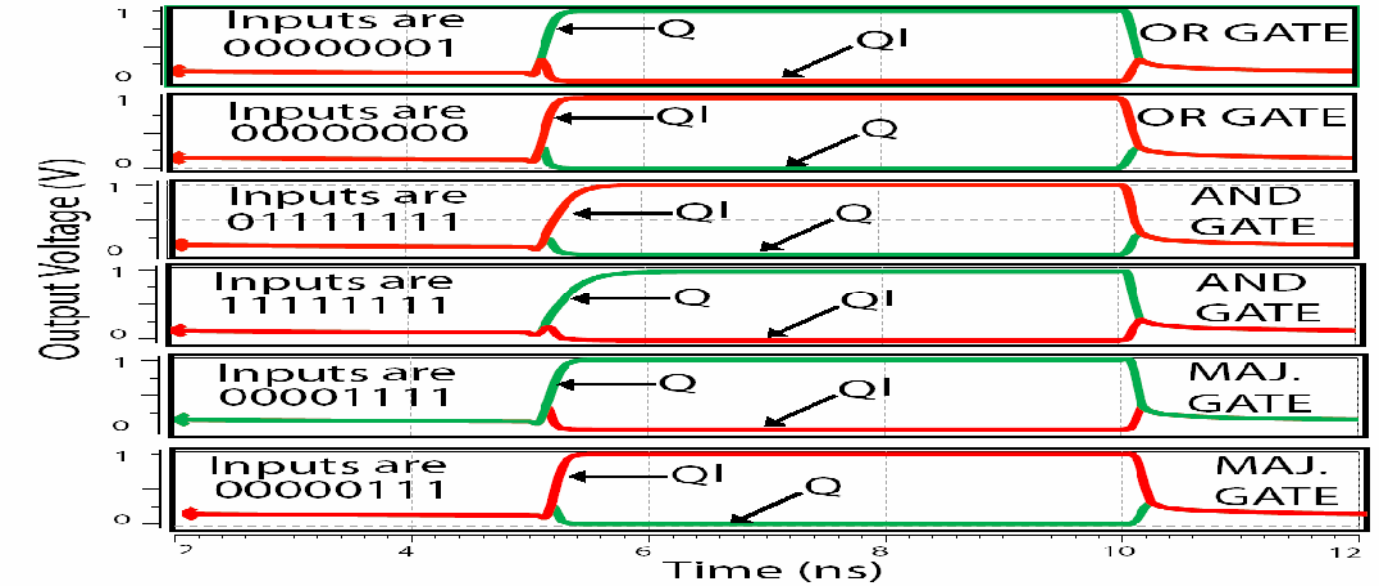



**Fig.7. Logic gates Realization simulations.**

## 8. CONCLUSION

In this paper, novel Current mode threshold logic gate circuits based on 45-nm DGMOSFET transistor are proposed, the two gates of DGMOSFET provided reduction in the number of transistors (almost to half ) that required to built TLG circuit. So reduction in the total area and the power dissipation. We have been realized and simulated many logic functions such as OR, AND, MAJ., NOR, NAND, and MIN, using proposed DGCMTL. HSPICE simulation results show good over all performances with single supply voltage 1V.

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**Table II. (8-input) DGCMTL gates simulated characteristics**

| Logic Gate | Proposed DGECMTL in Fig.3b | | | | Proposed DGECMTL in Fig.4 | | | |
|---|---|---|---|---|---|---|---|---|
| | PD (µW) | Delay (pS) | Power*Delay (fJ) | Device Count | PD (µW) | Delay (pS) | Power*Delay (fJ) | Device Count |
| OR | 3.78 | 224 | 0.846 | 2n+7 (23) | 2.73 | 260 | 0.709 | 2([n/2]+1)+7 (17) |
| AND | 2.5 | 520 | 1.3 | | 2.3 | 460 | 1.058 | |
| MAJ | 3.54 | 230 | 0.814 | | 2.6 | 290 | 0.754 | |

n is number of logic gate inputs. If n=8, then the device count will be 23 for Fig.3b, and 17 for Fig.4.