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HARDWARE REALIZATION OF DIGITAL WAVES USING ORTHOGONAL FUNCTIONS

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ABSTRACT

Different kinds of functions are required for today's Electronics and Communication applications with very precise characteristics like frequency, phase, magnitude and waveform etc. A technique for Field Programmable Gate Array (FPGA) based hardware realization has been developed for the design, implementation and prototyping of useful functions in digital form. The technique makes use of the orthogonal functions like Rademacher and the Walsh functions for the hardware realization. The FPGA based hardware realization of sinusoidal, triangular, and trapezoidal waveforms in their digital form has been demonstrated with good results. A comparative study of hardware realization of such functions targeted to various FPGAs available from Xilinx has been made. It is concluded that virtually any periodic function may be realized directly in its digital form (without the need of Analog to Digital conversion) with the help of FPGAs using orthogonal functions.

KEY WORDS

Walsh functions, Rademacher functions, Hardware realization, Field Programmable Gate Array (FPGA)

INTRODUCTION

Due to the recent advancement in Field Programmable Gate Arrays (FPGAs) over the past decade or so, the logic capacity of FPGAs has been enhanced, the performance greatly improved and price has been drastically reduced. Today, FPGAs are large and fast enough for use in multimillion-gate designs running at hundreds of megahertz. FPGAs now exceed the capacity and speed requirements of the vast majority of ASICs [1-2]. Thus FPGAs are becoming more attractive in a wide range of applications [3].

Different kinds of functions are required for today's Electronics and Communication applications with very precise characteristics like frequency, phase, magnitude and waveform etc. It has been demonstrated that, in principle, any periodic function may be realized using orthogonal functions [4].

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Many orthogonal functions and polynomials are being utilized for quite some time for scientific and engineering applications. These functions include trigonometric functions, Bessel functions, Hermite polynomials, Legendre polynomials etc. However, trigonometric functions which are inherently encountered in Fourier analysis have played a significant role in applications to engineering and science problems [5].

The selection and use of any orthogonal set of functions hinges primarily on the type of problem under study. For instance, while some sets render rather simple and useful solutions to a certain problem, other sets give complicated and less useful forms of solution. As an example, the discrete Karhunen-Loéve (KL) expansion technique may result in an efficient representation for discrete time random processes, but the implementation of the technique is usually very difficult. On the other hand, Walsh functions analysis may prove more advantageous from such points of view as multiplication and implementation of such processes [5].

The most important factor responsible for the increased use of Walsh functions is their digital nature. As the Walsh transform matrix is purely real, with entries {-1, 1}, fast operations require fewer operations than the comparable Fast Fourier transform (FFT). This in turn implies saving in processing time and storage allocations when using a digital computer as the signal processor. This advantage is particularly important to researches with limited facilities, a condition which is not uncommon to colleges and small-scale industries.

The rest of the paper is organized as follows. In the next section we discuss the definition and basic properties of Rademacher and Walsh functions. The Walsh series expansion is then formulated and discussed briefly. We then describe the technique for the successful generation of sinusoidal, triangular and trapezoidal digital waves using Walsh Functions. A comparison is made at the end using different Xilinx FPGA families. Finally we end the paper with some concluding remarks.

RADEMACHER AND WALSH FUNCTIONS

Fourier theory has been widely used in applications to science and engineering problems. In particular, Fourier analysis is well established in the engineering sciences as a means for analog wave analysis where the sine-cosine system of function finds ample opportunities for use. With the advent of digital computers and the introduction of their use in various fields, the theory of discrete (trigonometric) Fourier analysis has been developed. However, it is found that other theories can offer equal and sometimes better means of analysis. One such theory is based on a set of functions due to Walsh [5].

There have been many ways of defining or generating Walsh functions. In general, these investigations have been motivated by either of two purposes. The first purpose seeks a simple and efficient method of generating Walsh functions, and employing them for computational purposes particularly in using digital computers. The second purpose is to induce a definition which allows for simple and useful analytical or mathematical manipulations. It is easier to generate Walsh functions using the Rademacher functions [5]. A Rademacher function of the n^{th} order is defined as [5]:

$$\phi(n+1,x) = \text{Sgn}(\sin 2\pi 2^n x), \qquad n = 0,1,2,..., \qquad 0 \le x < 1$$
(1)

where, $\phi(0, x) = 1$ and the signum function Sgn(y) is defined by:

$$\operatorname{Sgn}(y) = \begin{cases} +1, & y \ge 0\\ -1, & y < 0 \end{cases}$$
(2)

The definition of Rademacher functions may be extended over the whole non-negative real line by the periodicity property [5]:

$$\phi(0, x+1) = \phi(0, x) \tag{3}$$

The Walsh functions may be derived as [5]:

$$\psi(0,x) = 1$$
 $0 \le x < 1$ (4)

and

$$\psi(n,x) = \prod_{i=0}^{N} \left[\phi(i+1,x) \right]^{n_i}, \qquad n_i \in \{0,1\}$$
(5)

where, $\psi(n,x)$ is the set of Walsh functions defined on [0,1) and the integer *n* is assumed to have the dyadic (binary) representation given as:

$$n = \sum_{i=0}^{N} 2^{i} n_{i} \tag{6}$$

Such a representation is imperative in considering the basic characteristics of Walsh functions. However, since the Rademacher functions are periodic outside the unit interval [0,1), it follows that Walsh functions are also periodic with the same unity period. Walsh functions are also taken right-continuous [5]. Fig. 1 depicts the first eight Walsh functions defined on the unit interval [0,1).

WALSH SERIES EXPANSION

Due to the completeness of Walsh functions, it is possible to formulate Walsh series expansion for suitable functions of periodic characteristics. The convergence aspect of this problem was studied originally by Walsh [5]. If f(x) is Lebesgue-integrable on [1,0), then it possesses an associated Walsh series expansion representation given by [5].

$$f(x) \approx A_0 \psi(0, x) + A_1 \psi(1, x) + A_2 \psi(2, x) + \dots$$
(7)

The expansion coefficients A_n are evaluated by:

$$A_n = \int_0^1 f(x)\psi(n,x)dx$$
(8)



Fig.1. First Eight Walsh functions

The use of Walsh series generally serves either of the two purposes:

- 1. Represent a function f(x) defined on a finite interval, for that interval.
- 2. Represent a periodic function f(x) for all values of x.

GENERATION OF DIGITAL FUNCTIONS

It may be seen from above that any periodic function may be represented in the form of Walsh series given in Eq. 7 where the expansion coefficients may be obtained from Eq. 8. Since Walsh functions are of digital nature assuming values of 1 and -1, the periodic function may be realized in digital form. Using the above mentioned technique, we have generated three different functions i.e., Sinusoidal, Triangular and Trapezoidal.

Generation of Sinusoidal Functions

Considering the general sinusoidal function $f(x) = \alpha^* \sin((2\pi x))$, the first 64 expansion coefficients obtained by Eq. 8 are given below:

 $\begin{array}{l} A_{0}=0, \ A_{1}=0.6365, \ A_{2}, \ A_{3}, \ A_{4}, \ A_{5}, \ A_{6}=0, \ A_{7}=-0.2637, \ A_{8}, \ A_{9}, \ A_{10}=0, \ A_{11}=0.1266, \\ A_{12}=0, \ A_{13}=-0.0525, \ A_{14}, \ A_{15}, \ A_{16}, \ A_{17}, \ A_{18}=0, \ A_{19}=-0.0627, \ A_{20}=0, \ A_{21}=-0.0260, \\ A_{22}, \ A_{23}, \ A_{24}=0, \ A_{25}=-0.0125, \ A_{26}, \ A_{27}, \ A_{28}, \ A_{29}, \ A_{30}=0, \ A_{31}=-0.0052, \ A_{32}=0, \\ A_{33}, \ A_{34}=0, \ A_{35}=0.016, \ A_{36}=0, \ A_{37}=0.0013, \ A_{38}, \ A_{39}, \ A_{40}=0, \ A_{41}=0.0062, \\ A_{42}, \ A_{43}, \ A_{44}, \ A_{45}, \ A_{46}=0, \ A_{47}=0.0026, \ A_{48}=0, \ A_{49}=0.0021. \end{array}$

It is obvious that the precision of the function depends upon the number of terms used in the Walsh series expansion at the expense of hardware. An analysis of the waveform using MATLAB has been made. It is found that a reasonable accuracy may be obtained by using 64-term approximation in the Walsh series expansion. The resulting waveform for $\alpha=1$ is shown in Fig. 2.

Very High-Speed Integrated Circuit Hardware Description Language (VHDL) codes were written for the realization of the sinusoidal wave. The terms for Walsh series were generated and added to produce the required function. The Walsh functions assume the values of +1 and -1 and these values are to be multiplied with appropriate coefficients generated in the previous sections.



Fig.2. MATLAB Simulation of Sinusoidal Waveform using Walsh functions

It may be noted that if we assign +1 to logic '0' and -1 to logic '1' then multiplication is replaced by a simple Exclusive-OR (XOR) operation. This greatly simplifies the multiplication of waves.

The design was targeted to Xilinx FPGAs using software packages available from Xilinx. VHDL was used for design entry. The design was implemented on FPGA boards and the implementation was thoroughly analyzed, verified and tested.

The results of the functional simulation results are presented in Fig. 3. CKK is the Clock signal. First five Rademacher functions are represented by R_1 , R_2 , R_3 , R_4 and R_5 . First eight Walsh functions with non-zero expansion coefficients are represented by W_0 , W_1 , W_2 , W_3 , W_4 , W_5 , W_6 and W_7 . The digital sinusoidal wave is represented by the 16-bit vector P (P₀ to P₁₅). The use of 2's complements is made for negative numbers. The results of timing simulation are presented in Fig. 4.

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Fig.3. Functional Simulation of Rademacher, Walsh and Sinusoidal Functions



Fig.4. Timing Simulation of Rademacher, Walsh and Sinusoidal Functions

The design was targeted and downloaded to several FPGA chips from Xilinx. A snapshot depicting some of the implementation results using Xilinx Spartan-3 FPGA chip with the ideal results superimposed are shown in Fig. 5.



Fig.5. Waveforms obtained after implementation on Spartan-3 FPGA Chip

A detailed analysis showed that the instantaneous values are very close to the ideal values calculated from sine equation. The difference is so small that it cannot be seen in the figure. It is to be noted that the accuracy may be further increased by taking more terms in the Walsh series expansion. However, the results in the present form are good enough for most of the digital applications of practical interest.

Synthesis results generated by the Xilinx design tools are summarized as follows:

Number of CLBs used in the design: 166 out of 400 (41%) Minimum period: 40.928 ns Maximum net delay: 11.143 ns Maximum frequency: 24.433 MHz

Generation of Triangular Functions

A triangular waveform represented by the following equations was selected for hardware realization:

$$f(x) = \begin{cases} 4x & 0 \le x \le 0.25\\ 2-4x & 0.25 \le x \le 0.75\\ 4(x-1) & x \ge 0.75 \end{cases}$$
(9)

The MATLAB analysis gave the following first 32 coefficients of the Walsh series expansion:

$$A_0 = 0, A_1 = 0.5, A_2, A_3, A_4, A_5, A_6 = 0, A_7 = -0.25, A_8, A_9, A_{10} = 0, A_{11} = -0.125, A_{12}, A_{13}, A_{14}, A_{15}, A_{16}, A_{17}, A_{18} = 0, A_{19} = -0.625, A_{20}, A_{21}, A_{22}, A_{23}, A_{24}, A_{25}, A_{26}, A_{27}, A_{28}, A_{29}, A_{30}, A_{31} = 0, A_{10} = 0, A_{10} = -0.625, A_{20}, A_{21}, A_{22}, A_{23}, A_{24}, A_{25}, A_{26}, A_{27}, A_{28}, A_{29}, A_{30}, A_{31} = 0, A_{10} = -0.625, A_{1$$

VHDL codes were written for the realization of the triangular wave on similar lines and the design was successfully implemented. Detailed reports have been generated by the design tools and were thoroughly examined. Some of the more useful results of design and implementation are given below:

Total equivalent gate count for design: 1,170 Additional JTAG gate count for IOBs: 2,592 Peak Memory Usage: 66 MB Maximum delay = 10.574 ns

Generation of Trapezoidal Functions

The trapezoidal waveform represented by the following equations was selected for hardware realization:

$$f(x) = \begin{cases} 4x & 0 \le x \le 0.25 \\ 1 & 0.25 \le x \le 0.75 \\ -4x + 4 & x \ge 0.75 \end{cases}$$
(10)

The MATLAB analysis gave the following first 64 coefficients of the Walsh series expansion:

 $A_0 = 0.75, A_1, A_2, =0, A_3 = -0.25, A_4 =0, A_5 = -0.125, A_6 = -0.125, A_7, A_8 =0, A_9 = -0.0625, A_{10} = -0.0625, A_{11}, A_{12}, A_{13}, A_{14}, A_{15}, A_{16} = 0, A_{17} = -0.0312, A_{18} = -0.0312, A_{19} - A_{32} = 0, A_{33} = -0.0156, A_{34} = -0.0156, A_{35} - A_{63} = 0.$

VHDL codes were written for the realization of the trapezoidal wave on similar lines and the design was successfully implemented. Some of the useful results of design and implementation obtained through implementation reports are given below:

Total equivalent gate count for design: 1,882 Additional JTAG gate count for IOBs: 2,592 Peak Memory Usage: 67 MB Maximum Delay = 11.572 ns

COMPARISON OF HARDWARE REALIZATION

Our designs are largely technology independent. Thus the designs were targeted to a large number of FPGA chips supplied by Xilinx. A comparative study was done and the results of this study in case of some selected representative technologies are presented in Table 1. The trapezoidal waveform has been selected for demonstration of the comparison. One chip from each technology family has been chosen for presentation. The values of some of the useful parameters are tabulated. A clear pattern is seen and it is evident that speed and power are two main conflicting parameters. A tradeoff has to be made depending upon the actual needs and applications. The given table will help in the selection of a suitable FPGA chip for a particular application.

The proposed technique provides many significant advantages over Look-up Table based Direct Digital Synthesis (DDS) technique. These advantages are as follows:

- ✤ Simple Design
- ✤ Low cost
- Small Area
- ✤ Higher flexibility
- ✤ Versatility

Walsh functions being inherently digital are most suitable for control by digital means.

CONCLUSIONS

A technique for FPGA based hardware realization has been developed for the design, implementation and prototyping of useful functions in digital form. The technique makes use of the orthogonal functions like Rademacher and the Walsh functions for the realization. Any periodic function can be realized in its digital form with precise requirements in terms of frequency, phase, amplitude and shape etc.

The hardware realization of sinusoidal, triangular, and trapezoidal functions in their digital form has been demonstrated with good results. A comparative study of hardware realization of such functions with different technologies available from Xilinx has been done. It is concluded that virtually any periodic function may be realized directly in its digital form (without the need of Analog to Digital conversion) with the help of FPGAs using orthogonal functions. Prototypes and IP Cores for the above mentioned functions have been developed and are available.

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SN	Technology	XC2s200	XC2s300	XC2s600	XC3s5000	XCV1000	XC2v8000	XC2vp100	XC4v1x200	XCV3200	XCqv2000
1.	Average Connection Delay (ns)	1.082	1.192	1.280	0.858	1.679	0.936	0.790	0.834	1.682	1.464
2.	Maximum Pin Delay (ns)	4.193	4.906	5.832	2.758	8.266	2.952	2.419	3.238	12.429	9.738
3.	Worst Ave. Connection. Delay (ns)	2.682	3.684	4.320	2.035	4.765	2.225	1.400	2.014	5.912	4.585
4.	Clock edge to Pad delay (ns)	11.72	11.57	13.23	10.29	16.90	10.15	7.581	10.835	17.002	17.516
5.	Minimum Period (ns)	23.44	23.14	26.46	20.58	33.80	20.30	15.16	21.67	34.004	35.032
6.	Maximum Frequency (MHz)	42.66	43.21	37.79	48.59	29.58	49.26	65.96	46.15	29.41	28.545
7.	Number of SLICEs	79	79	79	81	79	81	81	82	79	79
8.	Number of External IOBs	53	53	53	54	53	54	54	54	53	53
9.	Total Equivalent Gate Count	1882	1882	1882	1879	1882	1879	1879	1906	1882	1882
10.	Estimated power consump. (mW)	13	28	34	515	32	787	1165	-	367	907
11.	Estimated junction Temp. (°C)	25	26	26	25	25	33	25	-	30	34
12.	Design Score	162	193	214	126	263	138	107	124	286	238

Table 1: Comparison of Hardware Realization with Different Devices

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