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Modeling of Current-Voltage Characteristics of Deep Submicron MOSFET

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ABSTRACT

One of the deficiencies of many MOSFET models is that they are regional and can have discontinuities at the boundaries between regimes. This causes problems for deriving the conductance in circuit simulation.

In this paper, a physical one-dimensional MOSFET model is developed. Discontinuities between linear and saturation regimes are avoided using one-region closed-form equation for the drain current. The strong inversion current-voltage (I-V) characteristics for submicron n-channel MOSFET which is suitable for circuit simulation and rapid process characterization are presented. The model is also suitable as a starting solution for two-dimensional numerical modeling.

The resulting drain current is continuous over the entire operating range of the transistor. The calculated drain current is in agreement with publishing data using similar approaches.

KEY WORDS
MOSFET, Current-voltage characteristics, Submicron semiconductor devices.

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Introduction

The ULSI technology has driven the MOSFET into the deep submicron miniaturized structures. Although models based on quantum transport are needed to characterize these devices, there is a need to quick and reliable models to be incorporated in the present circuit simulators.

Realizing the fact that MOSFET's, no matter how small they are, still obey the fundamental MOS device physics , and that short-channel effects are gradual effects as the channel length is reduced, many models have been built to express the drain current in one equation and avoid discontinuities arise in some previous models. Moon, et al [1] proposed a semi-empirical strong inversion I – V model for submicron n-channel MOSFET's suitable for circuit simulation and rapid process characterization. Their model was based on a velocity-field relationship in the linear region and finite drain conductance due to channel length modulation effect in the saturation region. Joardar, et al [2] proposed MOSFET model that has overcome the discontinuities at the boundary between forward and reverse modes of operation. They used a proper velocity-field expression and applied a smoothing function at the transition between linear and saturation regions. This model has been implemented in MCSPICE simulator. Zhou and Lim [3] formulated a compact I – V models for deep submicron MOSFET devices. The model is a one-region closed-form equation that resembles the same form as long channel one, which covers full range of channel length and bias conditions. Abebe et al [4] used the methods of asymptotic analysis for modeling the I – V characteristics of MOSFET.

This paper reports an approach for the inversion layer charge and the current-voltage characteristics of n-channel MOSFET transistor. The transistor with its external bias is shown in Fig.1. It has a metal electrode as a gate, an oxide layer and a p-substrate. The source and drain regions are n-type.

Inversion Layer Charge

The solution of Poisson equation permits to obtain an expression of the inversion layer charge as a function of the gate voltage, the oxide capacitance and the depletion capacitance. The vertical electric field and the lateral electric field are assumed to be independent of each other. The separation of the electric field in the depletion layer and that in the inverted channel permits the solution of the Poisson equation in each region.

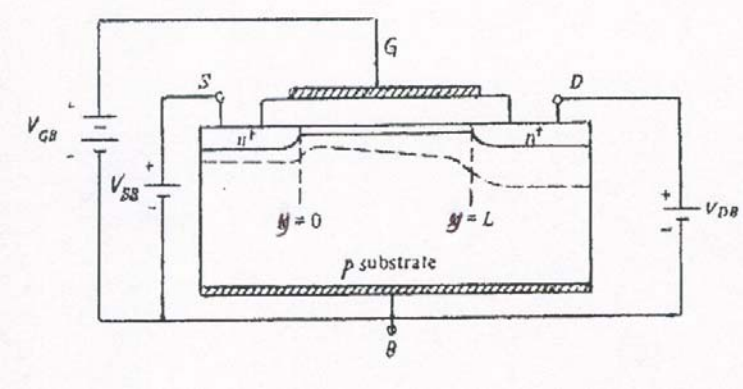

Fig.1 An n-channel MOSFET with external biases

The Poisson equation is

$$\frac{d^2\psi}{dx^2} = \frac{e}{\varepsilon_s}(n - p + N) \tag{1}$$

Where ψ is the potential in the channel, x is the coordinate perpendicular to the channel, ε_s is the silicon permittivity, e is the electronic charge, n is the electron density, p is the hole density and N is the substrate doping.

$$n = n_i e^{(\psi - \varphi_f)/\varphi_t} \tag{2}$$

$$p = n_i e^{(\varphi_f - \psi)/\varphi_t} \tag{3}$$

Where n_i is the intrinsic carrier density, φ_f if the Fermi potential and φ_t is the thermal voltage.

In this model, p-silicon substrate is considered. The hole density in the depletion region is neglected. The neutral p-substrate is used as the potential reference, that is, $\psi = 0$, then Eq. (3) may be written as

$$\frac{n_i}{N} = e^{-\varphi_f/\varphi_t} \tag{4}$$

Poisson equation may be multiplied by dΨ/dx and integrated to

$$\frac{1}{2}\frac{d}{dx}\left(\frac{d\psi}{dx}\right)^2 = \frac{\varphi_t}{L_D^2}\frac{d}{dx}\left(\psi + \varphi_t e^{(\psi-2\varphi_f)/\varphi_t}\right) \tag{5}$$

where L_D is the extrinsic Debye length given by

$$L_D = \sqrt{\frac{\varepsilon_s \varphi_t}{eN}} \tag{6}$$

Integrating Eq. (5) with the boundary condition

$$\begin{aligned} \psi = \psi_s \quad & x = 0 \\ = 0 \quad & x = x_d \\ d\psi/dx = 0 \quad & x = x_d \end{aligned}$$

where x_d is the space charge width and Ψ_s is the surface potential, gives the surface electric field $F_s = -\, d\psi/dx$, from which the surface charge per unit area is then

$$Q_s = -\,\varepsilon_s F_s = -C_{FB}\sqrt{2\varphi_t\left(\psi_s + \varphi_t e^{(\psi_s-2\varphi_f)/\varphi_t}\right)} \tag{7}$$

Where C_{FB} is the flat band capacitance given by

$$C_{FB} = \varepsilon_s/L_D \tag{8}$$

The bulk charge Q_B is given by

$$Q_B = \sqrt{2e\varepsilon_s N\psi_s} \quad = \quad \gamma C_o\sqrt{\psi_s} \tag{9}$$

where $\gamma = \sqrt{2e\varepsilon_s N}/C_o$ and is the oxide capacitance per unit area.

The inversion layer charge is then

$$Q_I = Q_s - Q_B = -\gamma C_o\left(\sqrt{\left(\psi_s + \varphi_t e^{(\psi_s - 2\varphi_f)/\varphi_t}\right)} - \sqrt{\psi_s}\right) \quad (10)$$

When a gate voltage V_{GB} relative to the substrate is applied, then

$$V_{GB} = V_{FB} + \psi_s - Q_s/C_o$$

$$= V_{FB} + \psi_s + \gamma\sqrt{\left(\psi_s + \varphi_t e^{(\psi_s - 2\varphi_f)/\varphi_t}\right)} \quad (11)$$

where V_{FB} is the flat band voltage.

Eq.(11) gives the relation between the gate bias and the surface potential. Three regions of operation have been considered [4]. They are the weak, moderate and strong-inversion regions.

Threshold Voltage

The threshold voltage specifies the critical gate voltage at which inversion layer is formed to a significant extent, giving rise to rapid increase of the inverse charge for higher gate voltages. The threshold voltage supports a bulk charge Q_B and at the same time introduces a band bending at the surface to reach the strong inversion potential φ_{si}. In addition it includes the metal-semiconductor work-function difference φ_{ms} and the oxide charge Q_o. Therefore, the threshold voltage is

$$V_T = V_{FB} + \varphi_{si} - gQ_B/C_o \quad (12)$$

The flat band voltage is given by

$$V_{FB} = \varphi_{ms} - Q_o/C_o \quad (13)$$

If a voltage ψ is established in the channel by external voltages at the source and drain under strong inversion, the bulk charge Q_B from Eq. (9) can be written as

$$Q_B = \sqrt{2e\varepsilon_s N(\psi + \varphi_{si})} \quad (14)$$

If the p-substrate has a negative voltage $-V_{BS}$, the negative space charge layer is widened and Q_B is now

$$Q_B = \sqrt{2e\varepsilon_s N(\psi + \varphi_{si} + V_{SB})} \quad (15)$$

g is the geometric factor to account of the short channel effect and is given by [5]

$$g = 1 - \frac{r_j}{L}\left(\sqrt{1 + \frac{2x_{dm}}{r_j}} \quad 1\right) \quad (16)$$

where L is the channel length and r_j is the junction depth.

Current – voltage relation

The inversion layer charge is obtained using Eq. (9) and Eq.(11), namely

$$Q_I = - C_o (V_{GB} - V_{FB} - \psi_s - \gamma\sqrt{\psi_s}) \quad (17)$$

Taking into account the drift and diffusion currents, the drain current is then

$$I_D L = \mu_n W \int_{\psi_{so}}^{\psi_{sL}} (-Q_I) d\psi_s + \mu_n W \varphi_t \int_{Q_{Io}}^{Q_{IL}} dQ_I \quad (18)$$

Where the first term is the drift current and the second term is the diffusion current.

Using Eq.(17) the integration of Eq.(18) yields the drain current

I_D

$$= \mu_n \frac{W}{L} C_o[(V_{GB} - V_{FB})(\psi_{sL} - \psi_{so}) - \frac{1}{2}(\psi_{sL}^2 - \psi_{so}^2) \quad \frac{2}{3}\gamma(\psi_{sL}^{2/3} - \psi_{so}^{2/3})] + \mu_n \frac{W}{L} C_o \varphi_t[(\psi_{sL} - \psi_{so}) + \gamma(\psi_{sL}^{1/2} - \psi_{so}^{1/2})] \tag{19}$$

where

$$\psi_{so} = V_{GB} - V_{FB} - \gamma[\psi_{so} + \varphi_t e^{(\psi_{so} - 2\varphi_f - V_{SB})/\varphi_t}] \tag{20}$$

and

$$\psi_{sL} = V_{GB} - V_{FB} - \gamma[\psi_{sL} + \varphi_t e^{(\psi_{sL} - 2\varphi_f - V_{DB})/\varphi_t}] \tag{21}$$

As the surface potential is the sum of φ_{si} and the appropriate bias

$$\psi_{so} = \varphi_{si} + V_{SB}$$

$$\psi_{sL} = \varphi_{si} + V_{DB}$$

Where $V_{GB} = V_{GS} + V_{SB}$

$V_{DB} = V_{DS} + V_{SB}$

The drain current is then

I_D =

$$\mu_n \frac{W}{L} C_o [(V_{GS} - V_{FB} - \varphi_{si}) V_{DS} - \frac{1}{2} V_{DS}^2 - \frac{2}{3} \gamma \{(\varphi_{si} + V_{SB} + V_{Ds})^{3/2} -$$

$$(\varphi_{si} + V_{SB})^{3/2}\}] + \mu_n W C_o \varphi_t [V_{DS} + \gamma(\varphi_{si} + V_{SB} + V_{DS})^{1/2} - (\varphi_{si} + V_{SB})^{1/2}]$$

(22)

Results and Conclusions

The model has been applied to MOSFET with the following parameters:
Gate oxide thickness t_{ox} = 250A
Flat band voltage V_{FB} = - 0.85 V
Low field mobility μ_n = 870 cm^2/Vs
Channel doping $5x10^{16}$ cm^{-3}
Channel length L = 0.25 μm
Channel width W = 1μm

Fig.2 shows the I-V characteristic of the modeled MOSFET.

In conclusion, the idea of this model is to provide a quick and reliable tool for deep-submicron technology development and a circuit models. The model is also considered as a starting solution for two-dimensional numerical simulation.

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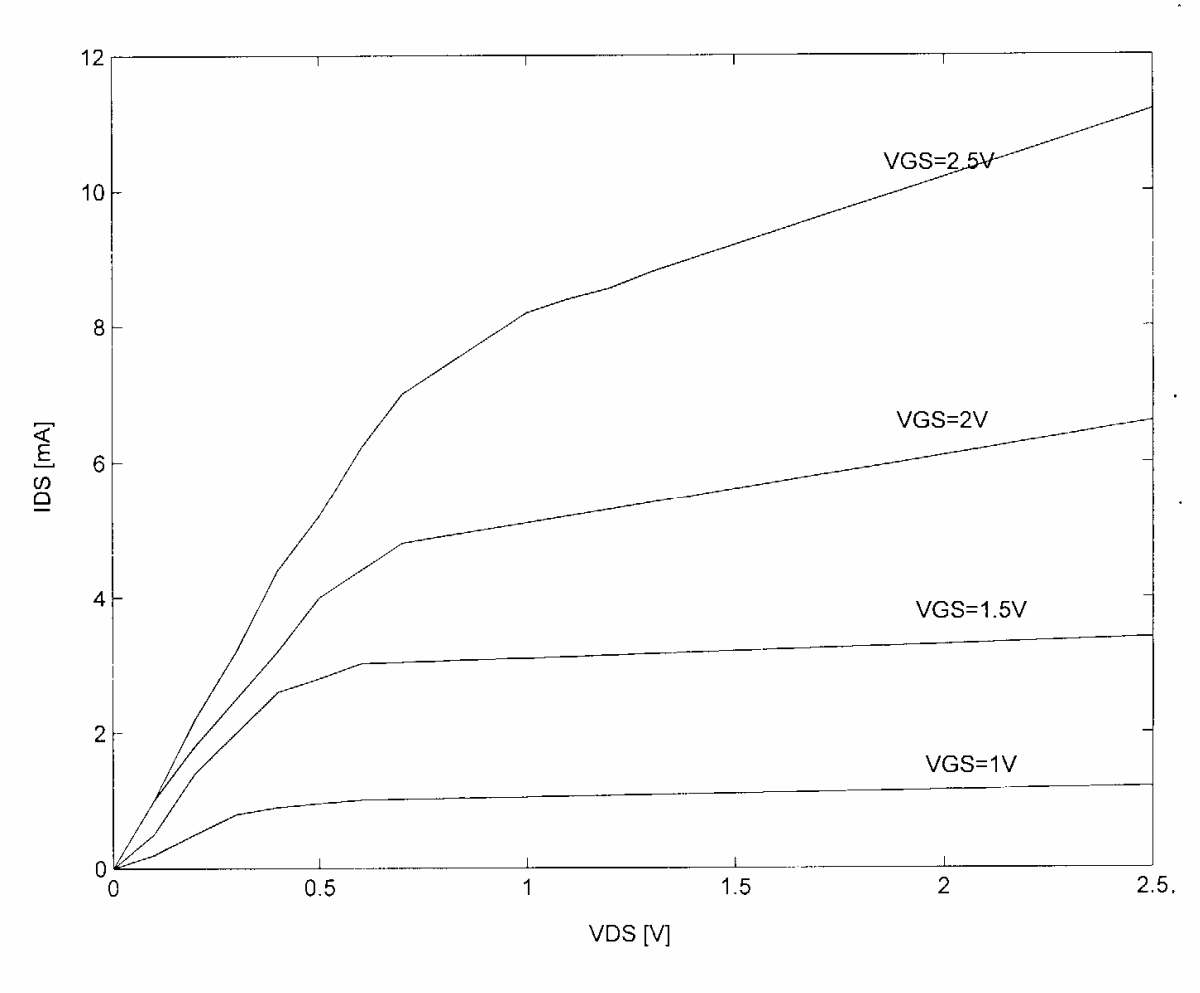

Fig.1 The modeled I – V characteristic of MOSFET.