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A NOVEL TESTING METHOD FOR MONOSTABLE MULTIVIBRATORS

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ABSTRACT

Several authors focused on testing of digital integrated circuits and their different test scenarios are proposed. No author speaks about the testing of the monostable multivibrator on the board. In this paper, a novel circuit design methodology is presented to test the monostable multivibrators functionally on the board. To test the monostable multivibrators properly, the time duration needs to be measured accurately. This method is based on the signature generation of the output of the monstable multivibrators. The measurement of the time duration is considered the signature that expresses the proper functionality of the monstable multivibrators. This testing design was implemented and applied to different pulse durations. The experimental results indicate the high accuracy of the proposal design approach. The measurements in the *millisecond* range had not any deviation from the setting pulse. The measurements in the *microsecond* range had small deviation from the setting pulse ± 1%.

KEYWORDS: Design-for-test (DFT), Automatic Test Equipment, Testing of electronic circuits.

1. INTRODUCTION

Military equipment and aviation systems have been characterized by the increased number of electronic components and the complexity of electronic systems. Sooner or later, every electronic system ends up in repair facility. When electronic equipment is not operational, the cost of being out of service (down time) is too high. Automatic testing techniques [1]-[3] achieve full flexibility of the adequate various test tasks required by a variety of units under test (UUT) such as automatic fault diagnosis, repair integration and qualification.

Automatic Test Equipment (ATE) are widely used to detect faults in digital and analog electronics systems [1]. ATE contribute to an improvement in product quality and productivity in the electronics industry through the transfer of control over the test cycle from an operator to an electronic controller. The semiconductor and component test category include a wide range of ATE systems that test individual components. Some test digital devices, including VLSI circuits, memory chips, and microprocessors. Others are specialized for analog devices. The third are used for discrete semiconductors, such as transistors, diodes, and zener diodes. The requirements within this category vary considerably. A test system for RAM chips, for example, must have the ability to provide complex test patterns in order to test the chip; memory locations and control pins [4]-[5].

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Numerous test pattern generation and test response compaction techniques of the digital integrated circuits have been proposed in the available literature [6]-[10]. These techniques are used in industrial practice as implementation platforms to cope with these objectives, for various types of failure, error, and in a variety of test scenarios. Several design techniques have been used over the years to avoid potential problems with testing. They are mostly aimed to improve testability across the entire circuit. In Built-In Self-Test (BIST), additional circuitry is included to generate test patterns, evaluate test responses, and control the test. Test patterns can be generated by simple circuits [9]-[10], and test responses can be compacted into a signature. This signature, obtained from the circuit under test (CUT), can be subsequently compared with a fault-free signature. High fault coverage in BIST can be achieved only if all faults of interest are detected and their effects are retained in the final signature after compaction.

The monostable multivibrator is mixed between analog and digital part. It has only one stable output state. The other output state can only be maintained temporarily. Monostable multivibrators sometimes called *one-shot* integrated circuits. One-shot circuits with very short time settings may be used to debounce the "dirty" signals created by mechanical switch contacts. In the past, mono-stable multi-vibrators (one-shots) were disconnected from the CUT and the tester is responsible for generating required pulses during testing operation. No author speaks about the testing of the monostable multivibrator on the board. In this paper, I present a novel circuit design methodology to test the monostable multivibrators functionally on the board. The functional testing is most important to the final user. It verifies that the circuit meets its performance specifications, i.e. it performs the functions it was designed for. To test the monostable multivibrators properly, the time duration needs to be measured accurately. The measurement of the time duration is considered the signature that expresses the proper functionality of the monstable multivibrators.

I will begin with the concept of the monstable multivibrators in section 2. Concept of the testing method will be in section 3. Circuit diagram of the design and its experimental results will be in section 4 and the conclusion in section 5.

2. BASIC CONCEPT OF THE MONOSTABLE MULTIVIBRATORS

A monostable device is only able to hold in one particular stable state indefinitely. The unstable state can only be held momentarily when triggered by an external input. A latch or flip-flop, being a bistable device, can hold in either the *set* or *reset* state for an indefinite period of time. Once it is set or reset, it will continue to latch in that state unless prompted to change by an external input. All monostable multivibrators are *timed* devices. That is, their unstable output state will hold only for a certain minimum amount of time before returning to its stable state. With semiconductor monostable circuits, this timing function is typically accomplished through the use of resistors and capacitors, making use of the exponential charging rates of RC circuits. A comparator is often used to compare the voltage across the charging (or discharging) capacitor with a steady reference voltage, and the on/off output of the comparator used for a logic signal. No matter how long the input signal stays high, the output remains high for just 1 second of time for example, and then returns to its normal (stable) low state as shown in Fig. 1.

For some applications, it is necessary to have a monostable device that outputs a longer pulse than the input pulse which triggers it as shown in Fig. 2. No matter how short the input pulse is; the output stays high for certain specific duration after the input drops low again. This kind of monostable multivibrator is called a *one-shot*. More specifically, it is a *retriggerable* one-shot, because the timing begins after the input drops to a low state, meaning that multiple

input pulses within 10 seconds of each other will maintain a continuous high output as shown in Fig. 3.

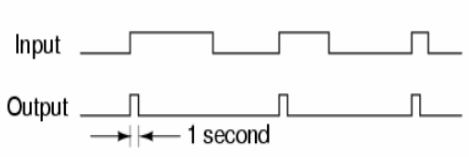

Fig. 1.

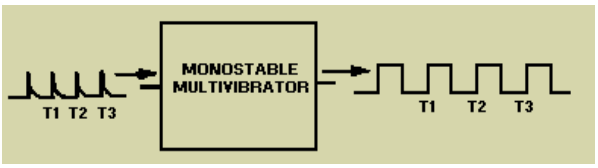

Fig. 2.

What if we only wanted a 10 second timed pulse output from a relay logic circuit, regardless of how many input pulses we received? In that case, the one-shot circuit is called the *nonretriggerable* one-shot as shown in Fig. 4. The objective here in this paper is to test the monostable multivibrators functionally on the board. To test the monostable multivibrators properly, the time duration needs to be measured accurately. In the next section, I present the concept of the testing design approach to do that.

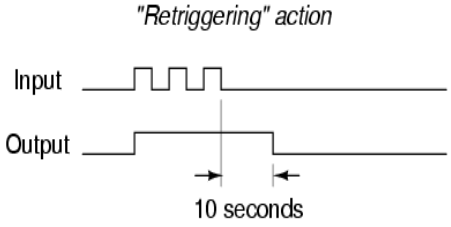

Fig. 3.

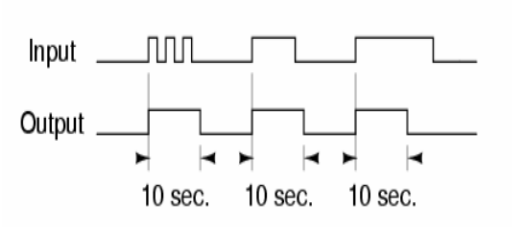

Fig. 4.

3. CONCEPT OF THE TESTING METHOD

The testing design approach, that tests the monostable multivibrators, is a mixture between analog and digital part. It measures the time between each edge of the pulse duration (unstable state) generated from the monostable multivibrators. The analog part is concerning of the detection of each edge of the pulse duration and constructs the starting and stopping of the measurement period. In the other side, the digital part is concerning of the time measurement digitally and automatically transfers to the personal computer (PC). Fig. 5 illustrates the block diagram of the testing design.

The analog part consists of differentiator, amplifier and rectifier. All these are considered as edge detector which is necessary so that the circuit will count only once for each edge. A differentiator stage produces an output voltage that is proportional to the slope (i.e., rate of change of the input signal). The fast change will produce larger output voltage than the constant value. The positive spike is generated due to the rising edge of the pulse and the negative spike is generated due to the falling edge of the same pulse. An amplifier amplifies the spikes generated from the differentiator. The rectifier is designed to rectify the negative spikes. The rectified spikes trigger a monostable multivibrator that generates one output pulse for each spike. These pulses have constant duration and amplitude. They trigger the first 5 μs monostable multivibrator, which produces pulse P1. The falling edge of pulse P1 triggers the second monostable multivibrator that also produces a 5 μs duration pulse P2. These two pulses are controlled by a NOR gate, which has output P3. This signal is high during the interval when PI and P2 are not occurring.

Immediately following the initiation of a spike, pulse P3 goes low for a total of 10 μs and is then returned to its initial level. The signal controls an AND gate so that a 1 KHz clock signal (or 1 MHz clock) is allowed to enter a counting circuit whenever P3 is high. Because P3 is high during the interval between spikes, the l-ms pulses (or 1-μs pluses) coming from the

clock (P4) clocks the counter during this period. If it is initially at zero, the number of pulses in the next spike arrives equals the number of milliseconds (microseconds) in the interval between this spike and the previous one.

Once the gate prohibits additional clock pulses from entering counter, pulse P1 enables the signal to be stored in a Latch, which serves as a memory. It is important to note that the contents of the counter must be zero before the gate is opened. Once the contents of the counter have been transferred to the latch, pulse P_2 clears the counter, and prepares it to next measurement. The latch can be then interfaced with the PC parallel port where the period value can be displayed on the computer monitor and processed.

This way of measurement is based on the edge detection. There is another way of measurement based on gating the clock using pulse duration itself. The explanation of the implementation of these two ways of time measurements will be explored in section 4.3.

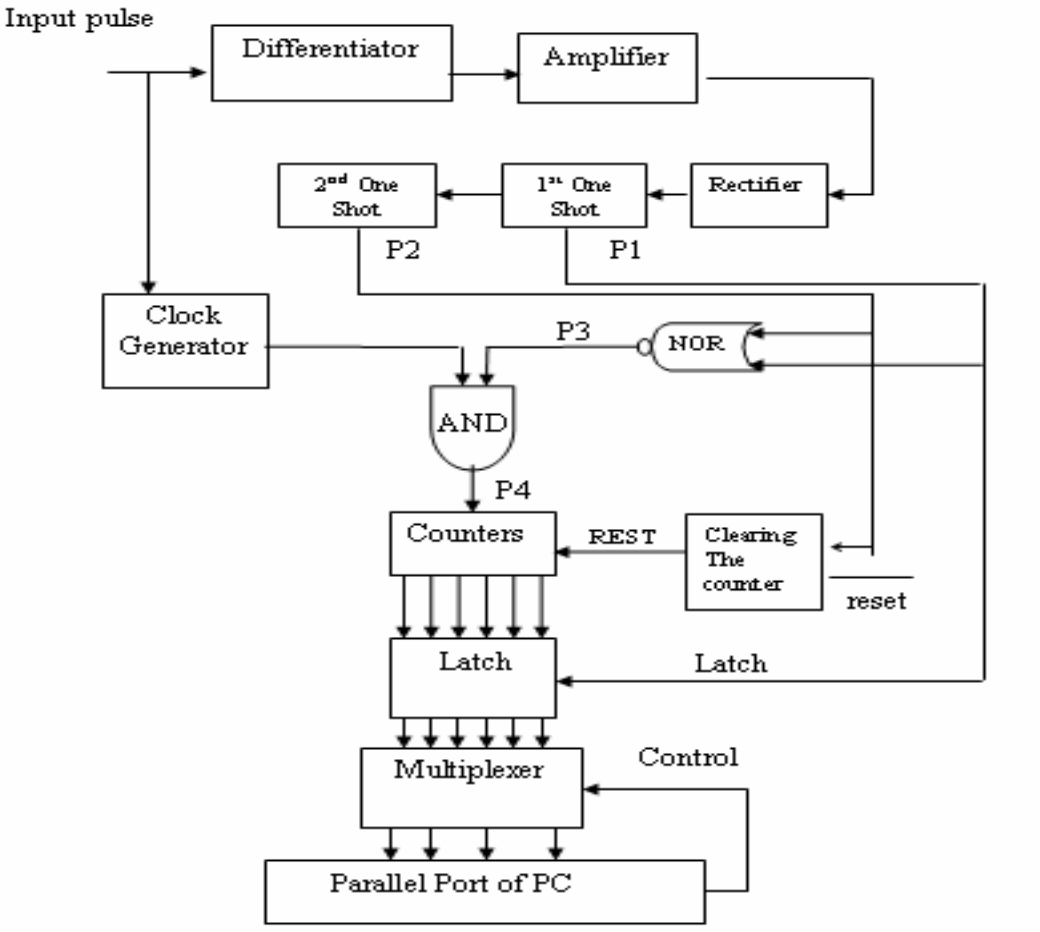

Fig. 5. Block diagram of the testing Design.

4. CIRCUIT DIAGRAM OF THE TESTING DESIGN AND ITS EXPERIMENTAL RESULTS

In the previous section, the block diagram of the testing design approach and the function of its blocks were studied. In this section, the design of each block as a circuit level using circuit simulator is presented.

4.1 Analog Part

The schematic diagram of the analog part is shown in Fig. 6. A differentiator stage, represented by R1 and C1, is the first stage of this part. Simple amplifier using an operational amplifier is utilized next to the differentiator. The output waveforms (V(A)) of the differentiator with amplifier stage are shown in Fig. 7. The rectifier stage is the next stage to produce two spikes in the positive polarities. The output of the rectifier (V(B)) is applied to Schmitt trigger inverter (74LS14) to produce V(C) as shown in Fig. 7. The generated pluses trigger a monostable multivibrator next to this stage. This one-shot stage will generate one output pulse for each rising edge or falling edge. These pulses have constant duration and amplitude. For a monostable multivibrator, I used 74LS123 connected as shown in Fig. 6. After the output of the first monostable multivibrators is triggered, it will produce pulse P1. The falling edge of pulse P1 triggers a second monostable multivibrator that also produces pulse P2 after the initiation of pulse P1 as shown Fig. 7.

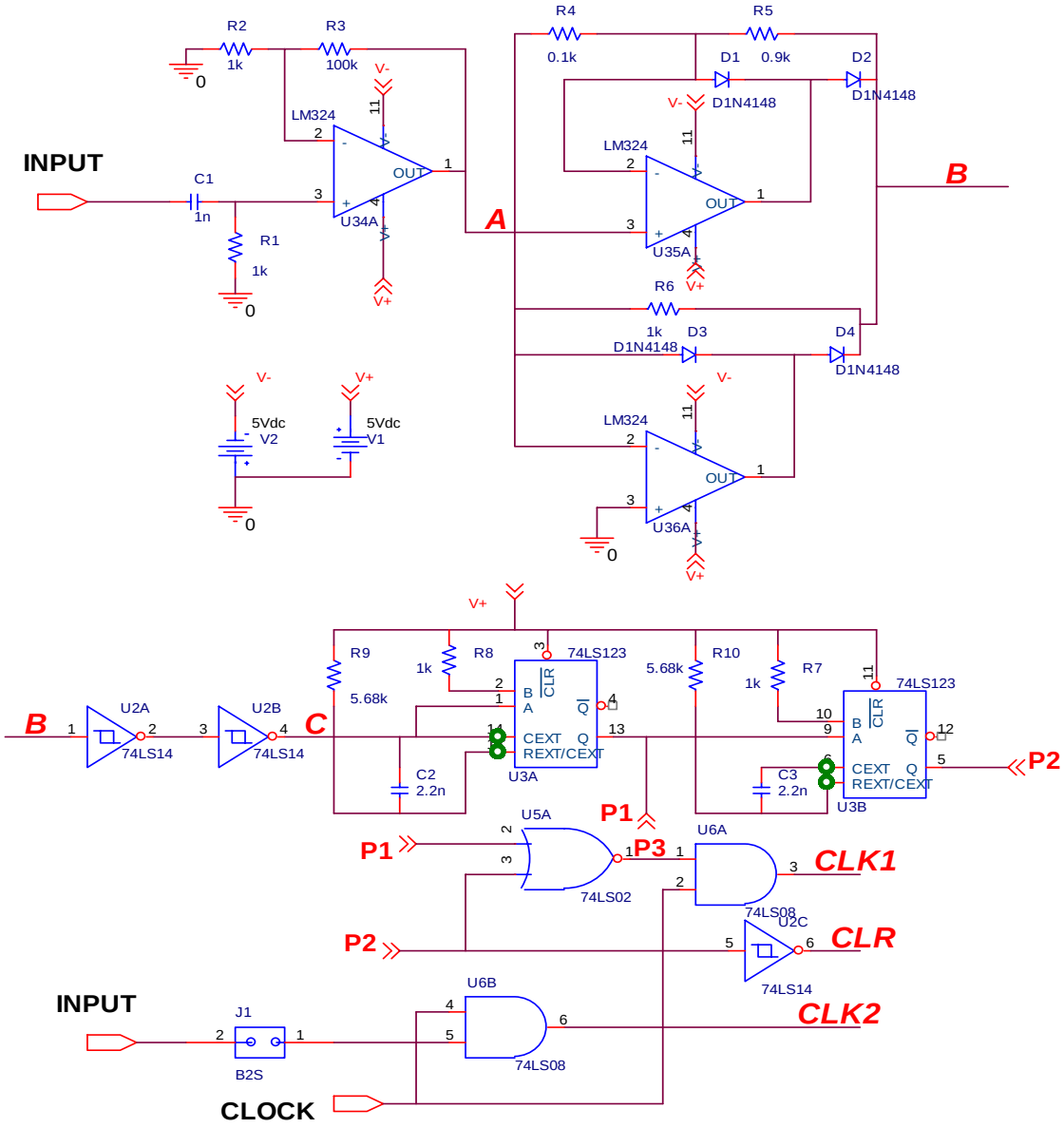

Fig. 6. Schematic diagram of the analog part.

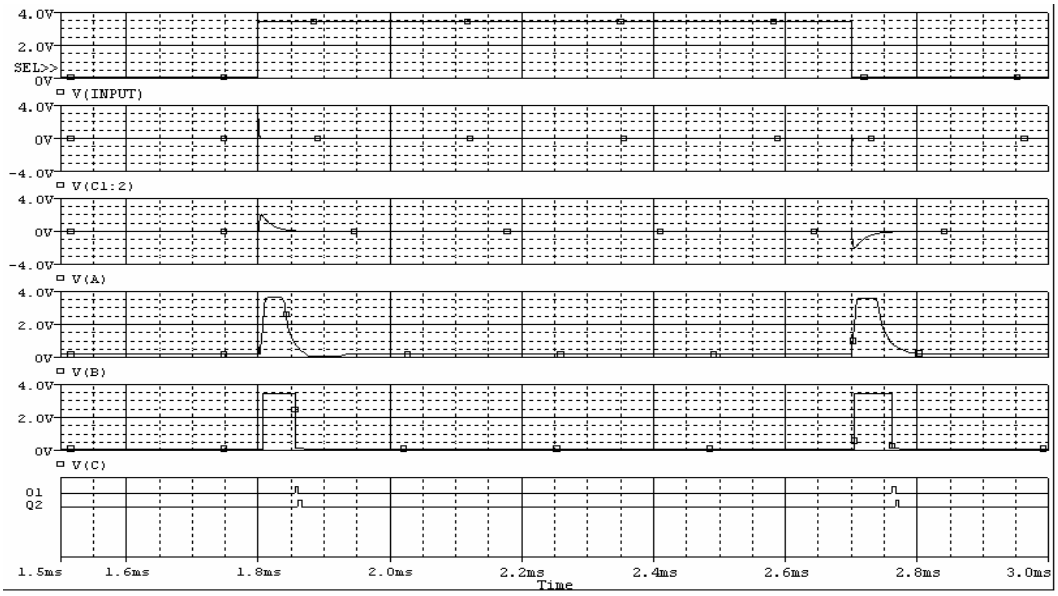

Fig. 7. Timing diagram for the schematic diagram of Fig. 6.

The detail explanation about the generation of CLK1, CLR, and CLK2 as shown in Fig. 6 will be presented in section 4.3.

4.2 Clock Generation

The circuit design has internal clock 1 MHz that generates microsecond range. Another 1 kHz clock, derived from 1 MHz, generates millisecond range. The clock (1 MHz) is divided by 1000 to produce 1 kHz clock. Each decimal counter (74LS190) divides by 10. Three decimal counters produce the desire division. Both these clocks are applied to digital multiplexer (74LS157) to switch between the microsecond range and millisecond range. Fig. 8 illustrates the schematic diagram of the clock generator.

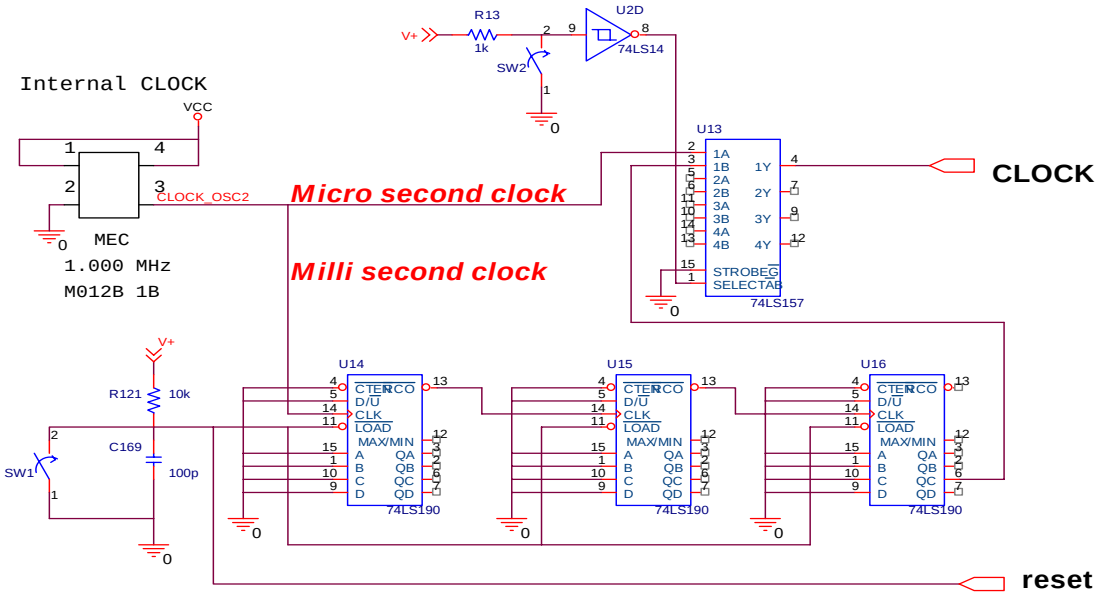

Fig. 8. Schematic diagram of clock generation part.

4.3 Counter

The schematic diagram of the counter is shown in Fig. 9. The counter in this diagram is represented by U9, U10, U11, and U12 (74LS190). The control signal for clocking the counter is CLK (P4) and for clearing the counter is REST. There is two way to control the counter operation. Each way has its own control signals which are applied to digital multiplexer (74LS157) to switch between them. CLK1, and CLR as shown in Fig. 6 to be utilized in the first way and CLK2 as shown in Fig. 6 and *reset* signal as shown in Fig. 7 to be utilized in the second way are applied to digital multiplexer (74LS157).

In the first way, CLK1 gated by P1 and P2, and CLR generated from P2 are applied to control the counter operation. The output signal P3 in Fig. 6 is high when PI and P2 are not occurring and goes low for a total of 10 μs immediately following the initiation of the rising or falling edge of the pulse. P3 controls an AND gate so that CLK1 is allowed to clock counter whenever it is high during the pulse duration. Once the gate prohibits additional clocks from entering counter, pulse P1 enables the content of the counter to be stored in the latch U7 and U8 as shown in Fig. 9. It is important to note that the contents of the counter must be zero before opening gate. Once the latch loads the content of the counter, pulse P_2, sets the counter to zero, and prepares it to count the next duration. The content of the counter equals the number of milliseconds or microsecond of the pulse duration. The timing diagram based the first way is illustrated in Fig. 10. In this figure, the pulse duration with 900 μs is generated from monostable multivibrator circuit. The content of the counter is 897 counts which mean 897 μs.

In the second way, CLK2 generated from Fig. 6 and *reset* signal from Fig. 7 are applied to control the counter operation. CLK2 is gated by the pulse duration itself through U6B as shown in Fig. 6 to clock the counter. The *reset* signal is generated from push bottom switch to clear the counter before the next measurement. The timing diagram based the second way is illustrated in Fig. 11. In this figure, the pulse duration with 900 μs is generated from monostable multivibrator circuit. The content of the counter is 901 counts which is 901 μs.

The first way has advantages and disadvantages. The advantage is capable to work with any amplitude. The disadvantage is low accuracy blew 100 μs due to the slow rate of the OP AMP. For example, if the pulse duration is applied with 20 μs, the content of the counter is 33 counts (33 μs). Also, the second way has advantages and disadvantages. The disadvantage is not capable to work with any amplitude just TTL level as shown in Fig. 6. The advantage is the high accuracy blew 100 μs. For example, if the pulse duration is applied with 20 μs, the content of the counter is 21 counts (21 μs).

This design was implemented and applied to different pulse width from 100 μs to 9999 *msec*. The measurements in the millisecond range had not any deviation from the setting pulse. The measurements in the microsecond range had small deviation from the setting pulse around ± 1%. The second way has a good accuracy blew 100 μs in expense of the limited amplitude just TTL level.

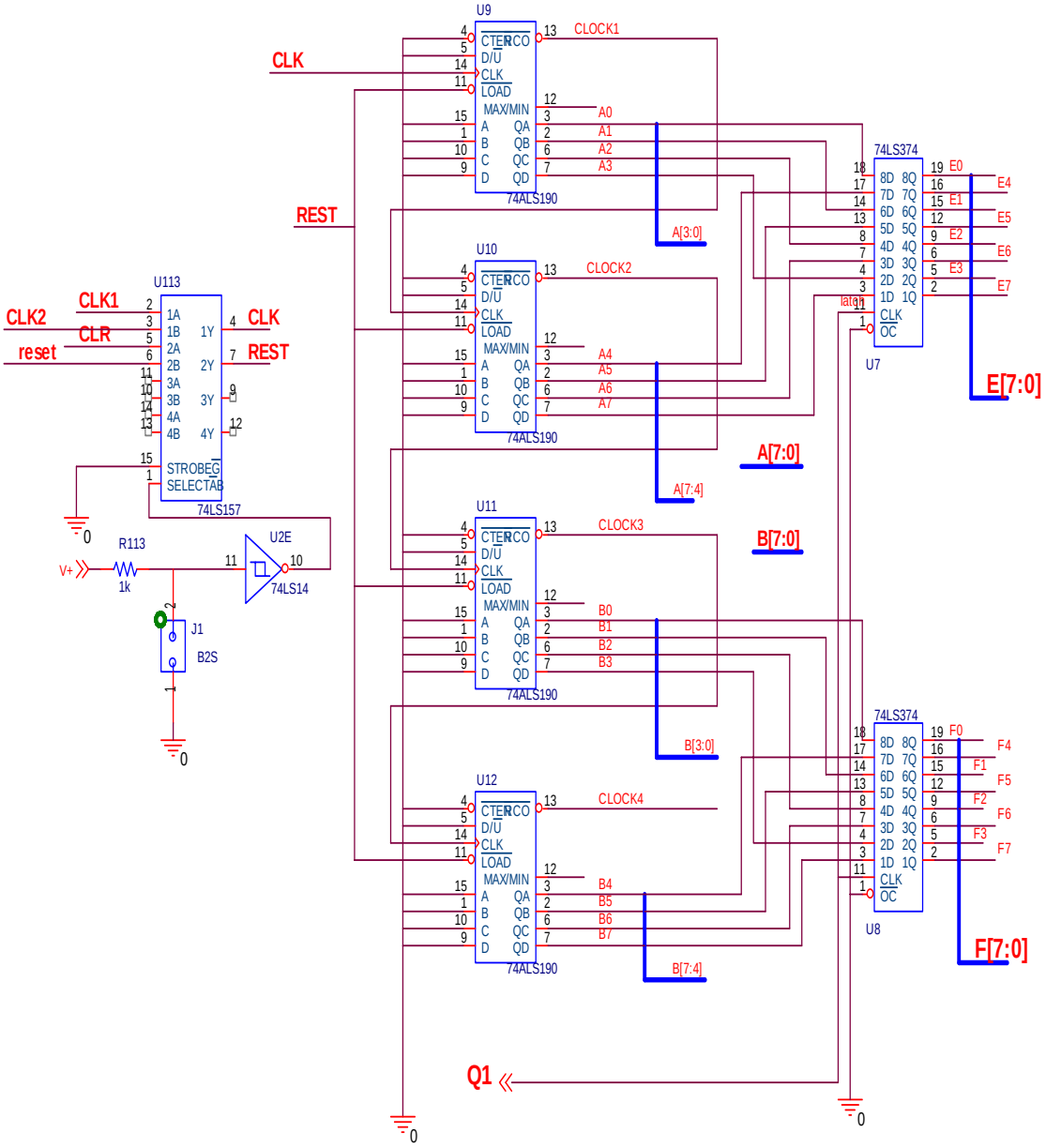

Fig. 9. Schematic diagram of the counter part.

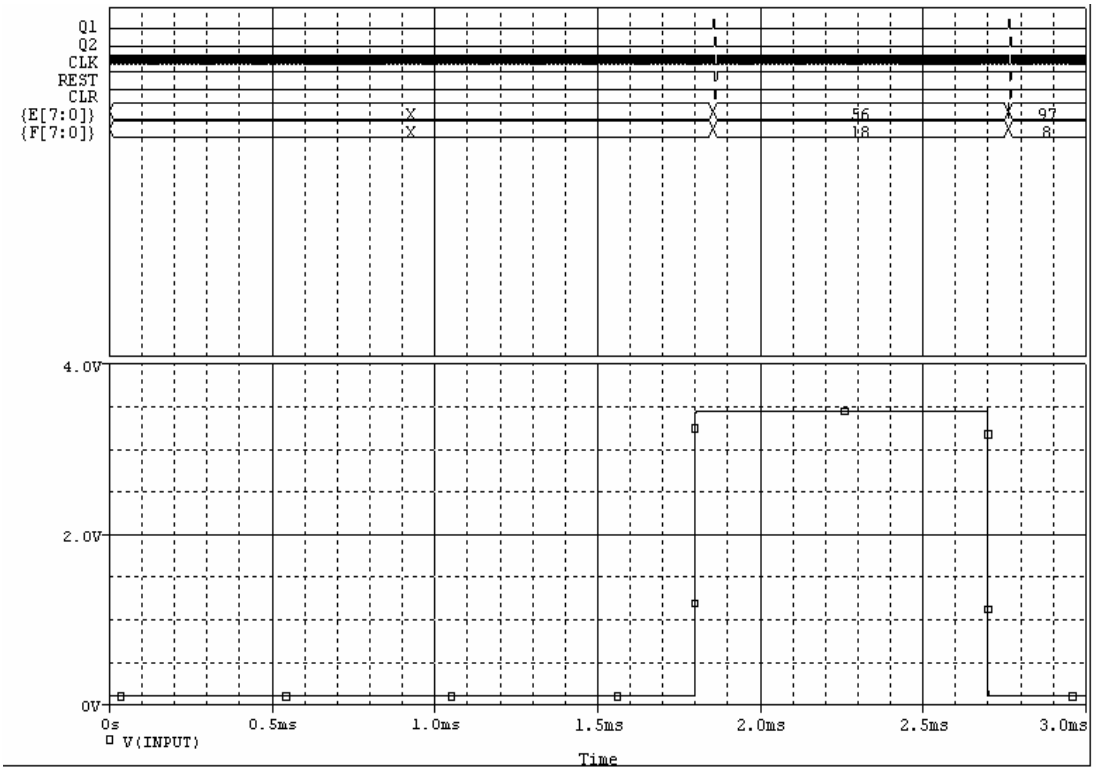

Fig. 10. Timing diagram based in the first way.

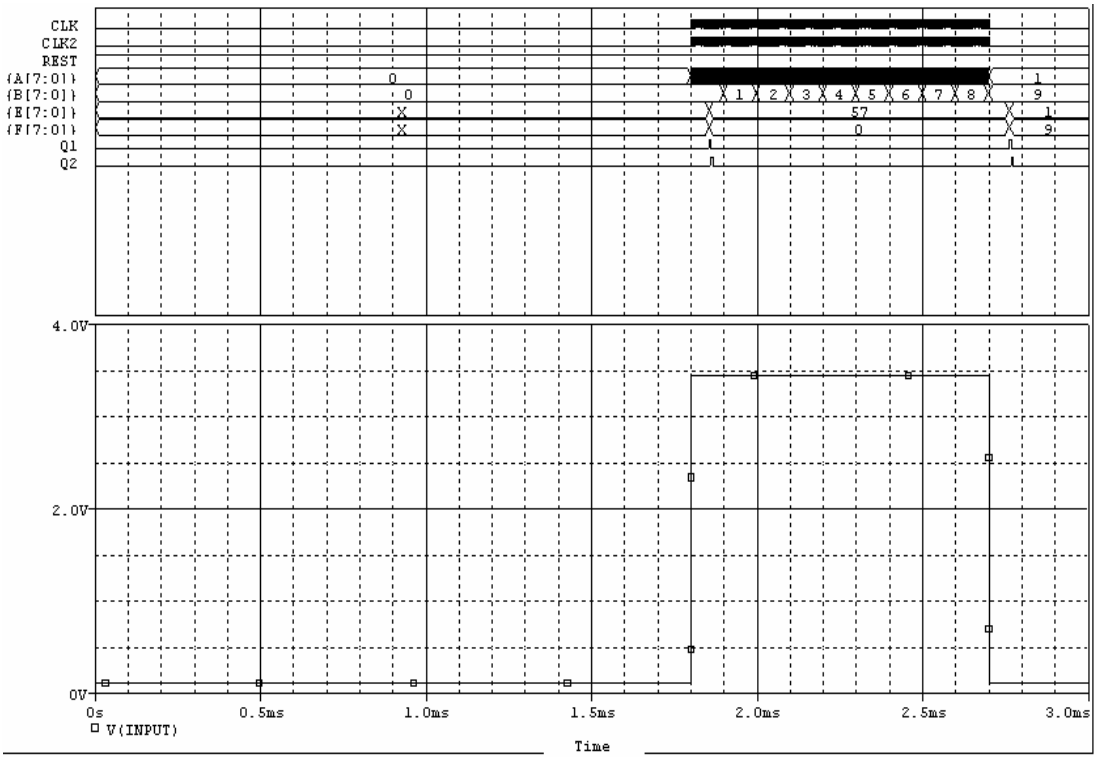

Fig. 11. Timing diagram based in the second way.

4.4 Interfacing Part

The original IBM-PC's Parallel Printer Port had a total of 12 digital outputs and 5 digital inputs accessed via 3 consecutive 8-bit ports in the processor's I/O space. It's found commonly on the back of your PC as a D-Type 25 Pin female connector.

- 8 output pins accessed via the **DATA Port**
- 5 input pins (one inverted) accessed via the **STATUS Port**
- 4 output pins (three inverted) accessed via the **CONTROL Port**
- The remaining 8 pins are grounded

Control signals required to control the set of digital multiplexers (74LS157) are generated from data port as shown in Fig. 12. These multiplexers are placed at the output of the latches of Fig. 9. The 16 bits generated from the latches need to be automatically transferred to the computer through parallel port. Control signals and inputs to the parallel port (output of the last multiplexer) are shown in Fig. 12.

Nibble mode is the preferred way of reading 16 bits of data. It uses three multiplexer (Quad 2 line to 1 line) to read a nibble of data at a time. Software can then be used to construct the four nibbles into a digital signature, expressed the time duration. The operation of the 74LS157, Quad 2 line to 1 line multiplexer is quite simple. It simply acts as four switches. When the A/B input pin is low, the A inputs are selected. E.g. 1A passes through to 1Y; 2A passes through to 2Y etc. When the A/B input pin is high, the B inputs are selected. The Y outputs are connected up to the status port, in such a manner that it represents the most significant nibble of the status register. First, the multiplexer must be initialized to switch either inputs A or B. Once the low nibble is selected, we can read the least significant nibble from the status port. Take note that the last line toggles bit inverted, however we won't tackle it just yet. We are only interested in the most significant nibble of the result, thus we AND the result with 0xF0, to clear the least significant nibble. Now it is time to shift the nibble we have just read to the least significant nibble. The multiplexers can be switched to select the remaining nibbles.

5. CONCLUSION

This paper presented the testing design approach that tests monostable multivibrators. This design measures the time between each edge of the pulse duration generated from the monostable multivibrators. Two ways of measurements are explored. The first way is based on detecting each edge of the pulse duration, constructs the starting and stopping of the measurement period, and automatically transfers this measurement to the personal computer (PC). The second way is based on the gating clocks using the pulse duration itself.

The design of each block as a circuit level using circuit simulator was presented. The simulation results indicate that each circuits works properly under applying input signals before the implementation. This design was implemented and applied to different pulse width from 100 μs to 9999 msec. The measurements in the millisecond range had not any deviation from the setting pulse. The measurements in the microsecond range had small deviation from the setting pulse ± 1%. The second way has a good accuracy blew 100 μs in expense of the limited amplitude just TTL level.

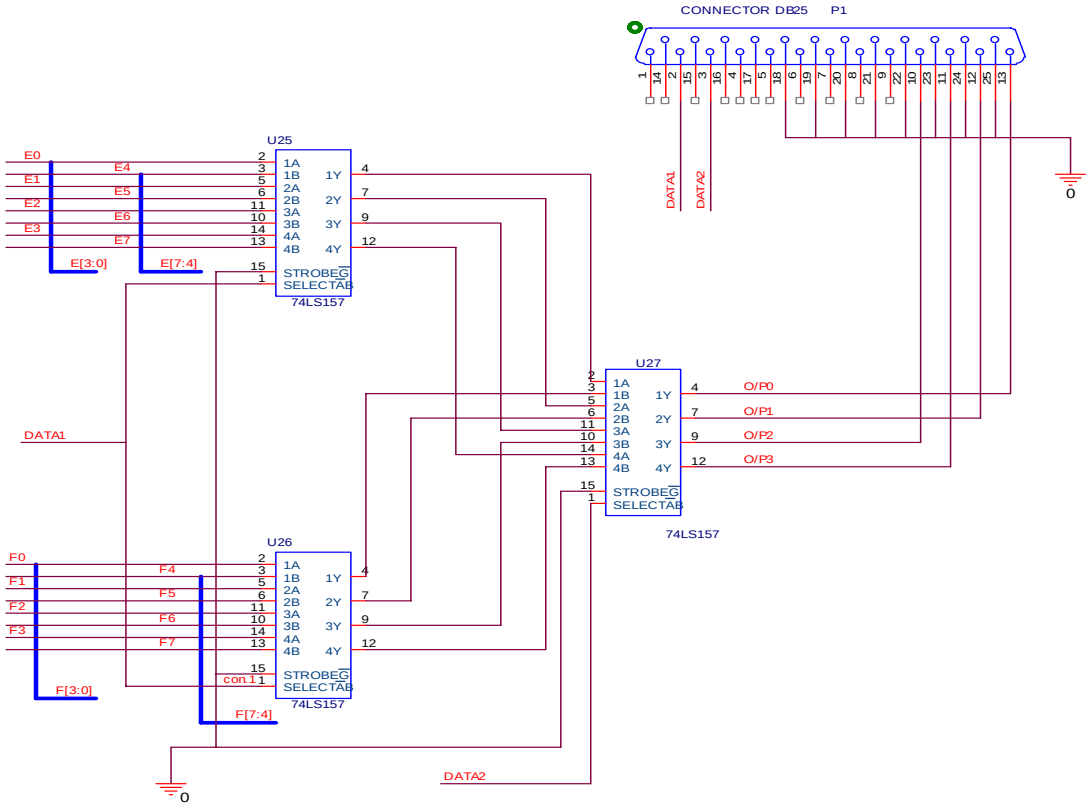

Fig. 12. Circuit diagram of the computer interface.

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