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# An AC Current Limiting and Interrupting Device for Low Voltage Systems

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## ABSTRACT

This paper describes the development of the hybrid fault current limiter and interrupting device (HCLID) which can be used successfully as a fast short-circuit protection means for low voltage AC industrial installations. The main components of the HCLID are a solid state commutation circuit that can supply a counter current injection from a stand-by pre-charged capacitor, saturable core reactor as the limiting impedance and fast mechanical contact switch all connected in parallel. Through this study, we can present a significantly improved and simplified approach that replaces the half-controllable silicon-controlled rectifier (SCR) in the commutation circuit with self-turn-off device such as integrated gate-commutated thyristor (IGCT). The use of high-performance semiconductors (IGCTs) as the commutating affords reduced recovery voltage, reduced losses, improved reliability and dynamic performance, and fast switching time (in μs). The new approach involves a fault detection using rate of current rise rather than the current magnitude and a time delay operating characteristic based on Piecewise Linear Electrical Circuit Simulation (PLECS) program. The control method is very simple. Simulations carried out during the research. Simulation results proved the practicability and validity of the new HCLID.

**Keywords:** Hybrid Current Limiting Interrupting Device, Self-Turnoff Device, Fast Mechanical Contact Switch, Control Strategy, PLECS package application.

## 1. INTRODUCTION

Saving electrical energy is considered to be one of the most important fields of technical developments. It is widely recommended either directly or indirectly. The increase in the demand and consumption of the electrical energy leads to increase the levels of system faults. It is difficult to change the rating of the equipment and devices in the system or circuits to accommodate the increasing fault currents. The cost of equipment like circuit breakers and transformers in power grids is very expensive. To protect the expensive equipment and devices in power systems from the increasing fault currents, Fault Current Limiters (FCLs) provide more cost-effective solutions to save such equipment and devices.

Several devices to limit the fault current have been proposed in recent years. Among these devices, the electronically controlled fuse, that can be used to interrupt the fault current before the first peak. The need of replacement after every operation is a major drawback which make them incompatible with HV system. [1]. Classical circuit breakers can limit fault current using speed of operation and magnetic effect on arcing [2]. However, Classical circuit breakers with high-current interrupting capabilities are bulky and expensive electromechanical systems.

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The superconducting fault current limiter (SFCL) has been noticed as one of the successful ones to solve fault current problem, because of its fast fault current limiting, compact design and high efficiency even including refrigeration penalty, but it hasn't a fast recovery time, which makes them difficult to use if the protected power circuit require autoreclosure. [3,4].

With the development of high-power semiconductor technology, such as new thyristors with higher voltage and higher current ratings, efforts have been made to develop an effective solid state circuit breaker and fault current limiter [5-7]. The Solid-State Circuit-Breaker (SSCB) offers a quick and arcless operation. There are no moving parts and or contact arcing wear, hence the number and the speed of operations are not limited. However, large loss and limited power in the current power electronic elements still exist.

In order to avoid aforementioned issues, this paper will address a new approach of the fault current limiter. The main objective in this approach is to develop a hybrid current limiting and interrupting device (HCLID) which can be used successfully as a fast short-circuit protection means for low voltage AC industrial installations. Through this study, we can present a significantly improved and simplified approach that may replace the expensive and higher power losses of power semiconductors included in fast switching elements such as Integrated Gate-Commutated Thyristor (IGCT). Compared to SCR- based hybrid FCL type, the proposed technique that is based on self-turn-off

device is superior. It is smaller in size, better in dynamic performance, and simpler in the control approach and circuitry. Topology and control strategies of the proposal HCLID are described in the full paper version. Simulation results are conducted in PLECS program and show that the suggested technique is successfully addressed to interrupt different short-circuit currents conditions at zero current contact separation.

## 2. STRUCTURES AND OPERATING PRINCIPLES OF HCLID

The configuration of the HCLID incorporated in a single-phase distribution network is shown in Fig.1. It consists of solid state commutation circuit, saturable core reactor, fast mechanical contact (main switch), and the energy absorb element (ZnO); all are connected in parallel. The commutation circuit, connected to the terminals A and B includes a single-phase half-controlled bridge-type scheme based on self-turn-off devices, such as IGCTs ($IGCT_1$, $IGCT_2$), diodes ($D_1$, $D_2$) and the branch with a pre-charged condenser $C_{Com.}$ and inductance $L_{Com.}$. The current limitation facility in the presented HCLID is based on the current-limiting element of saturable core reactor in series with the auxiliary switch. The mechanical contacts of the HCLID is actuated by power electronic circuit. The forced current zero can be coordinated with the instant of the auxiliary contact separation. Thus, a fast current interruption with no electric arc formation can be achieved.

The operating principle begins under normal operation, where the main contact is closed and carries the line current, while everything else is OFF. However when a fault occurs, the control circuit determines if the short circuit current exceeds a pre-set value $V_1$, at this time, the electrodynamic drive opens the main contact when a control signal has been applied to it from the control circuit. Once the main contact is open, the current is forced through the saturable core reactor during fault current limitation mode, the current limitation mode is able to limit the peak and RMS fault currents for a variety of fault current levels. The control system operates by comparing the magnitude of the current through the saturable core reactor with a reference value $V_2$. Once the compared value exceeds a certain preset value, two signals from the control circuit Fig. 2 will be conveyed simultaneously: one to switch the commutation circuit on and the other to initiate the auxiliary contact opening by electrodynamic drive.

The control method is able to discern the fault current if actual direction. As a result, the $IGCT_1$ or $IGCT_2$, is switched on, supposing that this current flows from to A to B, the $IGCT_1$, should be switched on. Then the commutation current $i_1$ in the auxiliary contact from the positive terminal of commutation capacitor $C_{Com.}$ through the diode $D_2$, will have an opposite direction to the fault current $i_f$. Then, the current summation through the auxiliary contact becomes zero. Between the instant of the main contact separation and the instant of the triggering of the commutation circuit, the currents $i_1$ and $i_{D1}$ as well as the currents $i_2$ and $i_{D2}$ are equal. Immediately after the instant of the triggering of the commutation circuit the currents $i_{D1}$ and $i_{D2}$ have profiles defined by a new rule. The diode $D_2$ now carries the fault current if that still increases, while diode $D_1$ carries the differential current ($i_c$- $i_f$) up to the instant of the current $i_c$ equal to the fault current $i_f$. At this time the diode $D_1$ turns off and the fault current $i_f$ reaches its maximum value and the recovery voltage appears across the mechanical switch, while the commutation capacitor $C_{Com.}$ is still charging. The voltages across the switch and the capacitor $C_{Com.}$ increase with time.

The selection of the commutation thyristor ($IGCT_1$ or $IGCT_2$) depends on the direction of the fault current $i_f$. Supposing that this current flows from B to A terminal (Fig. 1) the sequence of the events is similar to the sequence of events described above, only $IGCT_2$ will conduct instead of $IGCT_1$.

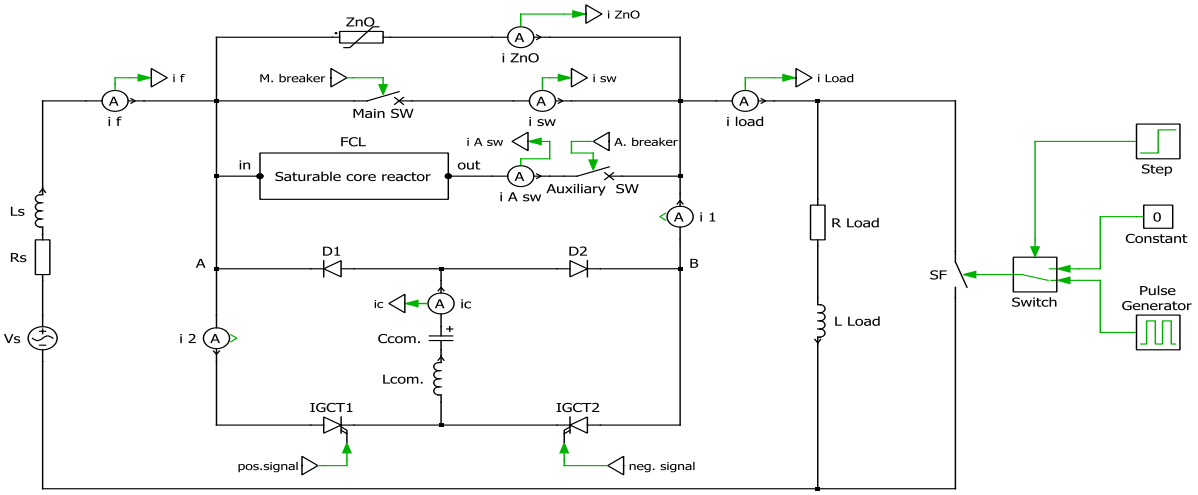


Fig. 1: HCLID circuit configuration

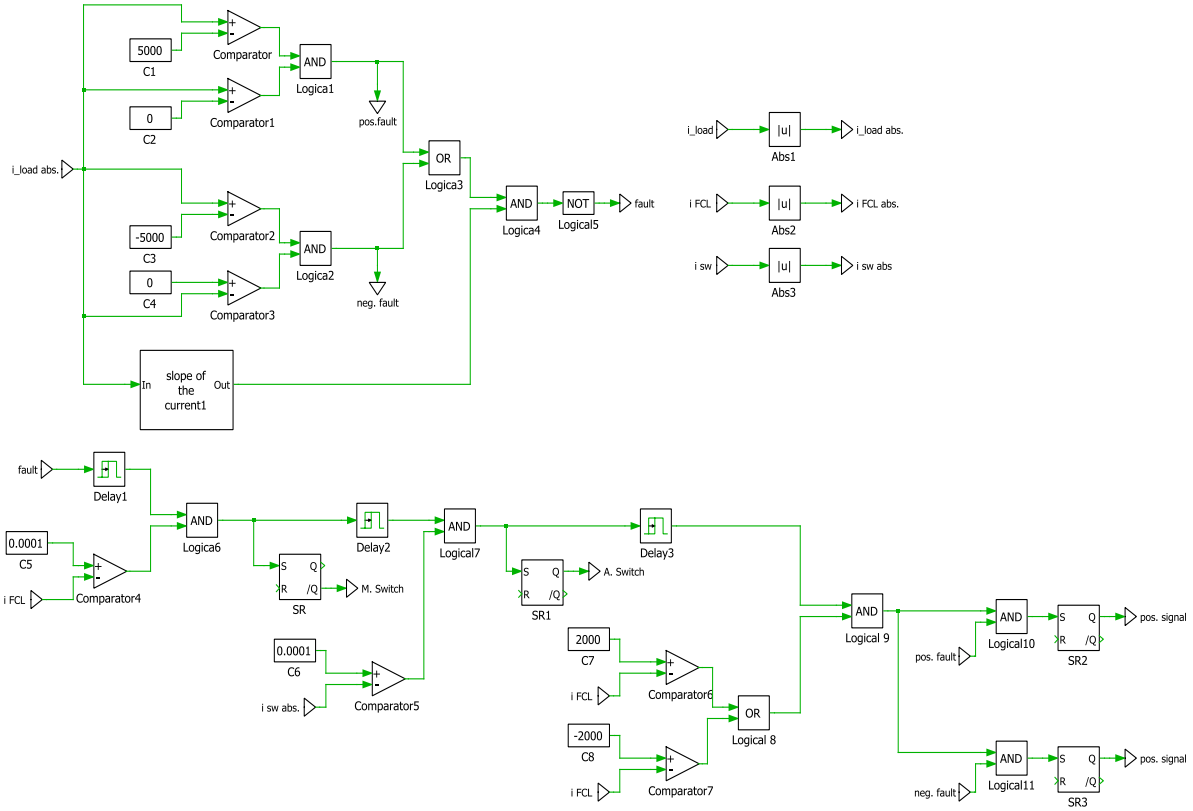


Fig. 2: Control algorithm implemented in PLECS program

## 3. CONTROL OPERATION

The controller algorithm is implemented in PLECS as standard logic blocks in the PLECS library [8]. The control circuit of the HCLID including short-circuit current detection system and gate signals to both the semiconductor switch and the electrodynamic drive to initiate the main and auxiliary contact is shown in Fig. 2. The control algorithm used in detecting the fault and maintaining the faulted state uses two key methods of detection. The first method of the controller, measured the load current as $i_{Load}$ and the absolute value of the measurement $i_{Load}$ is first compared to zero, to check if the fault current is in the positive or negative cycle of the current waveform. Also, this value is compared with tow arbitrary preset value, if the magnitude of the current exceeds this value, then a fault has occurred and the controller operates the HCLID as previously described.

The second method of detection, measures the slope of the fault current with comparison to normal current slope to verify if the current value is increasing. This ensures that the current is allowed to increase till it reaches a preset maximum value. At this instant the control circuit sends the appropriate signals to both the semiconductor switch and the electrodynamic drive.

There are six inputs to the controller but only three outputs to the HCLID which are the gate signals of the main contact, auxiliary contact and the commutation circuit. The six inputs are the load current $i_{Load}$, commutation capacitor current $i_c$, fault current limitation $i_{FCL}$, current through the main contact $i_{sw}$, $V_1$, and $V_2$. Each of these input signals are needed to properly operate the proposed HCLID control system. $V_1$, and $V_2$ are a pre-determined values. The output of control circuit is a logic signal that determines if the system is experiencing a fault or not.

Once a fault condition is determined from the short circuit current detection of the control algorithm, the correct order of operation is then set to separate the main switch.

Once the main switch is open, a verification of zero current through the mechanical contact is needed before turn on the auxiliary switch as shown in Fig.2. By waiting to triggering the commutation circuit until the current through the branch with saturable core reactor reaches to acceptable and safe value, the arc typically seen when opening up a breaker would be nonexistent thus lengthening the life of the mechanical contact switch. Also, the control strategy is able to discern the fault current actual direction and helps the fast mechanical switch to separate contact in a fixed time at all fault inception angles.

# 4. PARAMETER DESIGN AND OPTIMIZATION

### A. OVERVIEW OF THE SWITCHING ELEMENT AND SELECT THE SUITABLE SWITCH

The HCLID has set of requirements that must be met by choosing a suitable switching device to make the HCLID capable of delivering the stated performance (limiting and interrupting the fault current safely). The desirable features for the solid-state switches are as follows:

- High blocking voltage;
- High continuous current capability;
- Low on-state voltage drop ;
- Low conduction loss;
- High switching speed and low loss;
- Suitable control technique and thermal management;

Many power semiconductor devices have been developed for the HCLID applications such as; the insulated gate bipolar transistors (IGBT), SCR, gate turn-off (GTO) thyristor, emitter turn-off thyristors (ETO), and integrated gate-commutated thyristors (IGCT) [9]-[10]. These devices offer some improved characteristics compared with earlier conventional silicon devices

For high power applications, traditionally, a high power SCR is used in [9] as the symmetrical power semiconductor device for a FCL. The operation of the SCR in a solid state FCL has advantages over others in multioperation capability, lower voltage drop, lower cost and higher reliability. However, SCRs does not have the forced turn-off capability. Besides, and due to low switching frequency, the dynamic performance is low and a large filter is needed to attenuate the harmonics.

The Insulated-Gate Bipolar Transistor (IGBT) [10] has desirable qualities such as fast switching time, high reliability, voltage controllable, and has low gate drive power consumption. However, IGBT works in a transistor mode during on-state, and has a high conduction loss comparing with the GTO type devices.

For high-voltage and current applications, the GTO has been the dominate choice for a fully controllable semiconductor switch due to its large current and offstate voltage capabilities. This device can be turned off through its gate controls at any time during the period of operation. This function is a desirable characteristic for fault current limitation and circuit breaker action. However, it has a limited switching frequency and high switching losses and require a complex gate drive circuit. [11]

With the emergence of the Integrated Gate Commutated Thyristor (IGCT) [12], these drawbacks have been overcome. By combining the high blocking voltage ratings of the thyristor and blocking current with high reliability of the transistor, IGCT is thought to have low on-state voltage drop, low conduction loss, and fast switching times (within μs). The Present high power asymmetric IGCT devices are applicable to the proposed FCLs. The available IGCT device with the maximum voltage and current ratings is made by ABB and can be chosen as $IGCT_1$ and $IGCT_2$ of the HCLID shown in Fig. 1. The type is 5SHY 35L4510. The main parameters of the IGCTs are listed in Table 1 [13].

Table1. The main rating of the OF5SHY 35L4510 IGCT

| Symbol | Parameters | Value |
|---|---|---|
| $V_{DRM}$ | Repetitive peak off-state voltage | 4500 V |
| $V_{DC\text{-}link}$ | Permanent DC voltage | 2800 V |
| $I_{TGQM}$ | Max. controllable turn-off current | 4000 A |
| $I_{T(AV)M}$ | Max. average on-state current | 1700 A |
| $I_{T(RMS)}$ | Max. RMS on-state current | 2670 A |
| $di/dt_{max}$ | Max. rate of rise of on state current | 200 A/μs |
| $V_{FO}$ | Device blocking voltage | 1.4 V |
| $r_F$ | On-resistance | 0.032 mΩ |

The most significant parameters for selection are $V_{DClink}$, $I_{TRMS}$, and $I_{TGQM}$. The maximum rate of rise of on state current $di/dt_{max}$ is a very important parameter for the safety of IGCT devices, this is usually specified in the IGCT data sheets. IGCTs are used predominantly as snubberless devices in high-frequency PWM applications, so dv/dt do not deserve to be considered.

### B. SELECTION OF THE COMMUTATION PARAMETER $\{L_{Com.}, C_{Com.}, V_{Com.}\}$

The general idea is to interrupt the fault current at or close to zero current cross-over. In AC circuit the phenomena occur periodically twice at each cycle. A forced zero before the natural one can be done by the use of commutation principle. This method is based upon the superposition of an auxiliary oscillatory current on the fault current so that an artificial current zero can be obtained. It gives the circuit breaker a chance to interrupt the fault current before the peak of the first half cycle.

The commutation principles are described whereby the current in the main circuit is brought to zero by a commutation from a pre charged capacitor. The counter current injection from the commutation capacitor current is also used to produce a rapid extinction of arcs established between the mechanical contacts of the HCLID.

The commutation circuit parameters drastically influence the HCLID behavior. The parameters of the commutation circuit should be selected according to the critical fault inception angle.

The aim of this section is to prove that it would be able to be a very effective limitation of fault currents in the AC mains, at fault clearance time less than a fault period of line frequency and without generation of excessive switching over voltage. The required features of the HCLID can be achieved by the proper selection of the counter current injection

circuit (commutation circuit) $L_{Com.}$, $C_{Com.}$, $V_{Com.}$ by the use of a fast drive to open the main contact.
The most significant parameter of the commutation circuit and the optimal value of these parameters can be obtained as follows [14]:

$$L_{Com.}C_{Com.} = \left\{ \frac{(t_2 - t_1)}{\arcsin\left(\frac{1}{2}\sqrt{3 - \frac{A_2}{A_1}}\right)} \right\}^2 \quad (1)$$

$$V_{Com.}C_{Com.} = A_1 \frac{(t_2 - t_1)}{\left(\frac{1}{2}\sqrt{3 - \frac{A_2}{A_1}}\right)\arcsin\left(\frac{1}{2}\sqrt{3 - \frac{A_2}{A_1}}\right)} \quad (2)$$

Here, $A_1$ and $A_2$ are arbitrary constants;

$$A_1 = I_{cm}\sin\{\omega_{Com}(t_2 - t_1)\}$$

$$A_2 = I_{cm}\sin\{\omega_{Com}(t_4 - t_1)\}$$

Where,

$$I_{cm} = \frac{V_{Com.}}{\sqrt{(L_{Com}/C_{Com})}}, \quad \omega_{Com} = \frac{1}{\sqrt{(L_{Com}.C_{Com})}}$$

Where,
$L_{Com.}$: Commutation inductance,
$C_{Com.}$: Commutation capacitance,
$V_{Com.}$: Commutation capacitor initial voltage ,
$t_1$: Time of triggering commutation circuit,
$t_2$: Auxiliary contact separation starts,
$t_4$: Final fault current interruption and end of the recovery voltage,
$I_{cm}$: Maximum value of the capacitance discharge current,
$\omega_{Com}$: Commutation frequency,

The most critical parameter that has a complex effect on the current interruption process is the value of the commutation inductance which can be determined by the Eq. 1

The capacitance and the maximum stored energy within the commutation capacitor from the Eq.2 determined mainly the cost of the HCLID. Commutation capacitance has great effect on the capacitor discharge current, let through current, recovery voltage and maximum capacitor charge voltage. The maximum value of the capacitor discharge current, diode $D_1$ current and the let through fault current are directly proportional to the increase of initial voltage across the commutation capacitance.

## 5. SIMULATION RESULTS

In order to verify the validity of the proposed HCLID, Simulations based on PLECS program for the circuit shown by Fig.1 are accomplished. The normal current through the system is 200 A, as shown in Fig. 3, when the fault occurs at 0.04 sec, the prospective fault current in the system reaches 50 kA due to the fast transient and the inductive load in the system. The magnitude of the fault current and voltage greatly exceeds the power requirements of any devices operating in the system and justifies a need for a CLID to be placed for protection.

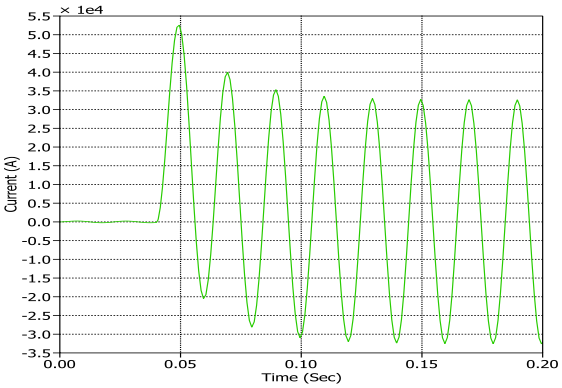

Fig. 3: Prospective fault current

The simulation parameters are given in table 2 and the parameters of the commutation circuit have been chosen to provide a safety HCLID critical parameters corresponding to critical fault inception angle in order to ensure safe current breaking over all ranges of angles of circuit breaker operations. This angle is measured between that the source voltage zero after which the positive voltage sine half wave has taken place and the instant of the short-circuit commencement.

The inception angle has a great effect on the rise rate (di/dt) and the peak value of the fault current**.** The effect of the inception angle on the critical HCLID current, voltage and time under ideal commutation principle are shown from Fig. (4 to 9). There are shown: the current and voltage wave-forms at (0, 90, and 170) ele. degree inception angle. The operation of the HCLID is simulated at these values of the inception angle and other angles. However, these values are presented only because they give a complete idea about the circuit breaker operation.

It has been found that there are some factors that have a great effect on HCLID operation like voltage source phase angle during fault condition, discrimination current, pre arcing time and time before appearing the recovery voltage across the mechanical contacts. The parameters of the commutation circuit are very sensitive to these parameters.

Table2. Parameters of the HCLID for simulation

| Parameter | Value |
|---|---|
| Source voltage $V_s$ | 220 $V_{RMS}$ |
| Source resistance $R_s$ | 0.147 mΩ |
| Source inductance $L_s$ | 5e-6 H |
| Load resistance $R_{Load}$ | 0.453 mΩ |
| Load inductance $L_{Load}$ | 8e-6 H |
| Commutation inductance $L_{Com.}$ | 5.2e-6 H |
| Commutation capacitance $C_{Com.}$ | 5e-3 F |
| Commutation capacitor initial voltage $V_{Com.}$ | 528 V |
| Frequency F | 50 Hz |

### A. EFFECT OF THE INCEPTION ANGLE ON HCLID OPERATION WITHOUT ZnO

The current and voltage wave-forms of the HCLID simulation under ideal commutation Principle presented in Fig. 4, Fig. 5 and Fig. 6 respectively**.** The HCLID are sustained to the maximum value of let-through current, commutation time and the time before appearing of the recovery voltage across the mechanical switch at inception angle 0, 90 degree. In these simulations we can notice that the maximum value of let-through current and minimum value of the time before recovery voltage occur at 90 degree; minimum value commutation time and maximum value of current diode D1 occur at 0 degree. The maximum value of the recovery voltage and capacitor discharge voltage occur at 90 degree because the maximum amplitude of the fault current is for the power factor cos φ = 0 and for the inception angle 0 degree. On the other hand the maximum initial rise rate of the fault current (di/dt) occurs for cos φ =0 and the inception angle 90 degree

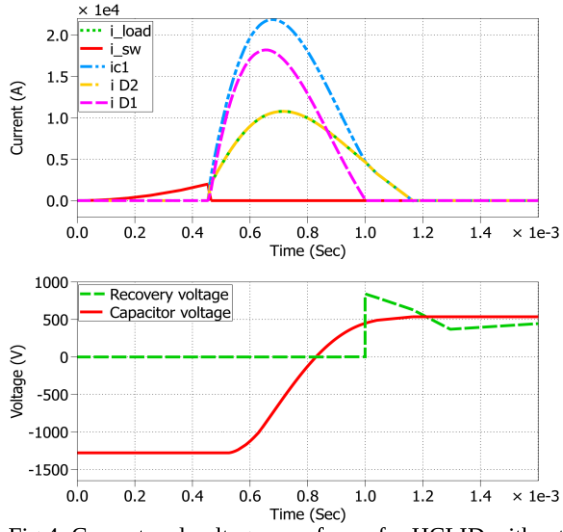


Fig.4: Current and voltage wav-forms for HCLID without ZnO at 0 ele. degree inception angle.

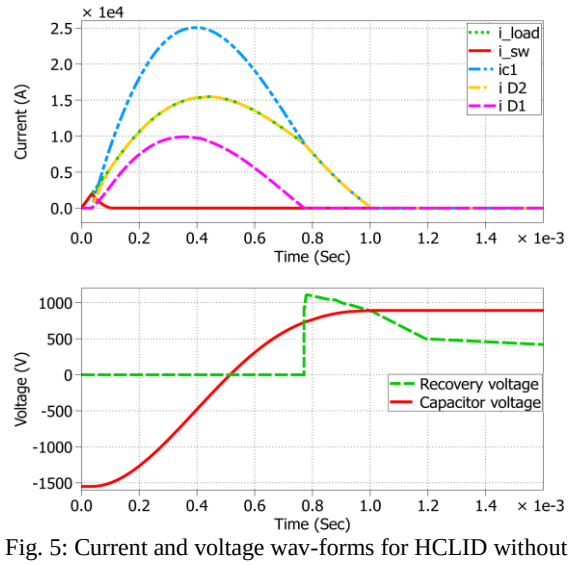


Fig. 5: Current and voltage wav-forms for HCLID without ZnO at 90 ele. degree inception angle.

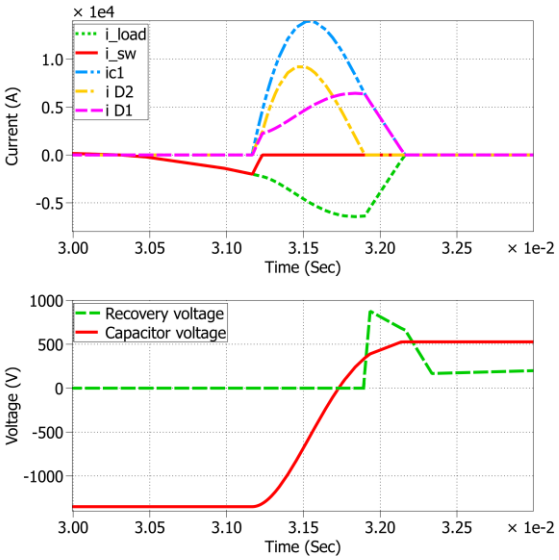


Fig. 6: Current and voltage wav-forms for HCLID without ZnO at 170 ele. degree inception angle.

### B. EFFECT OF THE INCEPTION ANGLE ON HCLID OPERATION WITH ZnO

In the design of an HCLID a special attention should be paid to the value of the recovery voltage and capacitor charge voltage at current breaking. The recovery voltage across HCLID should be limited to a level less than three times of the source voltage.

ZnO varistor is used across the main contacts of HCLID to clamp the recovery voltage if it is needed. The current and voltage wav-forms for HCLID using ZnO at (0, 90, and 170) ele. degree inception angle under ideal simulation have been shown in Fig. 7, Fig. 8 and Fig. 9 respectively. From these figures we can notice that the amplitudes of the maximum recovery voltage across the mechanical contacts and the maximum recharging capacitor voltage can be decreased in comparison to HCLID without ZnO at the angle 90 degree. While they have reached the minimum value at the angle zero degree. Therefore, the ability of the HCLID to withstand the maximum recovery voltage should be tested at the critical 90 angles. The inception angle 170 degree represent the ability of the HCLID to interrupt the fault current near the end of half cycle.

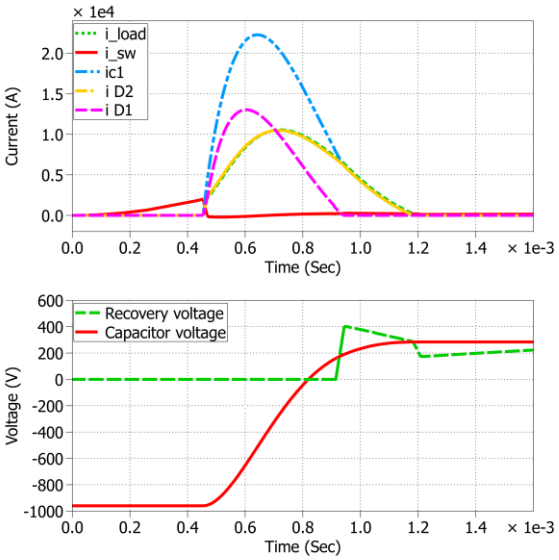


Fig. 7: Current and voltage wav-forms for HCLID with ZnO at 0 ele. degree inception angle.

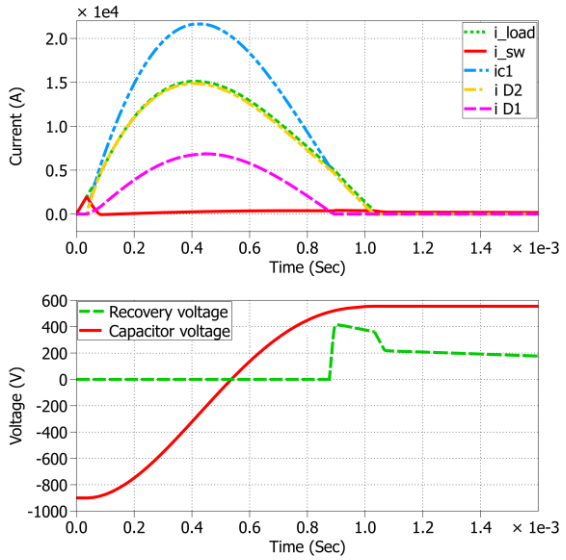


Fig. 8: Current and voltage wav-forms for HCLID with ZnO at 90 ele. degree inception angle.

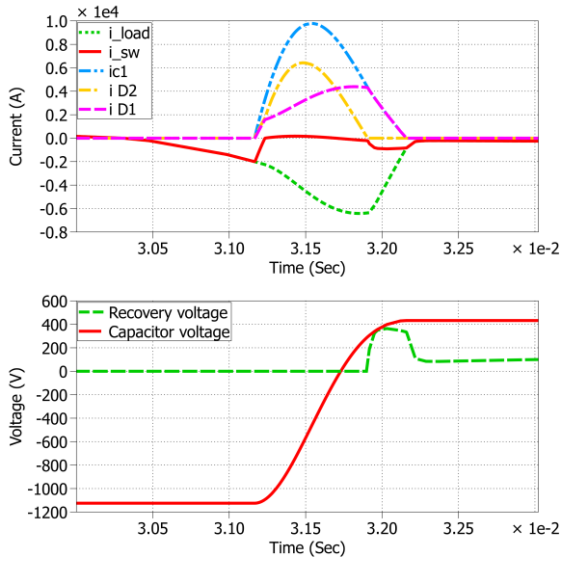


Fig. 9: Current and voltage wav-forms for HCLID with ZnO at 170 ele. degree inception angle.

### C. EXEMPLARY DATA OF COMPARISON THE OPERATION WITH AND WITHOUT ZNO

The purpose of the compensation is so to obtain the effects of the commutation circuit parameters $L_{Com.}$, $C_{Com.}$ and $V_{Com.}$ in the fault currents interruption process. This leads to investigate the optimum values of the commutation circuit parameters. Many simulation for both controlling techniques with and without using some defined ZnO at 50 $kA_{RMS}$ prospective fault current and different values of inception angle have been done. Exemplary results of simulations using ideal commutation parameters are shown in table 3.

Table3. Exemplary data of comparison the operation with and without ZnO

| Element of comparison | Operation without ZnO | Operation with ZnO |
|---|---|---|
| **Simulation results at 0 ele. degree inception angle.** | | |
| Commutation capacitor $C_{Com}$ (mF) | 8.7 | 6.2 |
| Recovery voltage (V) | 839 | 410 |
| Maximum capacitor charging voltage (V) | 1326 | 950 |
| Current diode $I_{D1}$(A) | 1.82e4 | 1.31e4 |
| **Simulation results at 90 ele. degree inception angle.** | | |
| Commutation capacitor $C_{Com}$ (mF) | 10.26 | 5.96 |
| Recovery voltage (V) | 1112 | 415 |
| Maximum capacitor charging voltage (V) | 1550 | 900 |
| Current diode $I_{D1}$(A) | 9.9e3 | 6.86e3 |
| **Simulation results at 170 ele. degree inception angle.** | | |
| Commutation capacitor $C_{Com}$ (mF) | 8.87 | 7.44 |
| Recovery voltage (V) | 876 | 365 |
| Maximum capacitor charging voltage (V) | 1340 | 1124 |
| Current diode $I_{D1}$(A) | 9.18e3 | 6.42e3 |

As depicted from the table, without a ZnO varistor the recovery voltage across the main contacts and the capacitor charging voltage is increased. The recovery voltage is culminated up to three times of the supply voltage while the capacitor charge voltage is culminated up to two times of the initial starting voltage across the capacitor. In addition, the maximum value of let-through current, recovery voltage and capacitor discharge voltage occur at 90 ele. degree. While the minimum value commutation time and maximum value of current diode $D_1$ occur at 0 degree. The inception angle 170 degree represent the ability of the HCLID to interrupt the fault current near the end of half cycle.

## 6. CONCLUSIONS

A new concept of HCLID has been studied and developed on the base of a combination of high-performance semiconductors (IGCTs) and of a fast-opening mechanical switch by substituting the half-

controllable SCR in the commutation circuit with self-turn-off device such as IGCT. The use of high-performance semiconductors (IGCTs) as the commutating affords reduced leakage current, reduced losses, improved reliability, and fast switching time (in μs). The new approach involves a fault detection using rate of current rise rather than the current magnitude and a time delay operating characteristic based on PLECS program. The control strategies of the proposal FCL are described. Simulations under which short circuit fault mode were carried out. Results proved the practicability and validity of the new HCLID.

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