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Design and Implementation of Digital-Up/-Down Frequency Converters

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Abstract:

Due to the increasing complexity in modern communication systems, State of the art data communication systems make extensive use of digital hardware. Besides baseband digital processing, the frequency tuning function is now being shifted from analog to digital implementation where the integration, cost, and case of programming are the primary motivations.

In this paper, a proposed technique for implementation of Digital Up Converter (DUC) and Digital Down Converter (DDC) is presented. The objectives are achieving an optimized and cost effective hardware implementation. The diverse hardware requirements for these systems including processing speed, flexibility, integration and time-to-market necessitate an FPGA based implementation platform.

Keywords:

Signal Processing, digital Communication, Up and Down Frequency Converters

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1. Introduction:

Recent advances in integrated circuit (IC) fabrication technology, particularly CMOS coupled with advanced DSP algorithms and architectures, are making possible single-chip all-digital solutions to complex communication and signal processing subsystems. In most communication systems Digital-Up/-Down Conversion (DUC/DDC) is the main process. The conversion process must support different wireless standards and bandwidths. The wideband communication standards, where a high number of narrow band channels are accommodated in the band, posses a formidable challenge to achieve low cost, small size, light weight, and efficient power consumption, especially to DSP processor-based designs [1].

In [2], an efficient way of performing decimation and interpolation based on a class of FIR prefiltering techniques for multirate applications was introduced by E. B. Hogenauer. It proposed the Cascaded Integrator-Comb filters (CIC filters), that work very well in practice. However in case of large rate changes, the proposed technique requires very narrow band filters, which is hard to be achieved. An extension of CIC filters has been published in [3] that showed a modified CIC architecture which provides significantly improved performance over the traditional CIC approach at very little extra cost. In 1991, H. Samueli and T. Lin [4] had implemented a high-performance decimating digital filter using recirculating halfband filter architecture of high-order decimation / interpolation filter consists of a polyphase implementation of a halfband filter, where the output data can be recirculated to the filter's input. In [5], a programmable high-order decimation/interpolation filter is introduced.

This paper presents an alternative to the traditional digital frequency conversions architectures. The proposed architecture achieves low power as well as high speed operation. A multirate filtering approach is used, which is applicable for both up conversion and down conversion of data.

The paper is organized as follows. In section 2, an overview of the whole system description is introduced. In section 3, the implementation of the proposed technique is presented. In section 4, a brief concern the design simulation is included. Section 5 is the conclusions.

2. System Description:

The basic modules for DUC/DDC are the Cascaded Integrator-Comb (CIC) filters. The CIC filter architecture is based on a class of FIR prefiltering techniques for multirate applications proposed by Hogenauer [6]. A CIC filter consists of two main sections: an

integrator section which is a cascade of N integrators, and a comb filter section which is a cascade of N comb filters. It performs as a CIC interpolation filter with interpolation factor R in the DUC module, and a CIC decimation filter with decimation factor R in the DDC module. Figures 1.a and b show the cascaded structure of both DUC and DDC with a rate change switch of factor R, and the associated transfer function.

(a) CIC interpolation filter.

(b) CIC decimation filter.

Figure (1): The block diagram of; (a) CIC interpolation filter, and (b) CIC decimation filter.

Both comb filters in the interpolator and decimator units operates at lower frequency compared to the integrator having the transfer function $H_c(z) = 1 - Z^{-R}$.

The general transfer function of the CIC filter is given by:

$$H(z) = \left\{ \frac{1 - Z^{-R}}{R(1 - Z^{-1})} \right\}^{N} \qquad (1.a)$$

and the frequency response of the CIC filter may be expressed as:

$$H\left(e^{j\omega}\right)=\left\{\frac{\sin\left(\frac{\omega R}{2}\right)}{R\sin\left(\frac{\omega}{2}\right)}e^{-j\omega(R-1)/4}\right\}^{N} \qquad (1.b)$$

Equations 1.a, and b describe a linear-phase filter with a lowpass sin(Rx)/sinx characteristic for the CIC filter. Both have nulls at integer multiples of (*1/R*)Fs, where F_S is the high-rate sampling frequency, and thus, the frequency bands that are aliased into the desired baseband signal by the interpolation or decimation operation centered around nulls, providing "natural" alias-rejection. Figure 2 shows the normalized frequency response for a single-stage (N=1) CIC filter with a decimation factor of R=8.

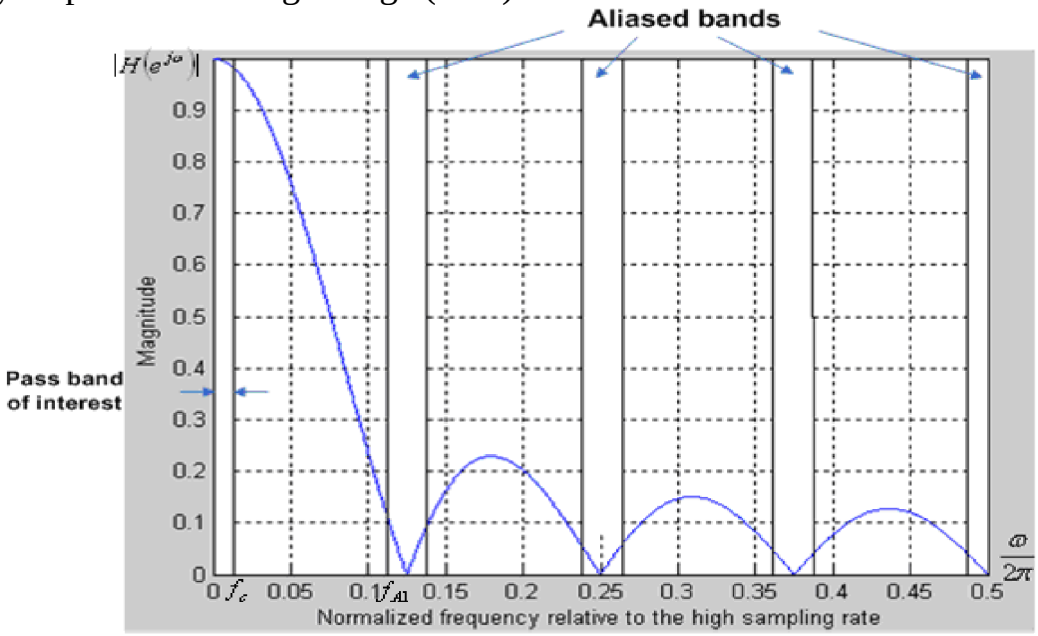


Figure (2): Single-stage CIC decimation filter frequency response for R = 8.

The next CIC architecture is based on a technique for sharpening the response of a filter proposed in [3]. This technique attempts to improve both the passband and stopband of a symmetric nonrecursive filter by using multiple copies of the same filter. In the simplest case, the sharpened filter $H_{sharp}(z)$ can be related to the original filter $H(z)$ by:

$$H_{sharp}(z)=H^{2}(z)[3-2H(z)] \qquad (2)$$

The block diagram of a sharpened filter is shown in Figure 3. Its implementation requires three copies of the original filter, scaling multiplier of value 3, trivial multiplier of value 2, adder, and delay line to equalize the group delay through the two channels in the first part of the structure. If the original filter is chosen to be a single-stage CIC filter, the resulting sharpened filter will have significantly reduced passband droop and improved alias rejection.

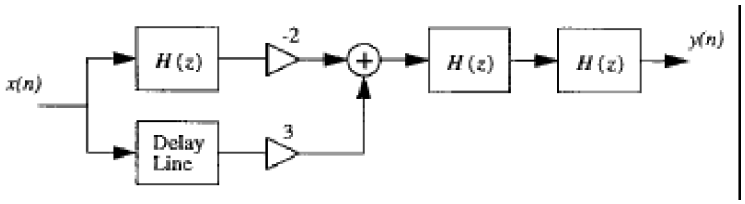


Figure (3): The block diagram of a sharpened filter.

The frequency response of the sharpened CIC decimation filter is expressed as:

$$H\left(e^{j\omega}\right)=\left[3\left(\frac{\sin\frac{\omega R}{2}}{R\sin\frac{\omega}{2}}\right)^{2N}\right]-\left[2\left(\frac{\sin\frac{\omega R}{2}}{R\sin\frac{\omega}{2}}\right)^{3N}\right] \quad (3)$$

which is restricted by factor R equals 2^i, where i is an integer.

The above structures can be employed in digital transceivers as shown in Fig.4. The interpolator section is required to separate the original baseband digital signal from its images. By using the criteria of interpolation and decimation, we handle the digital base band signal and increase its sample rate by a specified interpolation factor, which is a great benefit in reducing the required coefficients since sharp cutting edges for the stop frequency need huge filter coefficient also increase the size of the hard ware implementation. The Direct digital synthesizer (DDS) is used for implementing DDC and DUC. It can be replaced in a simple system by a sine wave generator using the lookup table technique. The output of the DDS is mixed with the output of the CIC interpolator in the transmission section and with the output of the analog tuner in the receiver section.

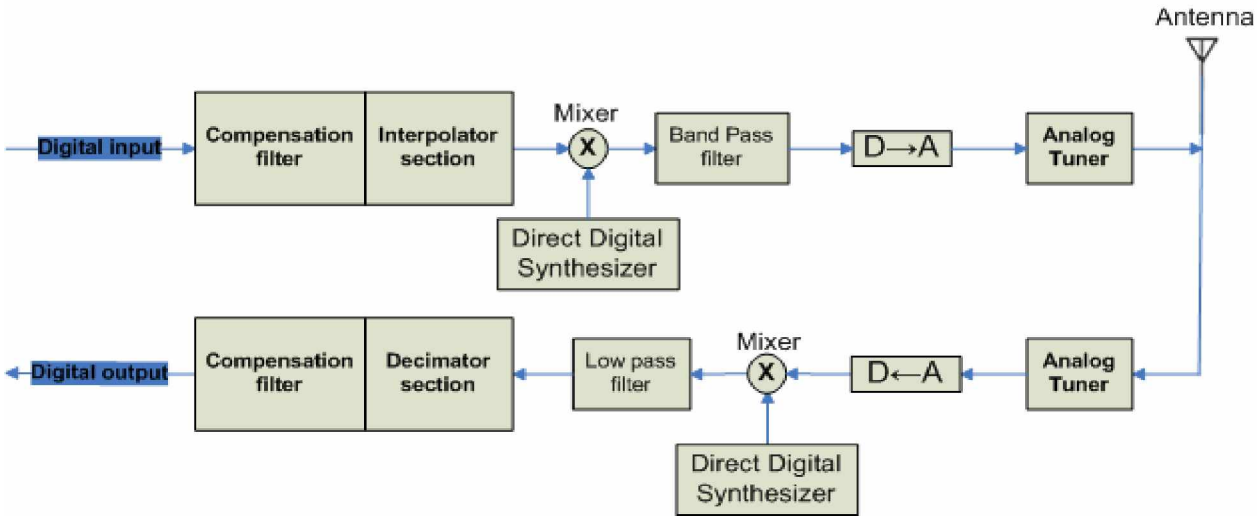


Figure (4): The overall block diagram of the digital transceiver unit.

Compensation filters are used to flatten the passband frequency response; e.g. for a CIC decimator the compensation filter operates at the decimated sample rate. The compensation filter provides $(x/\sin(x))^N$ shaping. For N = 3, and R = 64, Figure 5 shows the uncompensated CIC frequency response, the compensation filter frequency response, and the compensated CIC. Figure 6 provides an exploded view of the compensated filter passband. Similarly, the same technique was used with the CIC interpolator [7].

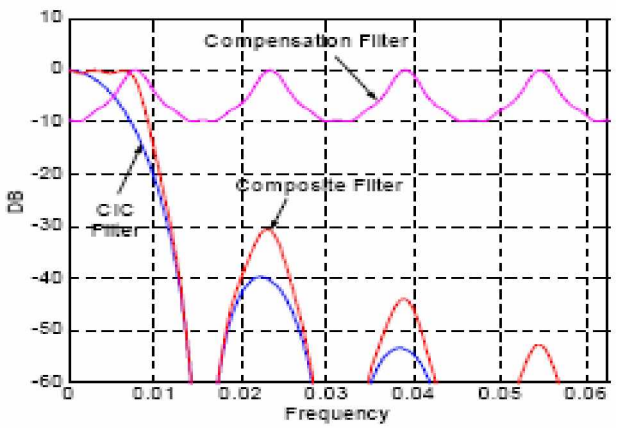


Figure (5): CIC compensation filter. N =3, R = 64.

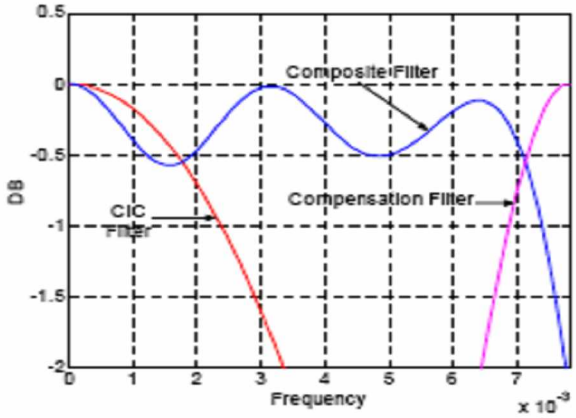
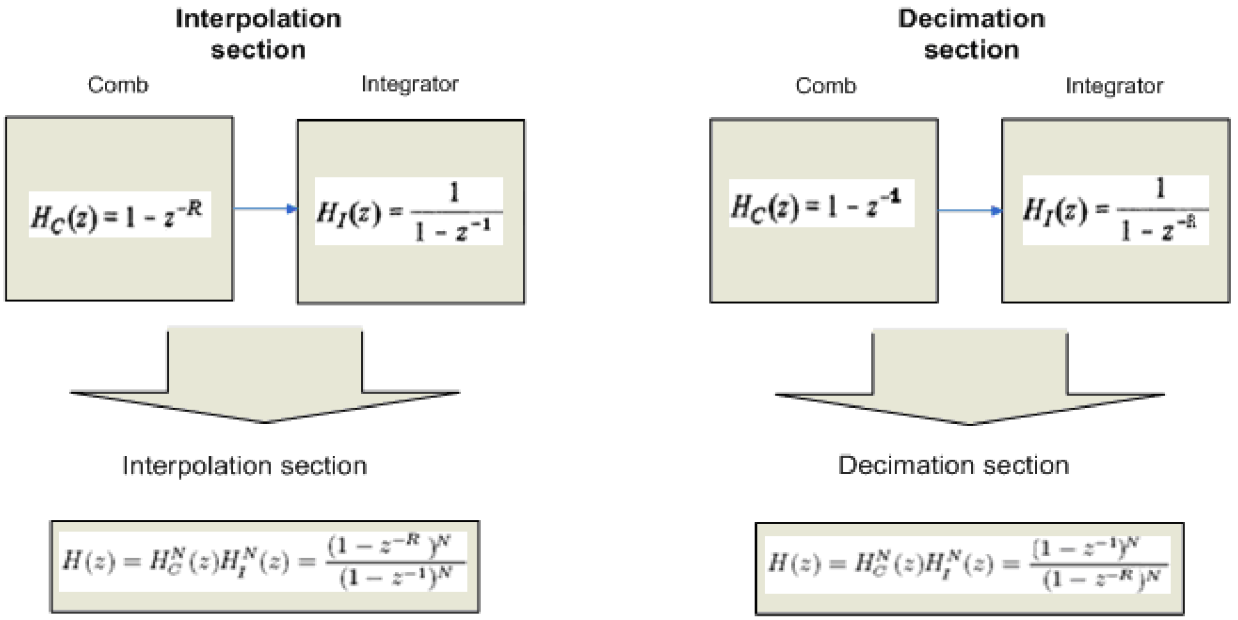


Figure (6): CIC compensation filter. N=3, R = 64. Passband response.

The proposed N-stages CIC filters for the interpolation and decimation process are shown in figure (7).

(a) Interpolation Section.

(b) Decimation Section.



(c) The general transfer function of the CIC filter.

Figure (7): The proposed design; (a) Interpolation Section block diagram, (b) Decimation Section block diagram, (c) The general transfer function of the CIC filter.

In figure 7, in case of interpolation, the sample rate is increased from F_{out}/R to F_{out} and again to F_{out}/R in case of decimation.

Both the interpolation and decimation process are synchronized using 2 different clocks (the system_CLK and the operating_CLK) related by the used factor R. This approach avoids the use of the rate change switch. It can be noted that the gain factor 1/R in the transfer function has been eliminated (compare to that in equation 1). Both the interpolation and decimation sections consist of N comb stages followed by N integrators. The clock of the integrators in the interpolation process is the system_CLK, while the clock in the comb sections is the operating_CLK. In the decimation process, the clock of the integrators and the comb section are exchanged compared to that of the interpolation process.

3. Design and Implementation:

This section is devoted to the design and implementation of digital transceiver of narrow baseband analog signal. Consider a system with IF frequency equals 10.7MHz and narrow baseband signal of width 50KHz. Assume that the 10.7MHz output signal of the DDS is represented by 32 sample/period, so the sampling rate of the DDS output is

342.4M Samples/sec that give rise to the necessary interpolation factor R equals 3420 in case of sampling the baseband at rate of 100K Samples/sec.

In the transmission section, as a result of the CIC interpolation process, the signal resolution before the mixer is 12-bit. Hence, the resolution of the DDS is selected to be 12-bit. The result may enforce the implementation to employ an expensive D/A converter with 24-bit resolution. An alternative to this approach could be the gain reduction or rounding technique. However, both are considered a source of noise that may reduce the overall performance. After the mixer, a simple bandpass filter is required to remove the harmonics of the mixer. This filter is designed using the FDA tool of MATLAB. An Equiripple bandpass FIR filter of order 20 provides a satisfactory performance in the system simulation as demonstrated in the next section.

In the receiver section, a 12-bit A/D converter is selected to provide the same resolution of the DDS. An Equiripple lowpass FIR filter of order 20 is used to remove the harmonics of the mixing process before the decimation process.

The lowpass and bandpass filters are generated in VHDL codes with schematic simulation. The bandpass filter has a worst case alias rejection of 75.86 dB, and the lowpass filter is of 78.92 dB. The design is tested on FPGA 4vfx12sf363-11 device on an evaluation board with 342 MHz clock frequency provided by built-in crystal oscillator. The following list shows the used resources of the device, and emphasizes the efficiency of the proposed design.

Device utilization summary:

Number of Slices	:	212	out of	6144	3%
Number of Slice Flip Flops	:	380	out of	12288	3%
Number of 4 input LUTs	:	224	out of	12288	1%
Number of bonded IOBs	:	14	out of	240	6%
Number of GCLKs	:	1	out of	32	3%
Number of DSP48s	:	3	out of	32	9%

4. Simulation results:

The simulation results have been developed in two different platforms. The first is the MATLAB using the tools of the simulink, while the second is the Modelsim of Mentor Graphics using VHDL and Verilog developed codes for the proposed DUC and DDC.

Using the simulink, Figure 8.a shows the sampled base output of a random generator with peak to peak in the range 15 to -15. The interpolated output by a factor R= 3420 is

shown in figure 8.b while the decimated one is shown in figure 8.c. It worth noting that the gain of the CIC process exceeds 1e8 in 3 stages that give rise to high amplitude of the interpolated signal. In addition, the gain reduction (suggested in the presented model in figure 1) may cause serious rounding and the original data retrieving becomes a difficult task.

Figure 9 shows the case of a sine wave sampled base signal. Obviously, a smooth sine wave is produced as a result of relatively high decimation factors that reduce significantly the bandwidth of the sampled signal.

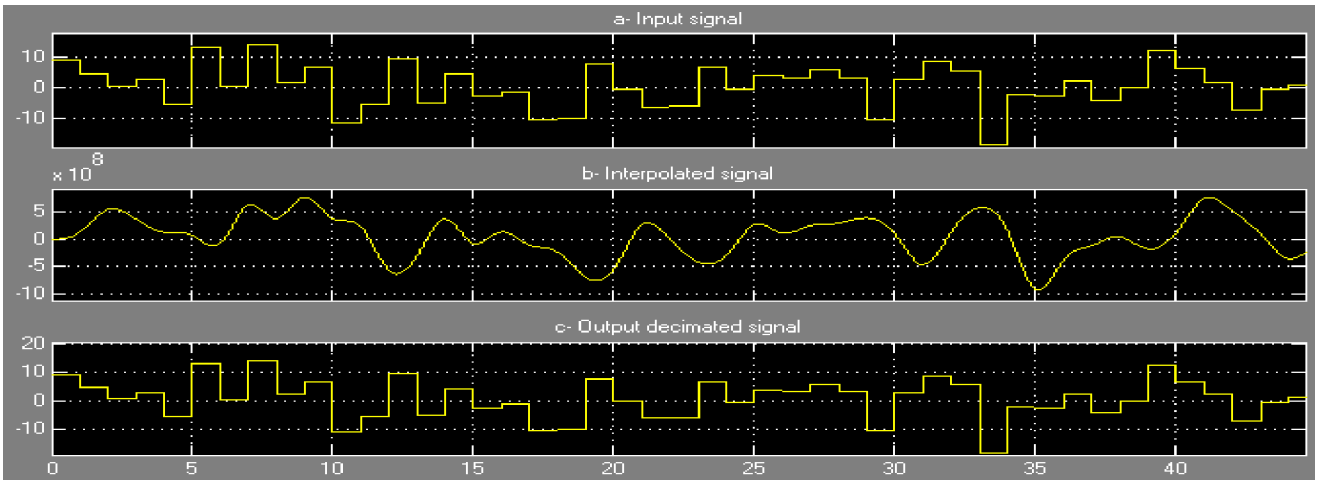


Figure (8): the CIC simulation of sampled base random signal; (a)Random generator sample based signal, (b)The interpolated signal by factor R=3420, (c)The decimated signal.

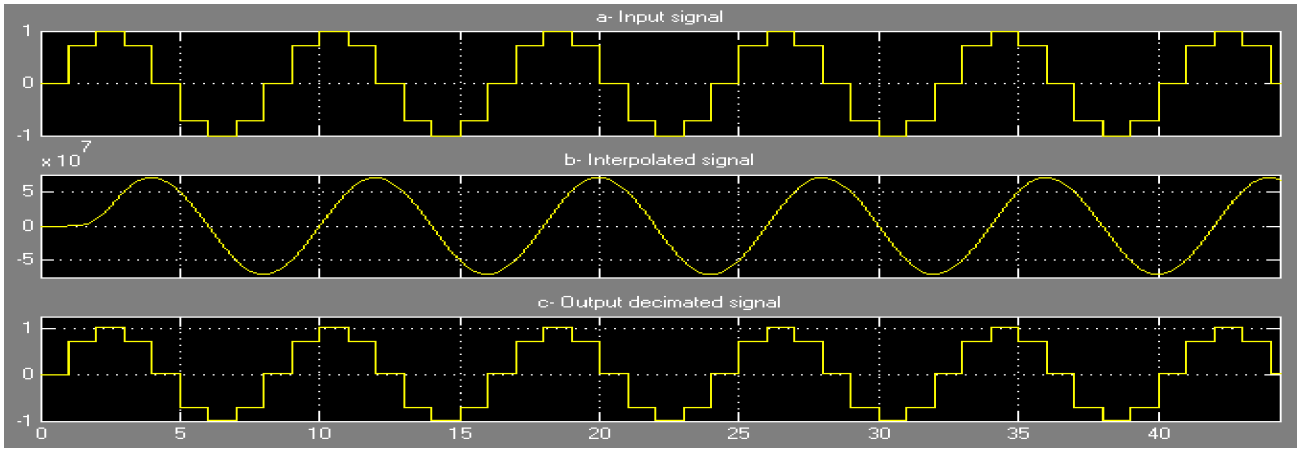


Figure (9): the CIC simulation of sine wave sampled base signal; (a)Sine wave generator sample based signal, (b)The interpolated signal by factor R=3420, (c)The decimated signal.

The VHDL and Verilog developed codes are verified and tested using the Modelsim. Figure 10 shows both the system CLK (Sys_CLK) and the operating CLK (operating_CLK); those are related by the factor R. It displays a random input signal (with a radix in decimal) and the final decimated output. It can be noted that the out put has been retrieved correctly after a delay interval measured by 6 operating_CLK. (one operating_CLK for each stage of the CIC interpolator and decimator).

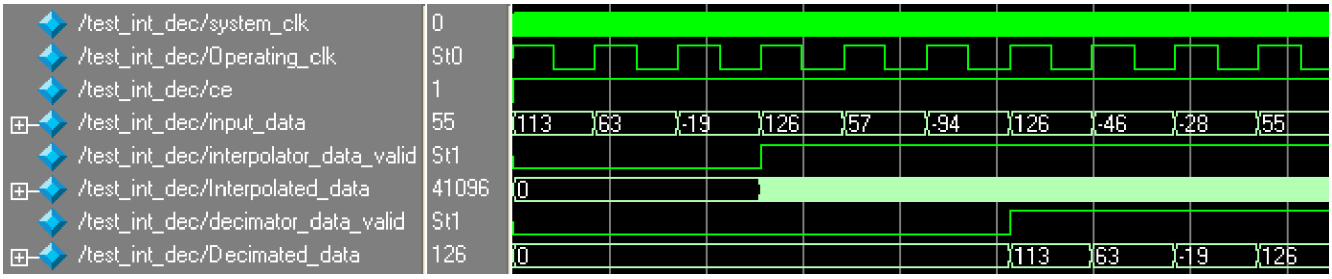


Figure (10): The wave default simulation behavioral model showing the input data, operating_clk, and output data (radix in decimal).

5. Conclusions:

The proposed CIC interpolating and decimating filter architectures enable an efficient implementation of DUC and DDC for single-chip solution of digital communication system. It retains the small-size advantages of the traditional multiplierless CIC approach and improves the performance by employing more stages. The CIC filters are implemented using a cascade of ideal comb stages operating at a high sampling rate and an equal number of integrator stages operating at a lower sampling rate. This approach eliminates the need for the rate change switch that affects the size of implementation.

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