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OVSF code generator using single OVSF code index

By

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Abstract:

Wideband code division multiple access (W-CDMA) system is adopted as the 3rd generation radio interface technology by 3rd generation partnership project (3GPP) [1]. In W-CDMA system, the orthogonal variable spreading factor (OVSF) code is the channelization code used for multiple accesses in the same slot as well as in the same cell. One of the most important characteristics of W-CDMA is the service flexibility, which can be supported by using OVSF codes for the channelization codes of the different users. In this paper, we propose hardware structure of W-CDMA frequency division duplex (FDD) and time division duplex (TDD) dual mode OVSF code generator using single code indexing method introduced in [2] with multi stage spreading scheme. The proposed algorithm has the advantages on memory size (reduce 98 %) and processing time (max. 32 %) compare to existing method.

Keywords:

OVSF, WCDMA, single code indexing, OVSF code generator

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1. Introduction:

In 3GPP, OVSF code is selected as the channelization code used for multiple access in the same slot [1]. OVSF code provides the orthogonal set of codes with variable spreading factors in order to support the variable data rates in code division multiple access (CDMA) based systems. Gilhousen proposed a method for allocating a set of OVSF codes for different data rates employing Walsh codes of variable lengths [3]. And code tree structure is also an useful alternative method to obtain OVSF code [4]. Those methods are based on the modified Hadamard transformation, and they need two indexes to indicate a spreading factor and a code number. In order to generate the OVSF code, conventional methods which based on the look-up tables (LUT) increase memory size and access time for the long code set. And we suggested single code index method to overcome various overheads [2].

This paper proposes multiage stage OVSF code generating method and describes the hardware structure. And the advantages of new structure are mentioned. In section 2, we introduce the conventional OVSF code generation method and Single code index method based on Kronecker product. Proposed method hardware structures are shown in section 3. The section 4 describes its advantage compare with existing method, and the section 5 provides some concluded remark.

2. OVSF code generator:

2.1 OVSF code tree structure

Let $C_{SF}(p)$ denote the OVSF code word with the spreading factor (SF) $SF = 2^L$, where L and P are the code number and the layer number. The codes are generated recursively from the code tree as shown in Figure (1) [4]. By definitions described in [3] and [5], the mother codes are the lower layer codes on the path from the specific code to the root code $C_1(0)$, and the descendent codes are those produced from the specific code. For examples, the mother codes of $C_8(2)$ is $C_4(1)$, $C_2(0)$ and $C_1(0)$, and the descendent codes of $C_4(1)$ are $C_8(2)$, $C_8(3)$ and their descendent codes. In here, mother code and descendent code are not orthogonal each other. It can be verified by correlation of two codes after generating both codes. And it means that memory size and comparing time are increased geometrically.

2.2 Single code index method

The tree-structured method can be interpreted by the recursive Kronecker procedure described as followings:

$$C_{2N}(p) = C_2(m) \otimes C_N(k) \tag{1}$$

with $p = 2 \cdot k + m$, where $k = 0,1,\ldots,N-1$, m = 0 or 1, and the initial codes are

$$C_1(0) = 1,\ C_2(0) = [1,\quad 1],\ C_2(1) = [1,\quad -1] \tag{2}$$

In this case, the OVSF code with the SF $N = 2^L$ can be factorized by the Kronecker product with L codes with their each SF 2. According to this property, the mother codes of $C_N(p)$ can be presented as Equation (3) with m = 2,3,..L. And we can apply exact code by using these property, multi stage spreading scheme.

$$C_N(p) = C_2(a_{L-m}) \otimes \ldots \otimes C_2(a_1) \otimes C_2(a_0) \tag{3}$$

And the descendent codes of $C_N(p)$ are all $C_M(q) \otimes C_N(p)$ with any M and q.

These properties can make possible to check orthogonality, just have to compare index code before generating OVSF code word. And long OVSF code word can be generated by expanding one code to the other codes using these properties.

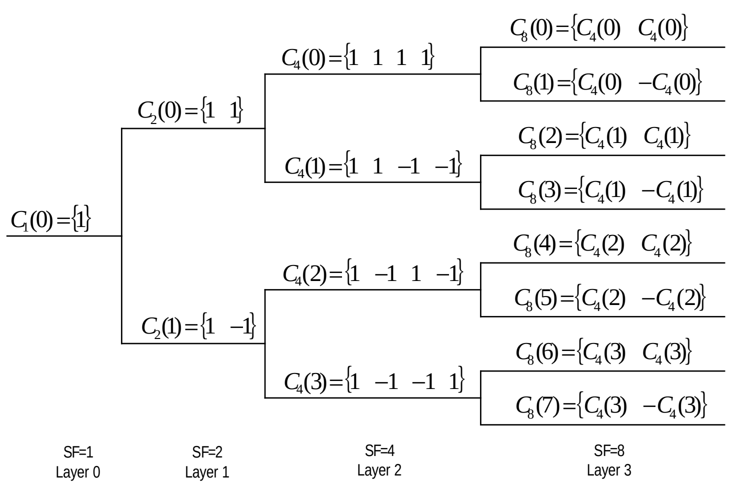

Figure (1): *OVSF tree structure*

The conventional OVSF code generator needs two independent input elements, which are SF and code number. With the single code indexing method both SF and code number can be described in one index, whose structure is as following;

$$(\underbrace{0, 0, \ldots, 0}_{SF\ part}\ 1,\ \underbrace{a_0, a_1, \ldots, a_{L-1}}_{code\ number\ part}) \tag{4}$$

The entire code length of binary number in Equation (4) is be determined by maximum SF used the system. The number of ‘0’ before the first ‘1’ from the left most significant indicates the SF of the code word, and the binary sequence after the first ‘1’ represents the code number. The OVSF code words with its SF up to 8 are shown in Table (1). The conventional OVSF code indices are shown in the first column, i.e., layer number (or SF) and code number. The new code index maps a single binary number to each code word as shown in the second column. The third column is the associated decimal code number.

Table (1): *The conventional and new code index representation*

Conventional code index (SF/Code number)	New single code index (a0,a1,…)	New code index in decimal	OVSF code word (-1 is substituted with 0)
1/0	0001	1	1
2/0	0010	2	11
2/1	0011	3	10
4/0	0100	4	1111
4/1	0101	5	1100
4/2	0110	6	1010
4/3	0111	7	1001
8/0	1000	8	11111111
8/1	1001	9	11110000
8/2	1010	10	11001100
8/3	1011	11	11000011
8/4	1100	12	10101010
8/5	1101	13	10100101
8/6	1110	14	10011001
8/7	1111	15	10010110

The following summarizes the advantages of the proposed new code indexing method.

- Reduced number of bits for identifying codes and increased capacity
- Easy to generate available orthogonal codes during code assignment
- Easy to spread and generate the long code
- Enable easy and fast DCA

3. Hardware structure:

The suggested code generator structure is designed applying to W-CDMA dual mode FDD (maximum SF:512) and TDD (maximum SF:16) in universal mobile tele-communications system (UMTS) system, and adopts multi-stage spreading scheme. To reduce hardware complexity and power consumption, this generator adopt generating scheme from two short code words Kronecker product combining. And while work in TDD mode, one code generator is working, but another code generator is stop working. Figure (2) is a block diagram of the proposed OVSF code generator. And the flowchart of the code generate proceeding is shown in Figure (3).

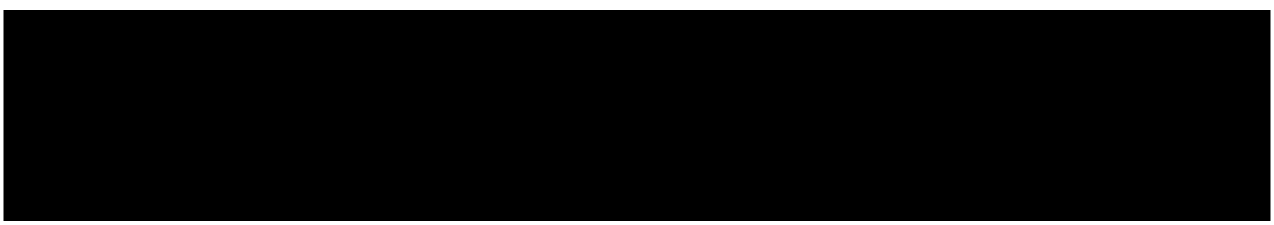

Figure (2): *Block diagram of the proposed OVSF code generator*

The block ZERO_COUNTER measure SF by counting the number of '0' (M) before the first '1' from input bits. Follow in ZERO_COUNTER result M, the block INDEX_DISASSEMBLER split a single index into two short indices, INDEX1 and INDEX2, and input these into each CODE_GENERATOR. The CODE_GENERATOR produce each short descendent code from mother code and previously mentioned property. And CODE_COMBINER combines two short descendent codes into a long code word by using Kronecker product.

Figure (4) is a block diagram of the proposed CODE_COMBINER module. Two stage spreading elements (short codes) from each CODE_GENERATOR are combined by using Kronecker product with repeater on each different time rate.

Figure (3): *The flowchart of the code generate proceeding*

Figure (4): *Construction of CODE_COMBINER*

4. Comparison with existing code generator:

The comparison of performance between proposed OVSF code generator using multiage stage scheme with single indexing method and existing method based on code tree structure in maximum SF 512, proposed method needs only 10 bits to distinguish all the codes of 1,024 codes. The reduction of 3 bits from 13 bits contributes almost 25 % increase in capacity. Existing method tabulate whole spreading code set and index (268,800 bits), but single code index method tabulate only index (5,120 bits) and this reduces memory size. Also, it is possible to generate available orthogonal code during code assignments without making any other memory for comparison (13,312 bits). Table (2) shows the result of comparison.

Table (2): *Comparison of memory size*

	Length of Index	Size for LUT	Memory for comparison
Existing method	13 bits	268,800 bits	13,312 bits
Proposed structure	10 bits	5,120 bits	0 bit

There are code word generation time of two methods in Table (3). Each code generators are implemented with VHDL and simulated by using Altera Quartus II. In all cases, proposed structure execute faster than existing method, and code wore length becomes longer, relatively speed becomes faster (maximum 32%).

Table (3): *Comparison of latencies*

SF	16	32	64	128	256	512
Existing method	0.06	0.08	0.114	0.145	0.18	0.25
Proposed structure	0.05 (16%)	0.07 (13%)	0.084 (26%)	0.115 (21%)	0.14 (22%)	0.17 (32%)

5. Conclusions:

In this paper, we propose an efficient structure for single index code generator. The result which designed with the maximum SF 512 and dual mode system for UMTS is that the suggested circuit has the performance improvements of 98 % in LUT size and maximum 32 % in speed. In addition, this method do not demand orthogonality check in code word level, therefore this structure does not request extra memory and time for compare mother code with descendent code. And this means that it is also an efficient structure for dynamic code assignment (DCA), because orthogonality verification time is the most part of overall DCA processing time. Therefore proposed structure is expected to be used in various CDMA based system.

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