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Article

A Novel Non-Superconducting Fault Current Limiter for Enhancing the Reliability and Stability of Electrical Distribution Grids

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Abstract: The expanding distributed power grids have elevated performance expectations for transmission equipment in power systems, emphasizing the crucial need to enhance stability and reliability in the electric power industry's development. This study presents the development and validation of a novel non-superconducting fault current limiter (NSFCL) for enhancing the reliability and stability of electrical distribution grids. The use of high power and self-turn-off solid-state switches is one of the main reasons for effectively reducing fault currents during transient events, and also improves the characteristics of NSFCL, including high voltage and current ratings, low losses, and good performance. Furthermore, the integration of a hybrid fault current limiter with DC systems offers additional benefits, including improved fault current limiting capabilities in DC circuits and enhanced stability during grid disturbances. The device's performance was rigorously tested through simulation and experimental trials, demonstrating its effectiveness in limiting interrupting fault currents while maintaining grid integrity. Overall, the experimental results demonstrated the efficacy of the NSFCL in limiting fault currents and improving the reliability of power systems. The successful implementation of the NSFCL in various power system applications highlights its potential to be an effective solution for protecting power systems from faulty conditions. As such, the NSFCL represents a significant contribution to the development of more reliable and efficient power systems. This novel solution holds significant promise for enhancing the reliability and resilience of electrical distribution networks by efficiently mitigating fault currents, thereby contributing to improved grid stability and reduced downtime.

Keywords: Hybrid DC circuit breaker, fault current limiter, short-circuit fault, solid state switches, distribution networks.

1. Introduction

The expanding distributed power grids have elevated performance expectations for transmission equipment in power systems, emphasizing the crucial need to enhance stability and reliability in the electric power industry's development. Mechanical breakers, currently prevalent in transmission systems, display commendable attributes

but are limited by inflexibility, lack of real-time responsiveness, and susceptibility to expanded circuit faults. The disconnection of load current poses challenges, as breaker contacts are prone to ablation by electric arcs, causing delays and hindering swift reactions to fault currents. Operational noise and constrained mechanical and electrical lifespans further contribute to the limitations [1,2].

Conventional mechanical circuit breakers (CBs) exhibit minimal contact resistance (a few micro-ohms) when in the closed position, providing galvanic separation when open. Despite these advantages, these devices suffer from prolonged reaction times attributable to the necessity of extinguishing the arc in a chute. The occurrence of arcs results in contact erosion, thereby reducing the lifespan of the device and incurring elevated maintenance costs [2].

Power semiconductor devices offer a rapid and arcless interruption, demonstrating heightened reliability and diminished maintenance requirements. However, these devices are burdened by elevated on-state losses and limited thermal capability in silicon wafers. Consequently, the accommodation of substantial transient overcurrents or high-rated currents is restricted, even with effective cooling measures in place. The amalgamation of a mechanical breaker and static switch allows for the fusion of the former's current-carrying functionality and the latter's swift and arcless interrupting characteristics. To preserve the advantages of static interruption, an ultra-fast contact opening is imperative.

Solid-state circuit breakers serve as integral components within the flexible AC transmission system, enabling rapid, adaptable, and precise control of power system parameters and grid structure. Leveraging power switch devices, these circuit breakers have garnered widespread attention due to their exceptional performance in managing switch currents since their inception.

Over the past two decades, various solutions have been put forth in this domain [1], encompassing hybrid breakers incorporating thyristors [2], [3], and gate turn-off thyristors (GTOs) [4]. The emergence of the integrated gate-controlled thyristor (IGCT), characterized by novel performance standards, heralds' fresh possibilities in the realm of hybrid switching techniques.

This paper introduces an inventive hybrid solution, emphasizing the validation of key functions, particularly the rapid opening speed. While anticipation for the realization of an industrial product is plausible, certain considerations remain imperative to ascertain compatibility with prevailing standards. The conventional breakers' opening delay time results in substantial short-circuit current values, establishing today's specified breaking capabilities beyond the 100-kA threshold. This exceeds the compatibility range for utilizing semiconductor devices to open or divert currents of such magnitude.

In reviewing previous efforts to enhance grid reliability and stability, it is evident that while significant progress has been made, certain shortcomings remain prevalent. One of the primary limitations observed in existing methodologies is the reliance on traditional fault current limiters (FCLs), such as resistive fault current limiters (RFCLs) and superconducting fault current limiters (SFCLs).

RFCLs, while effective in limiting fault currents to a certain extent, often exhibit high resistive losses, leading to energy dissipation and reduced efficiency in power transmission [6]. Furthermore, the transient response time of RFCLs may not be sufficient to address rapid fluctuations in fault conditions, potentially compromising grid stability during transient events.

Similarly, SFCLs have garnered attention for their ability to rapidly limit fault currents with minimal energy loss. However, the high cost associated with superconducting materials and cryogenic cooling requirements has hindered their widespread adoption in practical applications [7-10]. Additionally, SFCLs may face challenges in interrupting high fault currents effectively, particularly in high-voltage transmission systems, thus limiting their applicability in certain grid scenarios. Moreover, while some studies have explored the integration of FCLs with DC

systems to improve fault current limiting capabilities and grid stability, there remains a need for comprehensive evaluations of these hybrid systems under various operating conditions [11,12]. The effectiveness of hybrid FCLs in mitigating fault currents and enhancing grid resilience requires further investigation to address potential limitations and optimize system performance.

In summary, while previous works have made valuable contributions to the field of grid reliability and stability enhancement, there exist notable shortcomings that warrant attention. Addressing these limitations through innovative approaches, such as the development of novel non-superconducting fault current limiters (NSFCLs), as presented in this study, is essential to advancing the reliability and resilience of modern power systems.

The modernization and expansion of distributed power grids have imposed higher performance demands on transmission equipment within power systems, underscoring the critical importance of enhancing stability and reliability in the electric power industry's evolution. This imperative has prompted extensive research efforts aimed at developing innovative solutions to address these challenges [6]. A significant focus of recent research has been on the development of fault current limiters (FCLs) as essential components for enhancing the resilience and stability of electrical distribution grids. FCLs are crucial for mitigating the adverse effects of fault currents, which can lead to equipment damage, power interruptions, and grid instability. Various types of FCLs have been proposed and investigated in the literature, including superconducting fault current limiters (SFCLs), resistive fault current limiters (RFCLs), and non-superconducting fault current limiters (NSFCLs) [7]. Superconducting fault current limiters (SFCLs) have garnered significant attention due to their ability to rapidly limit fault currents with minimal energy loss. However, challenges such as high cost, cryogenic cooling requirements, and limited fault current interruption capabilities have hindered their widespread deployment in practical applications [8].

In contrast, non-superconducting fault current limiters (NSFCLs) have emerged as promising alternatives that offer advantages such as lower cost, simpler design, and compatibility with existing grid infrastructure. NSFCLs utilize solid-state switches and other innovative technologies to effectively limit fault currents during transient events, thereby enhancing grid stability and reliability [9].

Moreover, the integration of hybrid fault current limiters with DC systems has been proposed as a viable strategy for enhancing fault current limiting capabilities and improving stability in DC distribution grids [10-13]. Hybrid FCLs combine the advantages of different FCL technologies to achieve optimal performance in diverse grid scenarios, making them attractive solutions for modern power systems [14-17].

Building upon this body of literature, this study presents the development and validation of a novel NSFCL designed to enhance the reliability and stability of electrical distribution grids. By leveraging high-power solid-state switches and innovative design features, the proposed NSFCL offers improved fault current limiting capabilities while maintaining grid integrity during transient events. Rigorous simulation and experimental trials were conducted to evaluate the performance of the NSFCL, demonstrating its effectiveness in limiting interrupting fault currents and safeguarding power system operation [18-24].

This paper contributes to the ongoing efforts to develop more reliable and efficient power systems by introducing a novel NSFCL solution tailored to the evolving needs of modern electrical distribution networks.

2. Experimental setup and design considerations of the HDCCB model

The grid test system operates at a voltage level of ±220 V for the DC link, ensuring the efficient transmission of high-voltage direct current power within the setup. This configuration is vital for testing and assessing the performance of H-DCCBs and associated protective measures in a realistic and controlled environment.

The schematic of the proposed hybrid direct current superconducting fault current limiter (HDCSFCL) with direct current circuit breaker (DCCB) is depicted in Figure 1

the main assembly of the hybrid breaker, a Solid-state circuit breaker SSCB known as a residual circuit breaker (RCB) is incorporated. This SSCB serves as an additional safety and control measure for the system, particularly during fault scenarios.

This overall system architecture is designed to effectively handle and control high-current DC faults while ensuring rapid response times and reliable operation. It combines both mechanical and solid-state components to achieve the desired performance characteristics.

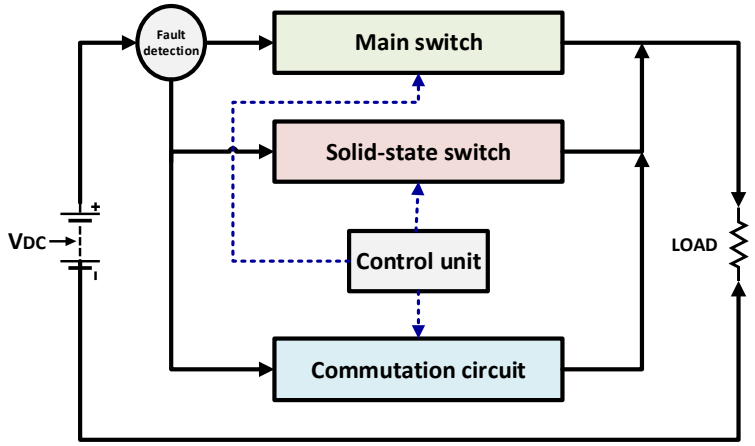


Figure 1. Schematic diagram of the proposed HDCSFCL

3. Schematic diagram and operation principle of the HDCCB

The proposed VSC-based five-terminal DC grid test system is designed with a symmetrical bipolar transmission line configuration to accommodate both positive and negative DC voltages. It incorporates HDCSFCL units with direct current circuit breakers (DCCBs) at each end of the transmission line to ensure robust protection against DC faults. The system employs multiple HDCSFCL units with DCCBs for enhanced fault protection. Furthermore, there is a series reactor connected to each DCCB, featuring an inductance of 100 millihenries (mH). These reactors serve to control the rate of DC fault current rise, thereby improving overall system stability.

The fault protection scheme in DC systems comprises two essential components. Firstly, a Fault Current Limiter (FCL) is employed to restrict the fault current, mitigating the impact of faults, and ensuring system stability and reliability. Secondly, the scheme involves coordination between the FCL and the DC Circuit Breaker (DCCB) to achieve swift and efficient fault current interruption. This coordination is pivotal in minimizing the duration of fault events and restoring normal system operation. To illustrate this proposed protection scheme, outlining the sequential steps involved in fault protection. These steps encompass fault current limitation by the FCL and subsequent action by the DCCB for fault current interruption. Effective coordination between these two components is paramount for successful fault management and system resilience.

In normal operation, the hybrid switch in the secondary circuit remains blocked, with diodes reverse-biased, while a capacitor is charged to a slightly lower voltage than the HV system. During this phase, the main contact of the hybrid DC circuit breaker is closed, allowing efficient current flow through the primary branch comprising the solid-state circuit breaker SSCB. In the event of a fault, current diverts to the auxiliary branch, composed of series-connected semiconductor cells, which rapidly open to redirect the fault current and protect the MCB from excessive

voltage. The ultrafast disconnector (UFD) opens when the auxiliary branch is no longer conducting current. To prevent thermal overload, a residual current breaker (RCB) is implemented to disrupt residual arrester current. Upon fault detection, the semiconductor branch becomes active, and a commutating element assists in current commutation and interruption. A control circuit constantly monitors the short circuit current, triggering the main contact to open when it surpasses a predetermined threshold, thereby halting the fault current. emitter turn-off (ETO) are integral to this process. In instances of faults originating from the opposite terminal, a similar sequence unfolds with designated ETOs being activated. A capacitor ensures that ETOs remain conductive until the fault current naturally diminishes or the primary switch disengages. For faults occurring at the opposite end, the fault current traverses distinct diodes, prompting the activation of specific ETOs as necessary. The mechanical switch's role is simplified in this process, as the main branch with the ETO provides an alternative path for the fault current. Initially, under normal conditions, the insulated gate bipolar transistor (IGBT) valves of line commutation switches (LCS) in an HDCCB are in a closed state while MB is in an open state. Hence, during normal load conditions, the DC load current passes through the load branch only. The corresponding current waveform of HDCCB, as proposed, is shown in Figure 2.

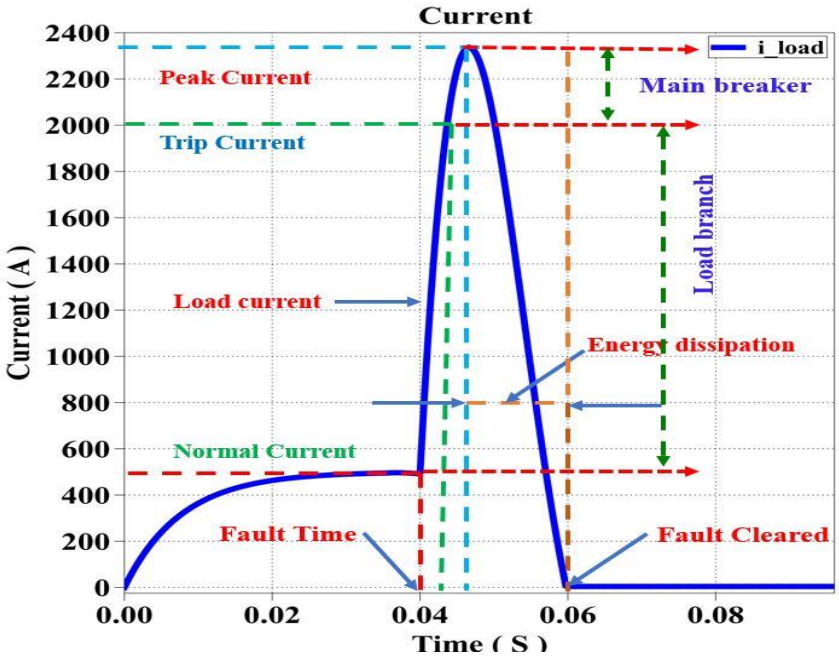


Figure 2. HDCCB fault current interruption.

The current changes over time after a fault occurs, the normal current is 500 A to the peak current is 2.4 KA the maximum current that flows through the system during the fault, the trip current of the main breaker is 2000 amperes, the load current is 1400 amperes, and the energy dissipation time is 80 μs. The current then decreases to zero as the fault is cleared.

The general strategy for DC fault isolation using an HDCCB consists of the following sequence of events:

- Step 1 involves the normal operation of the system, where the IGBT switch within the load LCS are in a closed state. Simultaneously, the IGBT switch within the MB are open. Given the low impedance of the load branch, a predominant portion of the load current is directed through this branch.
- Step 2 unfolds at time t_1 when a short circuit fault emerges, leading to a swift escalation of the DC fault current on the DC side of the VSC. Upon reaching a predefined threshold, denoted as the trip-value, a trip signal is generated at time t_2. In response, the LCS promptly disengages, and the IGBT switch in the MB is

activated. This action induces the fault current to transition from the load branch to the MB. Commonly termed the first commutation process, this sequence is visually represented in Figure 1. Notably, this process also instigates the opening of the UFA.

- In Step 3, the UFA undergoes a swift and complete separation of its contacts, achieving this within a 2 ms. This rapid action is crucial, as it ensures the capability to endure and safeguard the LCS from transient interruption voltages. Following this, at time t_3, the IGBT switch in the MB are deliberately deactivated.
- In Step 4, the preceding maneuver results in the intentional commutation of the DC fault current into the energy dissipation branch.
- Step 5 marks a pivotal stage where the majority of the fault current is successfully interrupted. Only a minimal leakage current traverses through the auxiliary branch, specifically the Static SSCB. In a strategic move to prevent thermal overload of arrestors, the RCB is actuated at time t_4, causing it to open.

Table 1 Model data

Symbol	Description	Value
Va	Output voltage of VSC 1	200 kV
Vb	Output voltage of VSC 2	199 kV
I_{Line}	Line nominal current	2 kA
R_{Line}	Line resistor	0.5 Ω
L_{Line}	Line inductor	30 mH
Rd	DC reactor resistor	0.05 Ω
Ld	DC reactor inductor	100 mH
R1	MB resistor (Magnetic Breaker 1)	2 Ω
R2	MB resistor (Magnetic Breaker 2)	2 Ω
R3	DC reactor damping resistance	200 Ω
RF	Resistance of the fault	

3.1 Overall of the laboratory model

The laboratory model for the hybrid DC fault current limiter (HDCFCL) in DC systems represents a comprehensive and innovative approach to address high-current DC fault challenges. This model features a three-branch topology, comprising the load branch with an ultra-fast mechanical actuator (UFA) and IGBT-based LCS, the main breaker (MB) branch employing a combination of IGBT valves for precise current control, and a solid-state energy absorption branch. A residual circuit breaker (RCB) adds an extra layer of protection before the main breaker assembly. This HDC SFCL aims to efficiently manage high-current DC faults, ensuring rapid response times, and reliable operation, making it a promising solution for enhancing the performance and safety of DC systems.

The experimental setup for the high-current direct current circuit breaker (HDCCB) model encompasses crucial design considerations and incorporates a fault detection technique. The HDCCB model is carefully designed to simulate real-world conditions, with a focus on the safe interruption of high-current DC faults. The setup incorporates key elements, including the main contact, semiconductor cells, and commutation components, to effectively control and interrupt fault currents. Additionally, the model features a fault detection technique that monitors and identifies fault conditions within the system promptly. This combination of hardware and fault detection methodology ensures that the HDCCB can reliably and efficiently respond to DC faults, contributing to enhanced system safety and performance.

The experimental setup incorporates measuring and protective devices illustrated in Fig. 3 to gauge and safeguard various components, such as mechanical contacts, a DC motor load, SSCB-Aux branch including current limiting inductors (CLIs) and a power dissipating resistor (PDR), a short circuit switch, re-settable circuit protector, DC current clamps PAC93, commutation circuit capacitor, Data View Monitor PAT.2 Software, and a power quality analyzer Chauvin Arnoux c.a 8336. These elements collectively serve to confine fault currents, dissipate residual currents, and oversee and assess the Fault Current Limiter (FCL)'s performance within a laboratory setting. Furthermore, the experimental circuit interfaces with a PC system enabling control, adjustment, and the printing of experimental results.

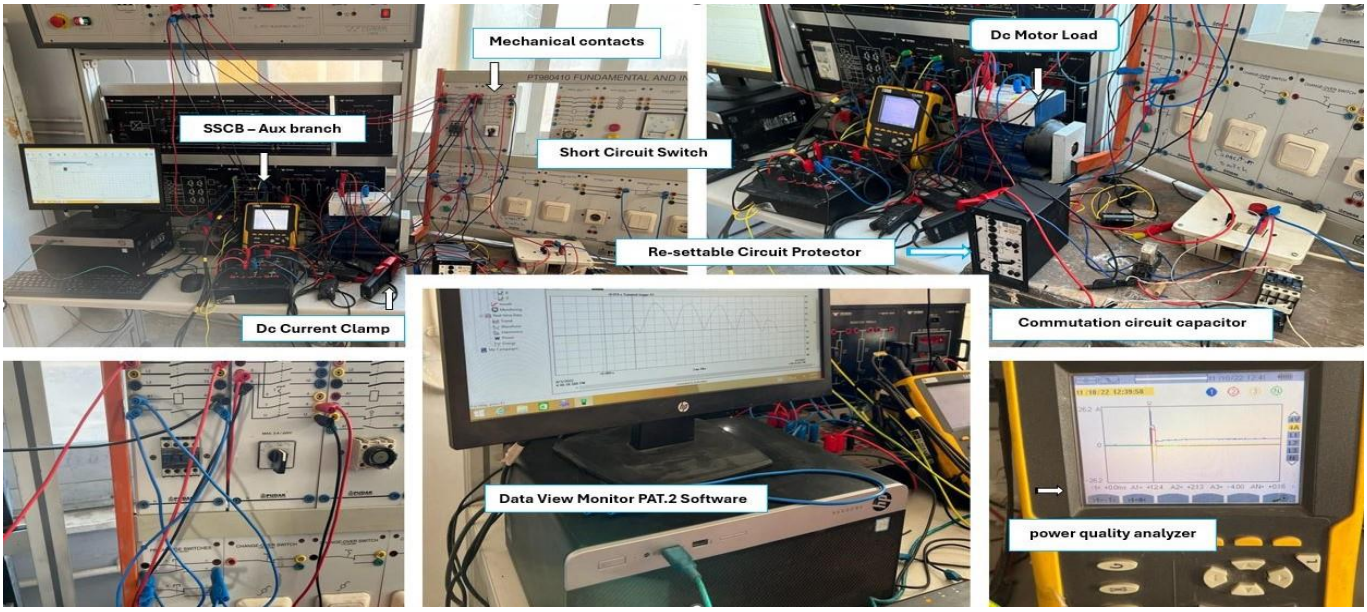


Figure. 3 Developed experimental prototype of HDCCB

3.2 Fault detection technique

Fault classification in DC systems using current magnitude, let through current, and di/dt of the fault current and voltage signal faces several challenges. One challenge is the difficulty in detecting and classifying high resistance faults, which require specialized algorithms such as the standard deviation index (SDI) [25]. Another challenge is the presence of insignificant fault currents in inverter-based islanded AC microgrids, which makes fault detection challenging. A voltage signal-based fault assessment method has been proposed to address this challenge, utilizing features such as instantaneous jumps in amplitude, phase angle, and frequency of the voltage signal[26]. Additionally, fault classification in DC systems requires fast protection algorithms and reliable DC circuit breakers, which are essential for clearing faults within a short time range[27]. Overall, the challenges in fault classification in DC systems include detecting high resistance faults, addressing insignificant fault currents in inverter-based microgrids, and ensuring the reliability of protection algorithms and circuit breakers.

So, in this paper during normal operation, the main contact of the hybrid DC circuit breaker is closed, allowing the line current to pass through the primary branch, which consists of the SSCB. The primary branch has a low conduction resistance, enabling efficient current flow shown fig.1.

a. In the event of a fault, the current is diverted to the auxiliary branch, which is made up of series-connected semiconductor cells.fig.1.

b. The cells within the hybrid DC circuit breaker play a crucial role in redirecting the fault current and protecting the SSCB from excessive voltage. These cells quickly open to create a new current path, ensuring that the increasing

voltage across the breaker is mitigated. At the same time, the ultrafast disconnector (UFD) opens as soon as the auxiliary branch no longer carries current. To prevent the solid-state banks from experiencing thermal overload, a residual current breaker (RCB) is employed. This component interrupts the residual arrester current and isolates the faulty line or cable from the DC grid. Furthermore, when a fault is detected, the semiconductor branch is activated (if not already active), and the commutating element is triggered to facilitate current commutation and interruption. As the current in the isolating switch decreases, the current in the semiconductor branch starts to rise. The control circuit continuously monitors the short circuit current and compares it to a predefined threshold. When the short circuit current exceeds this threshold, the control circuit sends a control signal to the electrodynamic drive, causing the main contact to open and effectively interrupt the fault current.

3.3 Commutation circuit

Upon opening of the main contact, the fault current is directed towards the auxiliary solid-state branch, and a signal is generated to activate the commutation thyristors, known as IGCT. This activation signal enables the fault current to pass through the current-limiting branch of the hybrid DC circuit breaker. The control scheme of the circuit breaker is specifically designed to accurately determine the direction of the fault current, particularly in cases where the short circuit current exceeds a predefined threshold, such as 20 kA, at a voltage of 500 kV. The IGCTs play a crucial role in the interruption process, relying on the control circuit's signal to ensure effective current commutation and interruption. For a visual representation of the circuit configuration and the involvement of IGCTs, please refer to Figure 1.

3.4 Control circuit

The combination of the IGCT and diodes in parallel creates a low-impedance path for the fault current, effectively limiting the current to a safe level. The presence of the capacitor ensures that the IGCT and diodes remain conducting until the fault current either decays naturally or until the main switch opens. In the situation where the fault current originates from the opposite terminal (as shown in Fig. 4), the sequence of events follows a similar pattern as described earlier. However, in this case, only the IGCT connected to the respective diodes (D_2 and D_4) will be triggered, allowing the fault current to be diverted through that particular path. The remaining components and operation of the circuit remain unchanged.

In the event of a fault occurring on the other end of the circuit, the fault current will flow through diodes D_2 and D_4. This will cause the voltage across the commutation booster circuit to become negative. As a result, the IGCT in the commutation booster circuit will remain in a blocking state, preventing the fault current from flowing through that specific path. However, as the fault current rises to a certain level, the IGCT in the main branch will be triggered on, providing a low-impedance path for the fault current. The mechanical switch does not need to produce a high arc voltage during the commutation process because the main branch with the IGCT provides an alternate path for the fault current.

The diodes D_1 and D_3 in the auxiliary branch will be reverse-biased, and the capacitor will discharge through the commutation booster circuit, Therefore, in this scenario, only the IGCT in the branch will be triggered on, with the other diodes in the circuit providing an alternate path for the fault current.

3.5 Characteristics of solid-state switches.

The main difference between ETO and IGBT or IGCT is the type of semiconductor device used. ETO is a type of thyristor-based device, while IGBT and IGCT are transistor-based devices. ETO devices consist of both thyristor-based and transistor-based components, while IGBT and IGCT devices are purely transistor-based. ETO devices aim

to reduce losses in both conduction and switching domains by combining thyristor and transistor components [28]. Seemingly, much of the effort is dedicated to optimization of components, improving the efficiency, and reducing the cost of a rather limited number of basic ideas.

in this study, it is proposed that the IGCT component be substituted with an ETO component due to its advantages demonstrated in Table 2. Many semiconductor devices on the market today possess favorable characteristics for implementing fault current limits. The selected device must be capable of withstanding high voltages and currents without failing and be able to stop the current within microseconds after a fault occurs. The IGCT is a powerful semiconductor switch that combines the benefits of transistors and thyristors. During conduction mode, it functions as a thyristor with low voltage drop and high blocking voltage ratings. However, during blocking mode, it acts like a transistor with high blocking current reliability and fast switching times. The IGCT diverts current to the gate during switching mode, where it is dissipated by the gate driver. A snubber circuit is required to assist the IGCT in handling higher currents. The ETO is another high-power semiconductor switch that enhances the limitations of the IGCT. It combines the advantages of GTO and IGBT and is a gate-off thyristor in series with a MOSFET. The ETO has fast switching speed, high current-carrying capacity, low conduction loss, and the ability to stop current up to 4000 A. It also has built-in sensors for voltage, current, and temperature. The ETO can operate with or without a snubber circuit, although one is typically included to limit the di/dt time. The total losses of a 4 kA/4.5 kV ETO are shown in Figure 4, which are better than those of the IGCT and IGBT. As the current increases, the losses for both the ETO and IGCT increase linearly. The ETO performs exceptionally well in total losses for a high-power switch.[29]

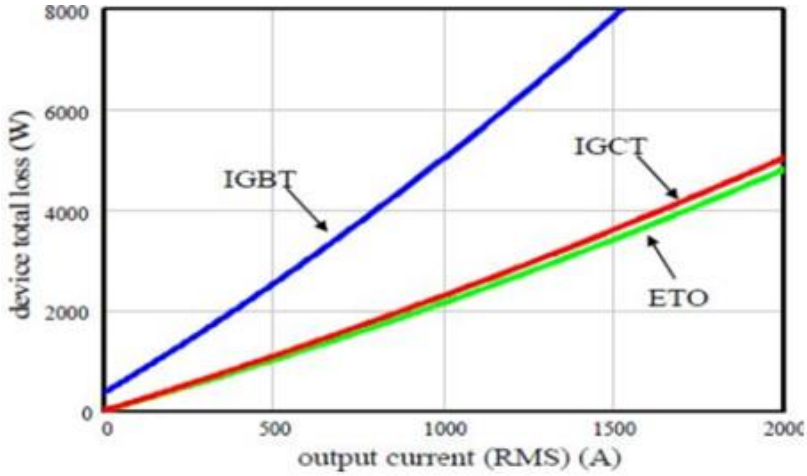


Figure 4 -1 kHz switching frequency total losses of a 4kA/4.5kV ETO and comparable IGBT and IGCT devices.[30]

4 Experimental data and results

The experimental setup includes measuring and protective instruments, as depicted in Fig. 3, which are employed to measure and protect various components within the system. Furthermore, the experimental circuit is connected to a laptop, allowing for control, adjustment, and the printing of experimental output results. In this particular section, a downscaled experimental prototype has been developed and executed in order to authenticate the simulation outcomes. The data pertaining to the prototype components can be found in Table 2. Figure 2 illustrates the devised prototype arrangement. Within this arrangement, a voltage source converter (VSC) supplies power to a DC load through a modeled DC line and the proposed hybrid direct current circuit breaker (HDCCB). In this evaluation, a

DC link to ground fault is established using a mechanical switch. Upon fault detection, the HDCCB is activated according to the operational pattern provided in Table 2.

The voltage and current signals that have been measured are presented in Figure 5 to 7. Figure 5 to 7 a show cases the DC link current under normal and fault conditions. In this signal, the magnitude of the normal current is 2 A, while the peak value of the fault current reaches 3 A. The delay of the proposed HDCCB from the occurrence of the fault until the zero-crossing of the line current is approximately 3 ms.

Figure 5. Fault current before using SCM with FCL" likely represents a graphical depiction or data illustrating the behavior of fault currents in the electrical system before the implementation of superconducting magnetic energy storage (SCM) with Fault Current Limiter (FCL). The magnitude, waveform, or other characteristics of fault currents under various fault conditions, such as short circuits or system disturbances, prior to the integration of SCM with FCL technology. Interpreting this figure could provide insights into the severity, duration, and dynamics of fault currents before the application of SCM with FCL. It serves as a baseline or reference point for evaluating the effectiveness of the SCM with FCL in mitigating fault currents and enhancing system reliability and stability.

Figure 6 portrays the voltage stress experienced by the HDCCB during the opening of the DC link in the fault state. The maximum voltage recorded for the main breakers (MBs) amounts to 180 V, which is less than twice the normal voltage. Figures 7 display the current for the LCS and the MBs, respectively. It has been demonstrated that following a fault, the peak current of the LCS rises to 2.5 A, while the peak current of the MB reaches 1.25 A. All of the experimental findings unequivocally validate the simulation results as depicted in Figure 5 to 7. Analyzing the experimental results presented in Figure 7 develop effective strategies for fault detection, protection, and system design aimed at enhancing the resilience and efficiency of power distribution networks.

Table 2 Experimental setup parameters

Symbol	Description	Value
Vs	Nominal voltage of VSC	200 V
I_{Load}	Load current	3 A
R_{Line}	Line resistance	0.5 Ω
L_{Line}	Line inductance	30 mH
Rd	DC reactor resistance	0.1 Ω
Ld	DC reactor inductance	100 mH
C	DC link capacitor	100 mF (millifarads)
R1	MB series resistor (Magnetic Breaker 1)	2 Ω
R2	MB series resistor (Magnetic Breaker 2)	2 Ω
R3	DC reactor damping resistor	200 Ω
RF	Resistance of the fault	0.01 Ω

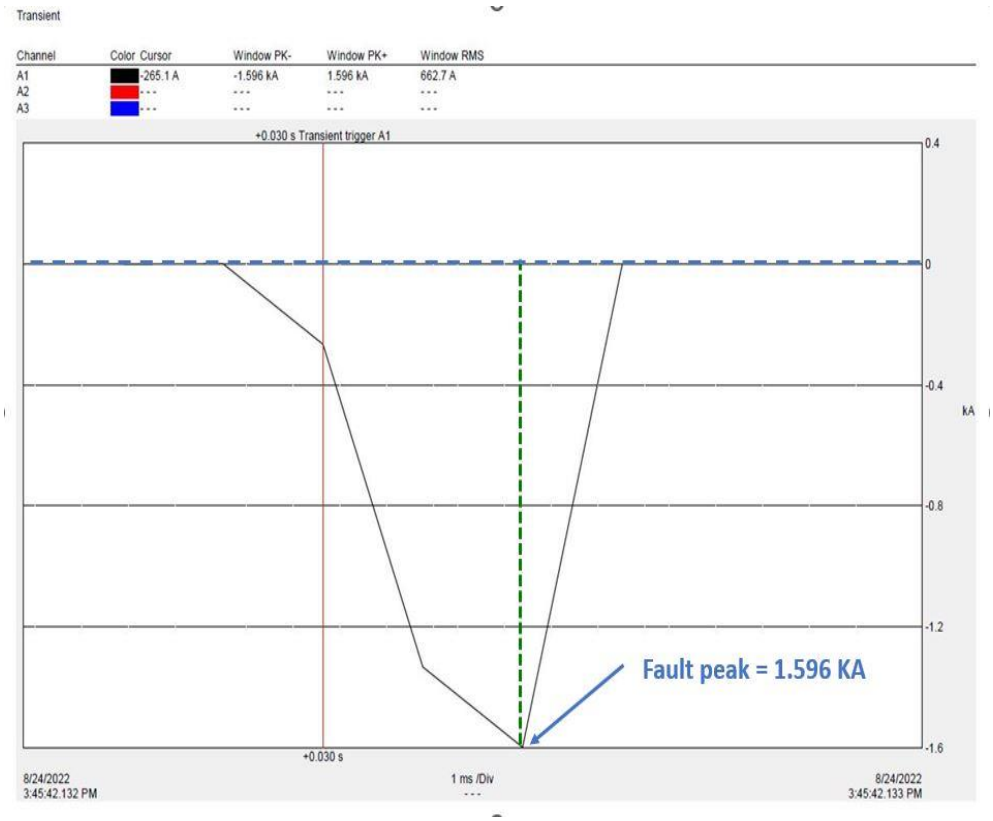


Figure 5. Fault current before using SCM with FCL

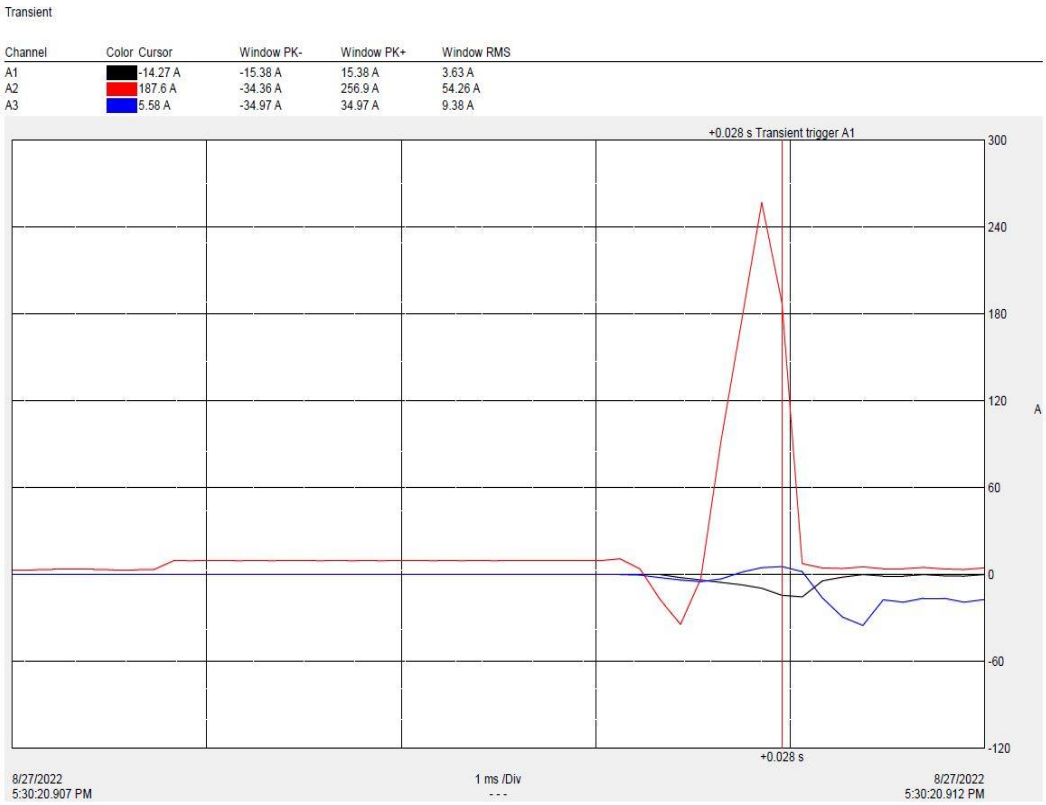
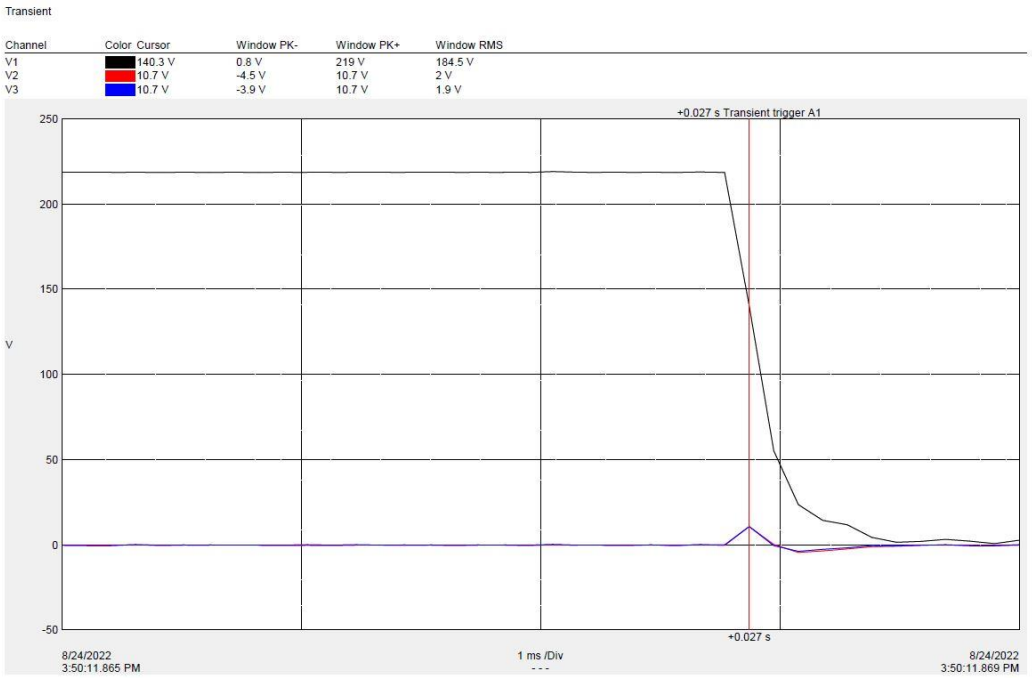
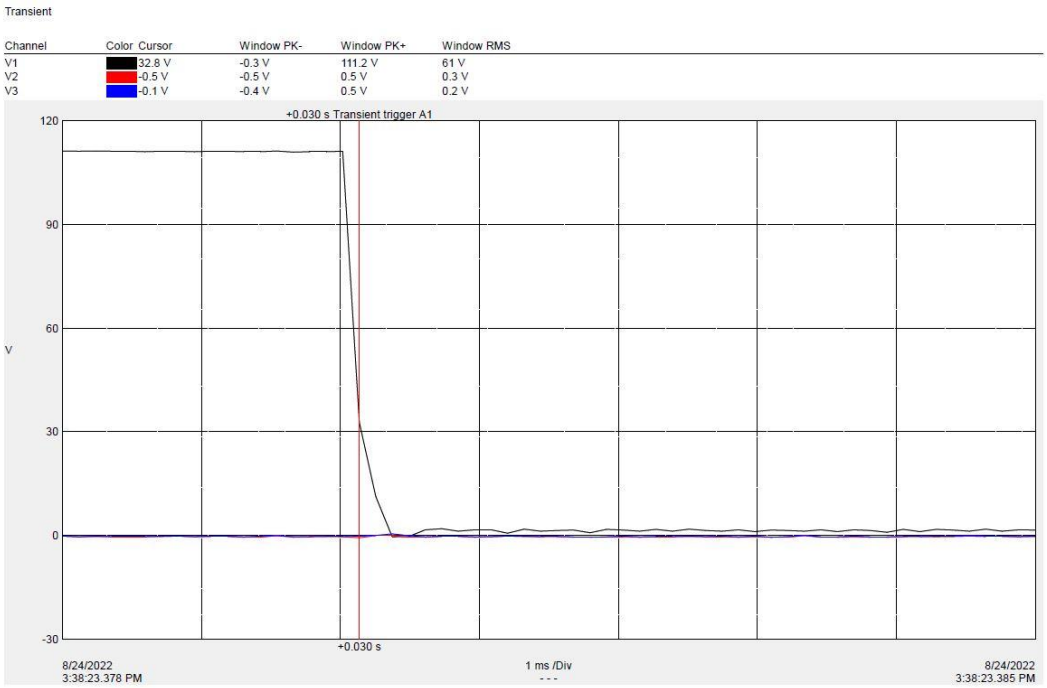


Figure 6. Fault current after using SCM with FCL



(A)



(B)

Figure.7 Effect of the fault on the source voltage at different value (A) and (B).

Figure 8 displays experimental test results pertaining to the HDCCB, delineating various aspects: Figure 8 displays (a) the Effect of commutation circuit on fault current. It explores how efficiently the commutation circuit manages the interruption and modulation of fault currents during operation. Figure 8 displays (b) the extent of the system's response to the hybrid fault limiter. It assesses the system's ability to detect and respond to faults, thereby minimizing

their impact and ensuring the integrity of the electrical network. Figure 8 displays (c) the component likely investigates the behavior of voltage restoration following the HDCCB's intervention in fault scenarios. It examines how quickly and effectively the system recovers its voltage levels post-fault, ensuring the resumption of normal operation and system stability. Experiments examining the proposed hybrid circuit breaker (HDCCB) are conducted, considering a line-to-ground voltage of 200 V and a line nominal current of approximately 2 kA. The experimental scenarios are categorized into three distinct time periods, with the line current being depicted in Figure 8. During the initial time period, the fault current is restricted by the DC reactor and LCS, resulting in the occurrence of peak fault current. Subsequently, the line current transitions to parallel MBs, attaining a value of 80 A owing to the resistive current limiter. At a later point in time, the MBs are deactivated in order to interrupt the fault current.

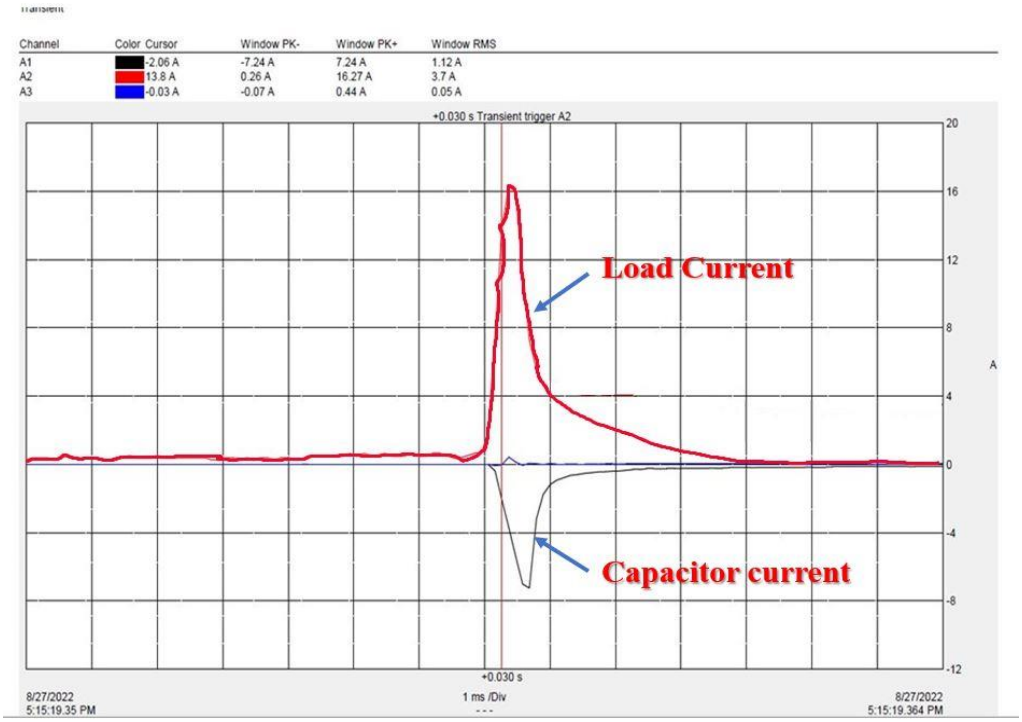
Figure 8 show the experimental test results for an HDCCB, providing insights into the performance of the commutation circuit, the system's response to a hybrid fault limiter, and the recovery voltage after the HDCCB has intervened in the electrical system. The effect of change the capacitor value increase, effect of change the capacitor value decrease and Effect of change the coil value increase as depicted in Figure 9.

Figure 9 presents experimental test results for the HDCCB, focusing on the effects of changing capacitor and coil values. The experiments examine the impact of increasing and decreasing capacitor values, as well as increasing coil values, on the HDCCB's performance and behavior in managing fault currents and ensuring system stability. These findings help researchers optimize HDCCB technology for enhanced reliability and efficiency in electrical grid applications.

5 Comparison of breakers

According to the provided data, a concise correlation between HDCCB and the conventional hybrid DC breakers [5] is delineated in Table 3. Within this section, experimentally verified simulation findings are juxtaposed with the results of a DC breaker prototype available in the market. In this comparative analysis, the assumed base voltage and current are 200 and 2 kA, respectively. Each IGBT unit is rated at 4.5 kV [31- 38].

Table 4 clearly illustrates the remarkable advantages of the proposed HDCCB breaker over its hybrid counterpart. Notably, the HDCCB breaker demonstrates markedly reduced rates for current elevation, peak current, and voltage of the MB when contrasted with the hybrid breaker. This significant disparity translates into a considerable enhancement in breaker switch safety. Additionally, both the operation time and dissipated energy values experience a notable decrease with the implementation of the HDCCB breaker. Furthermore, Table 4 provides a comprehensive comparison of the equipment utilized in both DC breakers, further emphasizing the superiority of the HDCCB design.


Transient
Channel Color Cursor Window PK- Window PK+ Window RMS
A1 -2.06 A -7.24 A 7.24 A 1.12 A
A2 13.8 A 0.26 A 16.27 A 3.7 A
A3 -0.03 A -0.07 A 0.44 A 0.05 A
+0.030 s Transient trigger A2
Load Current
Capacitor current
20
16
12
8
4
0
-4
-8
-12
A
+0.030 s
8/27/2022
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1 ms /Div
8/27/2022
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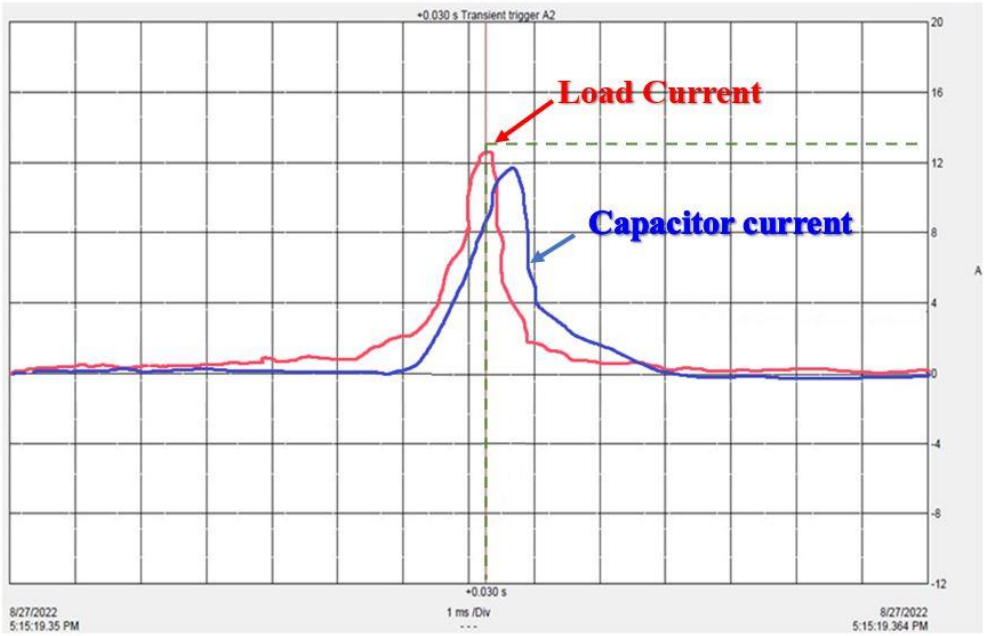
(a)


+0.030 s Transient trigger A2
Load Current
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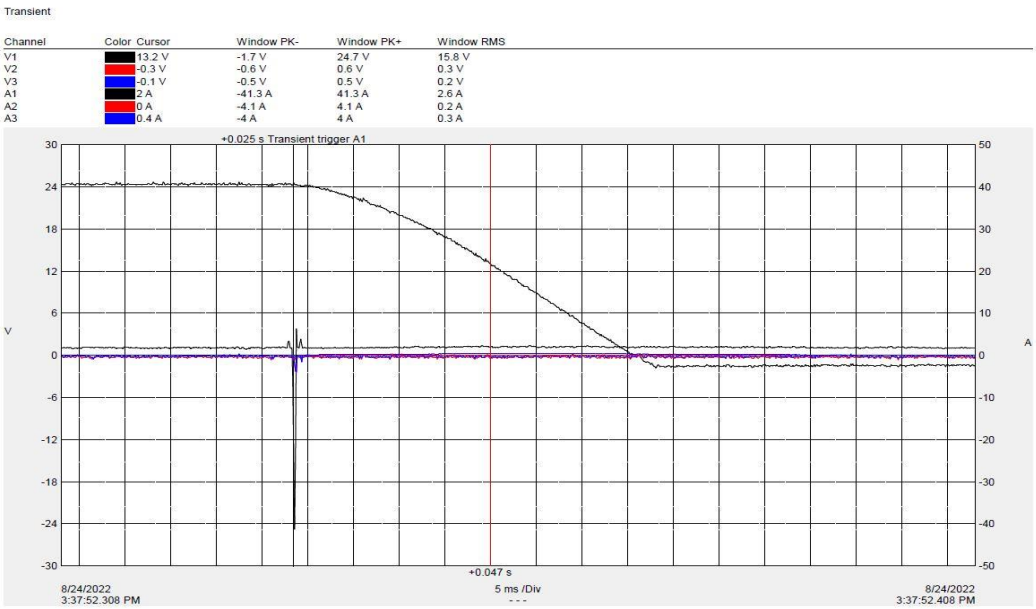
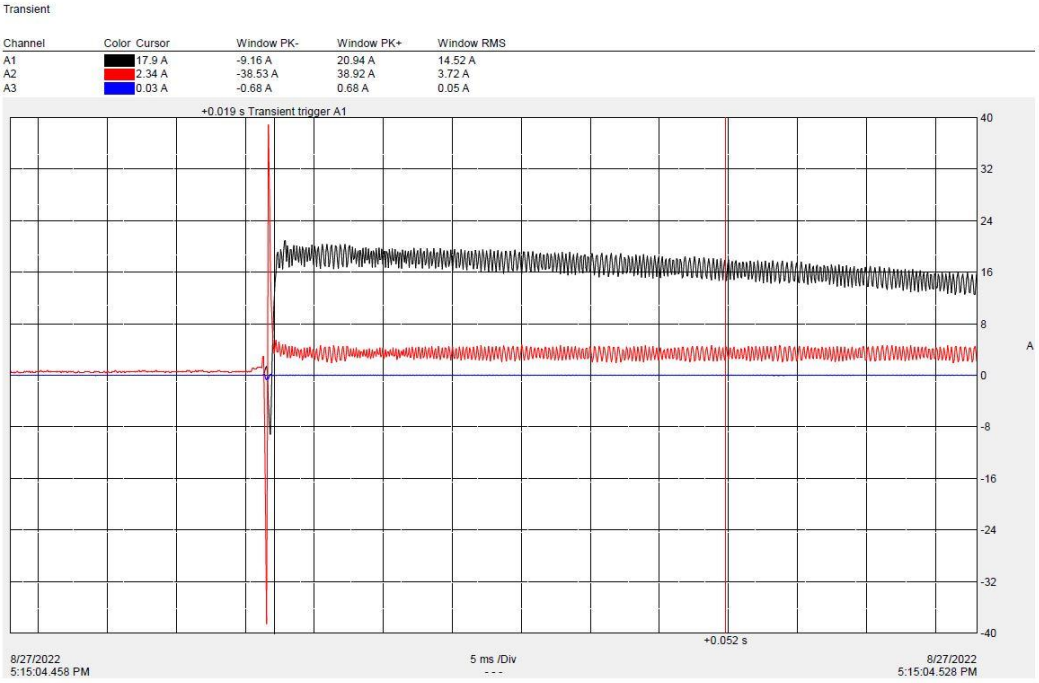
(b)

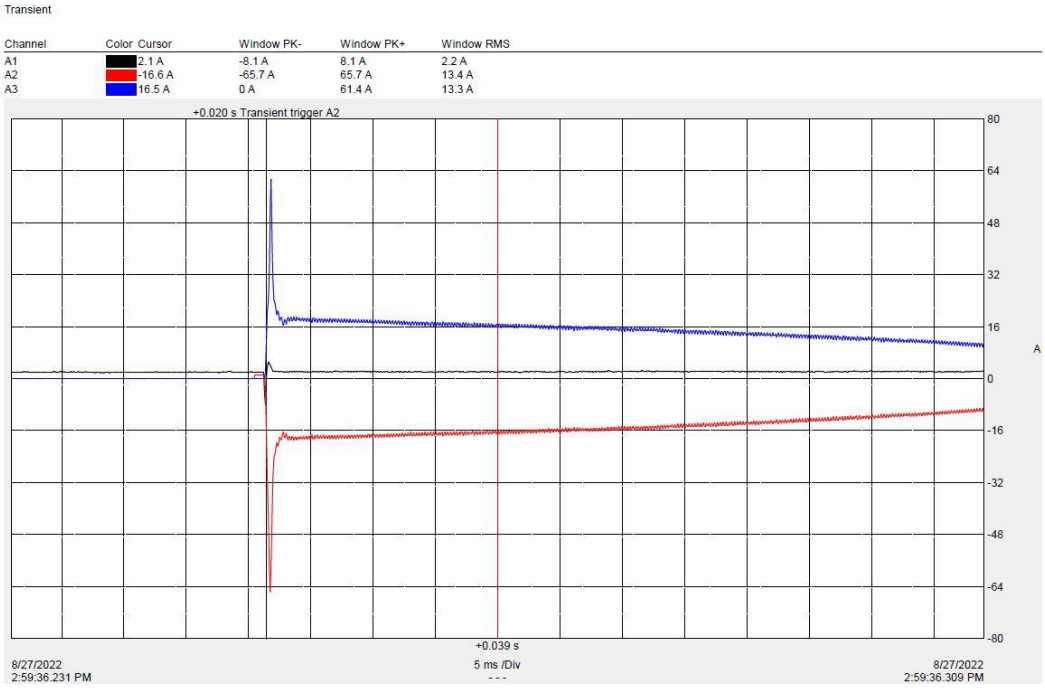


(c)

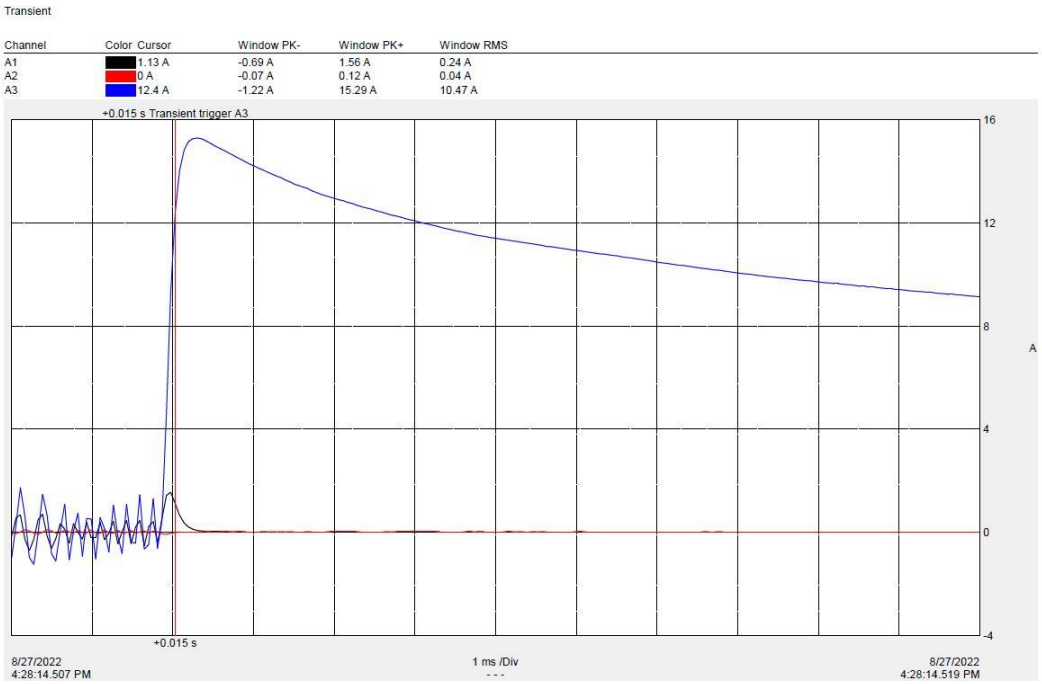
Figure.8 HDCCB Experimental test results, (a) Effect of commutation circuit on fault current, (b) The extent of the system's response to the hybrid fault limiter, (c)recovery voltage after HDCCB.



(a)



(b)



(c)

Figure.9 HDCCB Experimental test results, (a) Effect of change the capacitor value increase, (b) Effect of change the capacitor value decrease, (c) Effect of change the coil value increase.

Table 3: DC breakers comparison

Features	Mechanical Breaker (MB)	Hybrid Breaker	HDCCB
Peak Voltage of the Breaker (pu)	3	1.8	1.2
Peak Current of the Breaker (pu)	2.4	0.7	0.4
Number of Breaker Switches	134	160	40
Dissipated Energy on the Arresters (MJ)	2.75	1.76	1.5
Operation Time (ms)	5	2.9	1.8
LCS (Load Current Switching)	One packaged IGBT, 4.5 kV, 4.8 kA	One packaged IGBT and diode, 4.5 kV, 2.9 kA	One packaged IGBT and diode, 4.5 kV, 2.9 kA
MB (Main Breaker)	134 series IGBTs, 4.5 kV, 4.8 kA	160 series IGBTs, 4.5 kV, 1.4 kA	series IGBTs, 4.5 kV, 1.4 kA
Limiter	One DC reactor, 100 mH	One DC reactor, 100 mH	One DC reactor, 100 mH – one capacitor, 100μF
Arresters (Surge Arresters)	Metal oxide arrester, peak voltage 600 kV, 2.75 MJ	Metal oxide arrester, peak voltage 360 kV, 1.76 MJ	Two series IGBT, 10 kV, 100 A
Controlling Switch	IGBT, 10 kV, 100 A	Not specified	Not specified

Table 4: summarizing the specifications you provided for three different ETO, IGCT components [39]

Specification	ETO	IGCT
Critical Rate of Rise of On-State Current (di/dtmax)	1000 A/μs	1000 A/μs
Critical Rate of Rise of Off-State Voltage (dv/dtmax)	-	-
Max. Controllable Turn-Off Current (ITGQM)	4000 A	4000 A
Forward Voltage (at nominal current) (VT)	3.3 V	1.8 to 2 V
Maximum Repetitive Voltage (Vm)	4500 V	4500 V
Maximum Reverse Voltage (off) (Vrrm (off))	17 V	17 V
Maximum Reverse Voltage (on) (Vrrm (on))	-	10 V
Repetitive Peak Off-State Current (IDRM)	100 mA	50 mA
Typical Off-State Current (ID)	-	-
Max RMS On-State Current (IT(RMS))	1850 A	3300 A
Rated Junction Operating Temperature (Tjunc,rated)	10 to 125°C	-40 to 125°C
Junction to Case Thermal Resistance (RΘjc)	12.7 K/kW	8.5 K/kW

6 Conclusions

In conclusion, the implementation of a novel non-superconducting fault current limiter (NSFCL) presents significant outcomes for enhancing the reliability and stability of electrical distribution grids. Through fault current limitation during transient events, the NSFCL effectively reduces the risk of equipment damage and power interruptions, thereby contributing to improved grid stability. Rigorous performance evaluation through simulation and experimental trials underscores the NSFCL's efficacy in maintaining grid integrity under diverse operating conditions. Furthermore, the cost-effectiveness and compatibility of NSFCLs with existing infrastructure offer promising prospects for their widespread adoption in modern electrical distribution networks. Overall, the successful implementation of NSFCLs signifies a notable advancement in safeguarding power systems from fault conditions, ultimately enhancing their safety, stability, and overall performance.

The successful implementation of NSFCLs in various power system applications highlights their potential as an effective solution for protecting power systems from fault conditions, with implications for improved grid stability and reduced downtime. In summary, the outcomes of implementing a novel NSFCL include improved fault current limitation, enhanced grid stability, increased reliability, cost-effectiveness, and compatibility with existing infrastructure, ultimately contributing to the overall efficiency and resilience of electrical distribution grids.

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