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Power minimization in CMOS RF mixers

By

Ahmed ElDeib* Roshdy A. AbdelRassoul** *Senior Member, IEEE*

Abstract:

A new very low power RF mixer is introduced. The proposed mixer is based on two techniques: A CMOS transistor pair is applied to the four cross-coupled commutating transistor (the first technique), and current boosted technique, as described in the paper. The CMOS mixer is simulated in 0.8 µm CMOS technology. The mixer has an input signal of 0.2V and operates on a single 2.5V supply with transistor threshold voltages of 0.57V for all NMOS transistors and -0.52V for all PMOS transistors, and has a power dissipation of 2.3 mW.

Keywords:

CMOS, RF, mixer, low power, current-boosted.

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* Modern Academy, Cairo, EGYPT. E-mail: ahmed.eldeib@gmail.com
** Arab Academy for Science, Technology & Maritime Transport, Alexandria, EGYPT, 21937. E-mail: roshdy@gmail.com

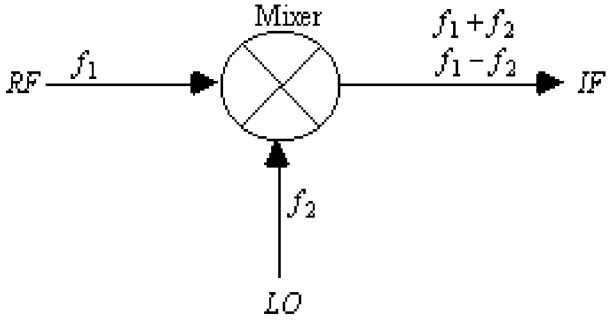
1. Introduction:

A Mixer is used for frequency conversion and is a critical component in modern radio frequency (RF) systems. A mixer converts RF power at one frequency into power at another frequency to make signal processing easier and also inexpensive. A fundamental reason for frequency conversion is to allow amplification of the received signal at a frequency other than the RF, or the audio frequency. A receiver may require as much as 140 decibels (dB) of gain. It might not be possible to put more than 40 dB of gain into the RF section without risking instability and potential oscillations. Likewise the gain of the audio section might be limited to 60 dB because of parasitic feedback paths and microphonics **[1]**.

The ideal mixer, represented by **Fig. (1)** , is a device that multiplies two input signals. If the inputs are sinusoids, the ideal mixer output is the sum and difference frequencies given by

$$V_o = [A_1 \cos(\omega_1 t)][A_2 \cos(\omega_2 t)] = \frac{A_1 A_2}{2}[\cos(\omega_1 - \omega_2)t + \cos(\omega_1 + \omega_2)t] \qquad (1)$$

Typically, either the sum, or the difference, frequency is removed with a filter.

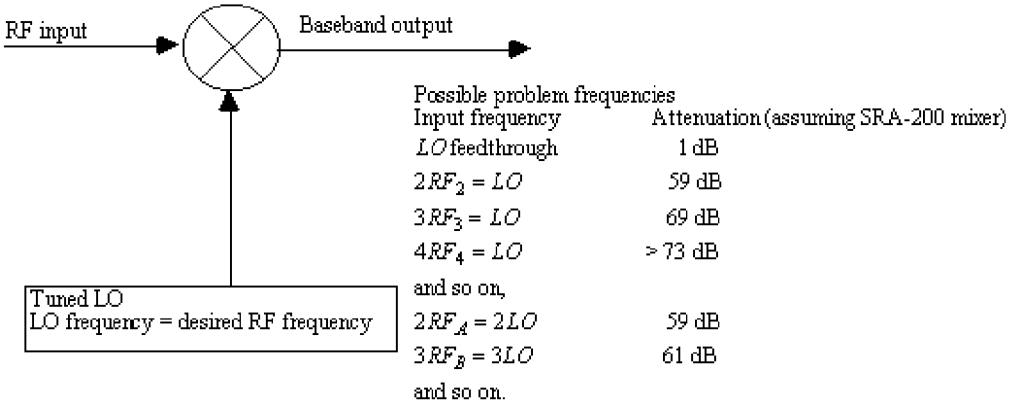


***Figure(1**):Circuit symbol for a mixer*

The direct conversion receiver of **Fig. (2)** suffers from several disadvantages. It does not have an intermediate frequency (IF) stage **[2].** The purpose of an IF stage is to allow additional amplification at a non-harmonically related frequency that will not feedback into the RF input and cause oscillation. The gain of the direction conversion receiver is therefore limited to the gain of any RF amplifiers preceding the mixer, and any audio amplifiers following the mixer. AM and SSB can be demodulated, but not FM. There is usually significant LO feed through at the desired frequency, which can cause undesired beats in the audio output for AM signals**.**

In reality, mixers produce more than just the sum and difference frequencies. The inter modulation products are given by

$$IF = N*RF \pm M*LO \qquad (2)$$

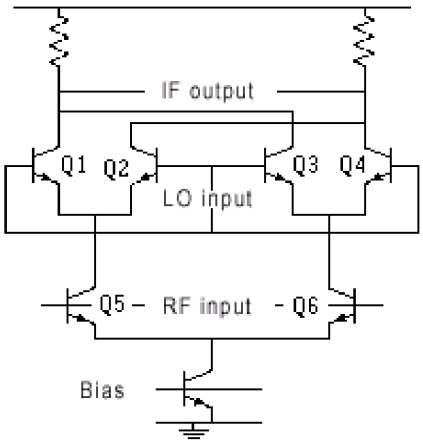


Where M and N are integers.

Figure(2): *Direct conversion receivers*

2. Gilbert Mixer Basics:

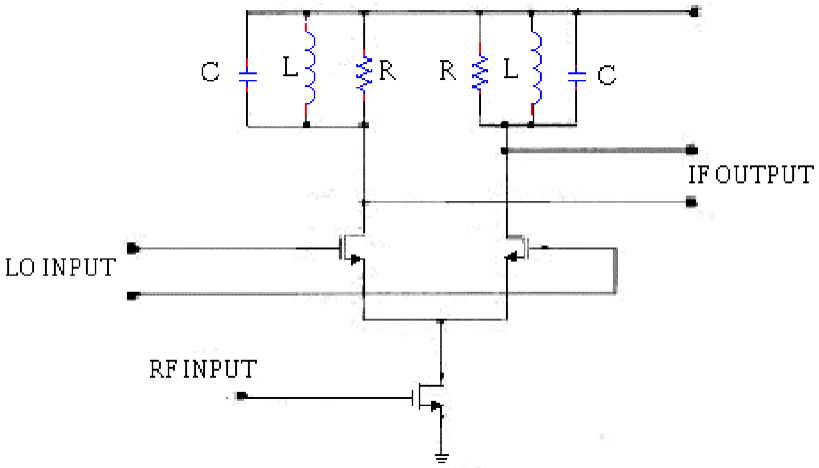
Gilbert mixer was proposed in the 1960 and is still the backbone of most of the mixers we have today. **Fig. (3)** shows the main elements of the Gilbert mixer, including an RF stage and an LO stage. The RF stage consists of a bipolar differential pair, Q5 and Q6, and a current source. For the LO stage, including Q1, Q2, Q3 and Q4, if LO voltage is sufficiently large, it will operate as a current steering circuit by steering the current from one side to the other side of the differential pairs. It is very common to apply a large LO signal to modulate the RF signal in mixers **[3]**. But the original multiplier principle of the Gilbert mixer is targeted at sinusoidal signal for both RF and LO inputs**.** Thus, small signal is assumed for LO for the explanation of the principle of the Gilbert mixer. For the mixers used nowadays, the LO signal is chosen large enough so that the LO stage transistors alternately commutate all of the tail current from one side to the other at the LO frequency. It is equivalent to use a square wave at the LO frequency to modulate the RF signal. Although the square wave introduces a lot of odd harmonics, the undesirable harmonics will be filtered out with the IF filters **[4].**.



Figure(3): *Standard form of Gilbert mixer*

3.Single-Balanced Design:

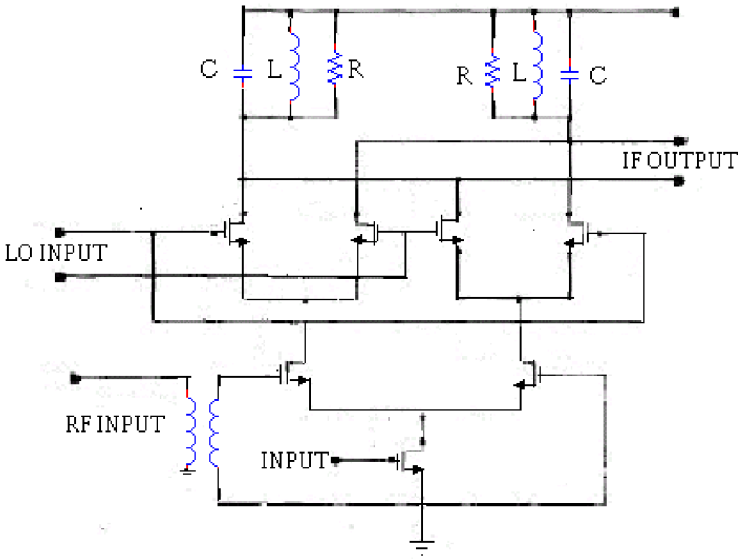
The single-balanced mixer shown in **Fig.(4)** is the simplest approach that can be implemented in most semiconductor processes. The single balanced mixer offers a desired single-ended RF input for ease of application. Though simple in design, it has moderate gain and low noise figure. However, the design has low 1dB compression point, low port-to-port isolation, low input IP3 and high input impedance **[5].**



Figure(4):*Single balanced mixer*

4. Double-Balanced Design:

The double-balanced or Gilbert cell mixer in **Fig. (5)** is most desirable for high port to port isolation and spurious output rejection applications. It can provide high gain and very low noise figure. The linearity is reasonably good. Typically, the RF filter preceding the mixer is single-ended so a balun transformer is needed to convert the single ended input to a differential signal for the mixer. Transformer that has low insertion loss is very difficult to implement in integrated circuits. This forces the use of an external transformer which occupies more board space and cost. The additional space and cost may not be justified for consumer product **[6].**



Figure(5): *Double-balanced Gilbert cell mixer*

5. Proposed circuit:

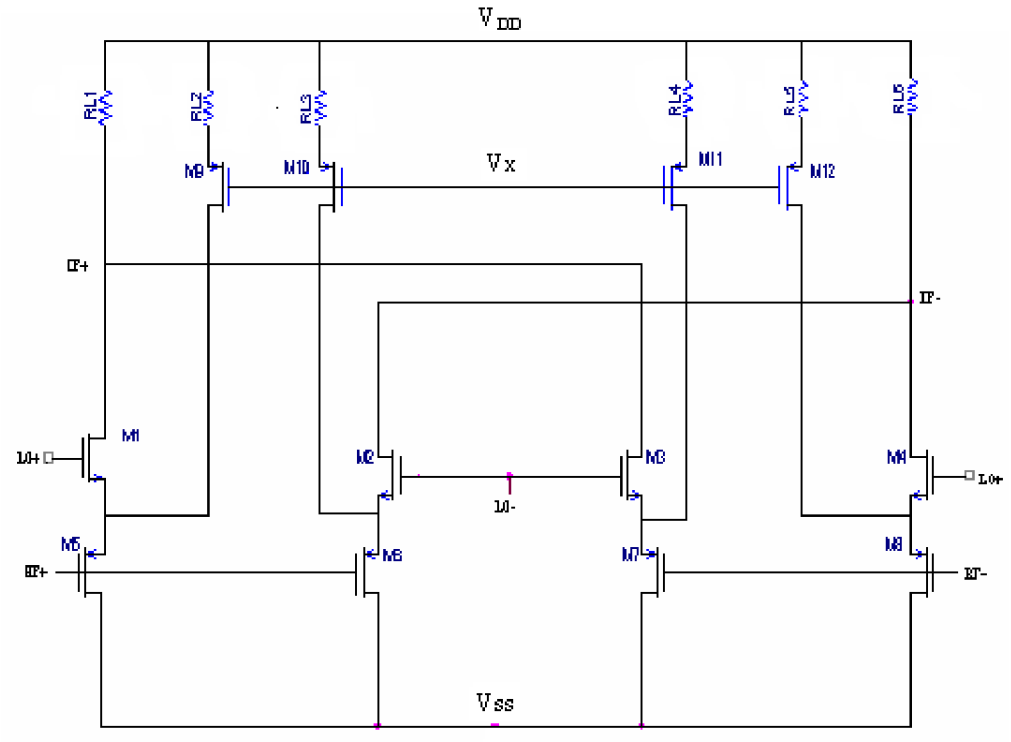
The new mixer as shown in **Fig. (6),** is derived from the basic Gilbert multiplier, and is based on two techniques: A CMOS transistor pair is instead applied to the four cross-coupled commutating transistor M1 to M8 (the first technique) **[7]** then the additional dc current is fed through the current sources that are long channel PMOS transistors M9 to M12 (second technique called current boosted technique) **[8]** The implemented mixer utilizes large long channel PMOS transistors. They are biased into saturation region acting as current sources thus providing the bias current for mixer core with negligible effect on the total noise performance. Hence the use of

high impedance load is enabled. By current boosting, a lower mixer noise figure is achieved without deteriorating the linearity.

The additional dc current is feed through the current sources that are long channel PMOS transistor (M9, M10,M11,M12) to the source of NMOS transistors (M1,M2,M3,M4).

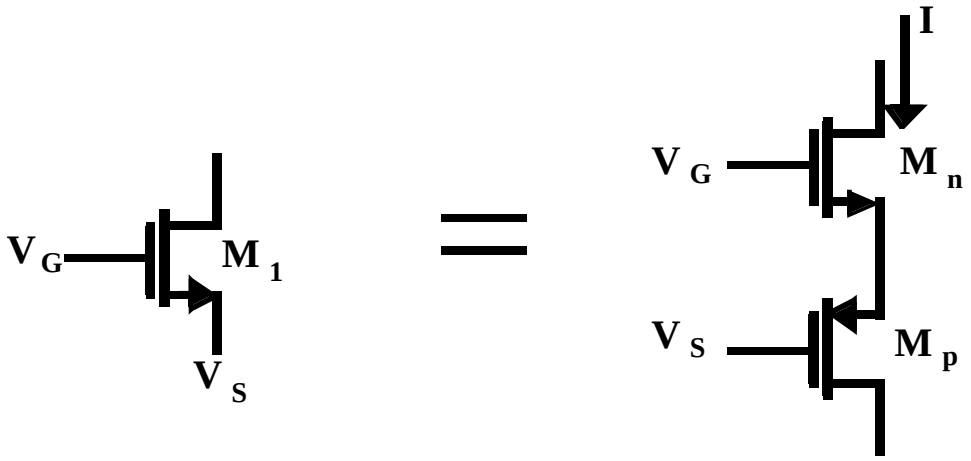
A device selection of the additional current sources is one of the most specious design steps in this topology. These current sources are significant noise contributors that ensure that the current sources exhibit as small gm as possible. The amount of additional noise is minimized as their thermal noise floor is suppressed. Large source degenerated PMOS transistors can be used as current source. However, the resistor degeneration is noisy by itself and does not decrease the gm of the current source device enough. Better performance can be achieved using small long channel PMOS devices as current source.

The frequency spectrum of the proposed circuit after using bandpass filter is shown in **Fig. (8).** The time domain simulation shown in **Fig. (9).** If we want to select the lower side band we must use high order low pass filter.



Figure(6): *Proposed mixer*

In the presented mixer, the CMOS pair shown in **Fig. 7** is used as a composite transistor to isolate the RF signal. The CMOS pair behaves like a single transistor with



***Figure(7):** CMOS Pair*

Where :

$$I=I_D=\beta_{eq}/2(V_G-V_S-V_{teq})^2 \quad (3)$$

$$, \quad \frac{1}{\sqrt{\beta}}=\frac{1}{\sqrt{\beta_n}}+\frac{1}{\sqrt{\beta_p}} \quad (4)$$

$$\text{and } V_{teq}=V_{tn}+|V_{tp}| \quad (5)$$

This is under condition that $V_G-V_S > V_{teq}$.

Where $\beta_n=\mu_n C_{ox} W/L$, $\beta_p=\mu_p C_{ox} W/L$, V_{tn} is the threshold voltage of NMOS transistor and V_{tp} is the threshold voltage of PMOS transistor.

6. Analysis:

Assuming that all transistors are identical and in saturation region, the currents of the transistors are expressed as:

$$I_1= \beta/2(LO^+-RF^+- V_{teq})^2 \quad (6)$$

$$I_2= \beta/2\ (LO^--RF^+- V_{teq})^2 \quad (7)$$

$$.I_3= \beta/2\ (LO^- -RF^-- V_{teq})^2 \quad (8)$$

$$I_4= \beta/2\ (LO^+-RF^-- V_{teq})^2 \quad (9)$$

The output can be expressed as:

$$IF=IF^+-IF^-= ((I_2+I_4)-(I_1+I_3))\ R_L=\beta\ R_L\ (LO)\ (RF) \quad (10)$$

Where $LO = LO^+ - LO^-$ and $RF = RF^+ - RF^-$

$$IF/\ R_L =\beta/2(LO^+-RF^-- V_{teq})^2+ \beta/2\ (LO^--RF^+- V_{teq})^2-\beta/2(LO^+-RF^+- V_{teq})^2 -\beta/2(LO^--RF^-- V_{teq})^2 \quad (11)$$

$$IF/\ R_L = (\beta/2(LO^+-RF^-- V_{teq})^2 -\beta/2(LO^+-RF^+- V_{teq})^2) + (\beta/2\ (LO^--RF^+- V_{teq})^2 -\beta/2\ (LO^- -RF^-- V_{teq})^2) \quad (12)$$

$$IF =\beta/2((LO^+-RF^-- V_{teq}- LO^++RF^++ V_{teq})\ (LO^+-RF^-- V_{teq} + LO^+-RF^+- V_{teq}) + (LO^- -RF^+- V_{teq}- LO^- - RF^++ V_{teq})\ (LO^--RF^+- V_{teq} + LO^--RF^-- V_{teq}))\ R_L \quad (13)$$

$$=\beta/2((-RF)\ (2\ LO^--RF^+-RF^- -2\ V_{teq}) + (RF)\ (2\ LO^+- RF^-- RF^+-2\ V_{teq}))\ R_L \quad (14)$$

$$= \beta/2((RF)\ (2LO^+- RF^-- RF^+-2\ V_{teq} -2\ LO^-+RF^++RF^- +2\ V_{teq}))\ R_L \quad (15)$$

$$= \beta/2((RF)\ (2LO))\ R_L \quad (16)$$

$$= \beta\ (RF)\ (LO)\ R_L \quad .(17)$$

7. Simulation results:

In order to demonstrate the proposed mixer, the simulation was done using PSPICE simulator in the standard 0.8 μm CMOS technology .The simulation was done by using 25MHz carrier frequency (The frequency of the LO), 1GHz RF frequency, 0.2V peak-to-peak amplitude, and a single 2.5V supply voltage.

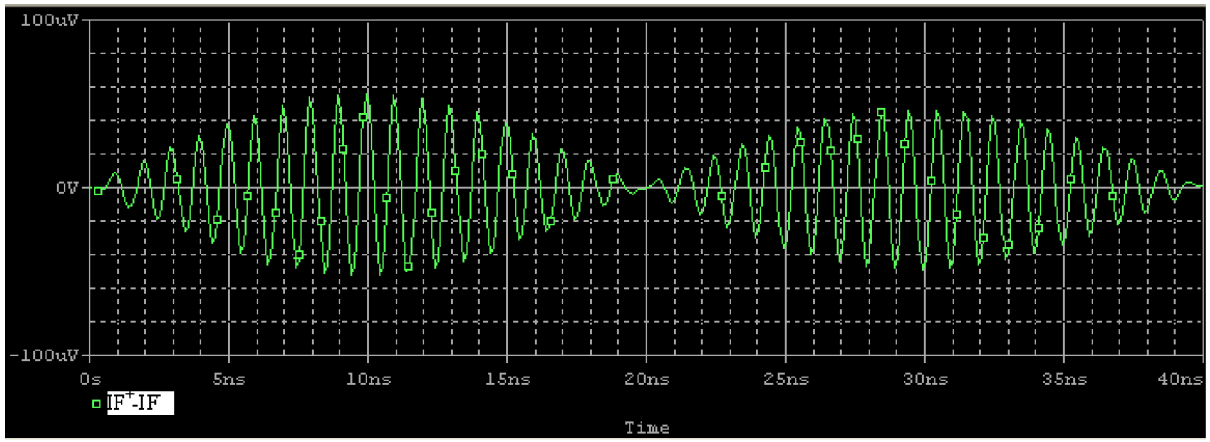
The IF frequency which resulted from down conversion mixer is 975MHz, the other frequency (1.025GHz) is rejected by low pass filter.

these results are equivalent to our analysis where

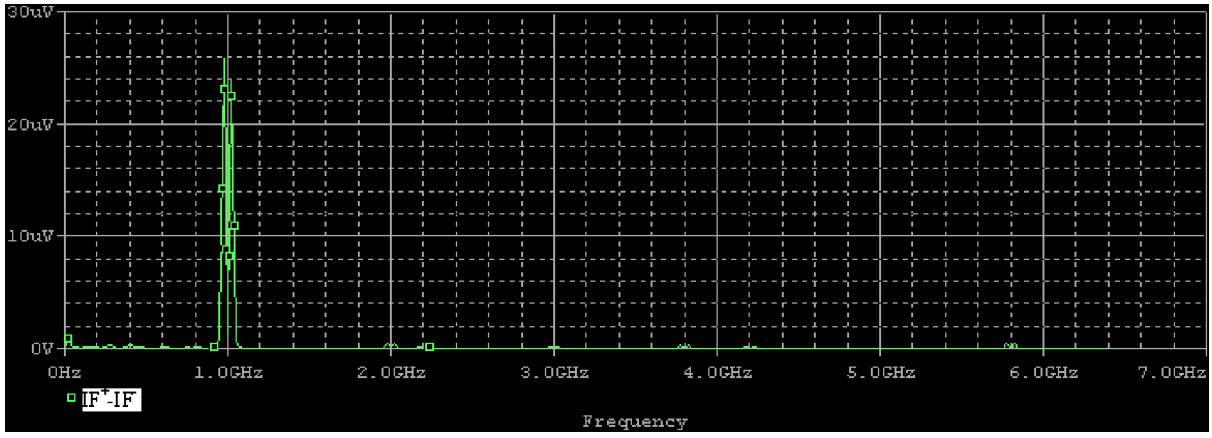
$IF=IF+-IF^{-} = \beta$ RL (LO) (RF) (18)

LO=0.2sin (2Π*10^9t) (19)

RF=0.2sin (2Π*25*10^6t) (20)



Figure(8) *Time domain simulation*



Figure(9): *Frequency domain simulation*

***Table(1):** Simulated results of proposed mixer compared with second technique and current boosted mixers*

	First technique mixer [4]	**Proposed mixer [This work]**
Supply voltage	2.5V	2.5V
RF input frequency	1GHz	1GHz
LO input frequency	25MHz	25MHz
IF output frequency	975MHz	975MHz
Power dissipation	3mW	2.3mW
Technology	0.8μm CMOS	0.8μm CMOS

8. Conclusion:

A low voltage, low power downconversion mixer is proposed in this paper. A new principle for minimization the power of RF mixer using two techniques was introduced. A specific biasing technique is adopted to guarantee the very low-voltage operation and it is obvious that the down conversion is not limiting the flexibility of direct conversion receiver for multi mode applications. Simulation of the proposed circuit was done using pspice simulator in standard 0.8um CMOS technology. The simulation was done using 1GHz RF signal. The LO is amplitude modulated by a 25MHz, 0.2V peak-to-peak amplitude signal, and the IF frequency which resulted from downconversion is 975 MHz. a single 2.5V supply were used. The power consumption of the proposed downconversion mixer is 2.3mW.

9. References:

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Nomenclatures:

AM	Amplitude Modulation
CMOS	Complementary metal oxide semiconductor.
FM	Frequency Modulation
IF	Intermediate Frequency
LO	Local oscillator
NMOS	N-Channel MOSFET.
PMOS	P-Channel MOSFET.
RF	Radio Frequency.
SPICE	Simulation Program with Integrated Circuit Emphasis.
V_T	Threshold voltage
F	Frequency
λ	Wave length
μ	Mobility
C_{ox}	Oxide Capacitance
β	Transistor gain factor
L	Inductance
C	Capacitance
R	Resistance