Military Technical College
Kobry El-Kobbah,
Cairo, Egypt

6th International Conference
on Electrical Engineering
ICEENG 2008

Hardware realization and implementation of neural network

By

* Dr. Abdelelah Kidher Mahmood

Fares Hassan Taha **

Abstract:

In this work the neural network is realized by use of operational amplifiers and electronic devices. The structure of neural network like the neuron and weights function and activation function has been implemented by simulation in (multisim software) simulator .

The result , show good fulfillment of a neural network with analogue hardware devices

Keywords:
Neural network, hardware realization .

---

*Department Of electrical Engineering
University Of Mosul

** Department Of electrical Engineering
University Of Mosul

1- Introduction

The neural network is an intelligent technique which can be used in signal processing and signal condition and recognition. It may be implemented and realized by two methods, one is by analogue devices which realize the continuous time signal processing and conditioning circuit, and the other method is by digital processing or discrete signal processing. Which realized by software .The analogue devices like operational amplifiers and combination of CMOS or FET transistor can be implemented to realize the architecture of the neural network.The previous work on this method (topics) are in two categories: one by use of (CMOS) [1]transistor to construct a signal chip processing the other are uses operational amplifiers.[2]

In this work a multisim software is used to perform and realize each part of neural network, a back propagation is used to self adjust the weights of neural network.

2- Basic neural network

In general any artificial single layer neural network has a structure shown in fig (1) with P1- Pn are input connected to the neuron body through weights W1,W2, ------Wn .The neuron output is function of inputs and associated weights as shown in following equations [3].

$Yo = PW - b$,

where $P = [P1\text{----------}Pn]$ input vector to the neuron (1)

$W = [W1\text{----------}Wn]$ weight matrix

$Yo = P1W1 + P2W2 + \text{----------} PnWn - b$, b bias threshold level

The output is entered to the activation function which may be linear or nonlinear function.

$Yn = f(y_o)$

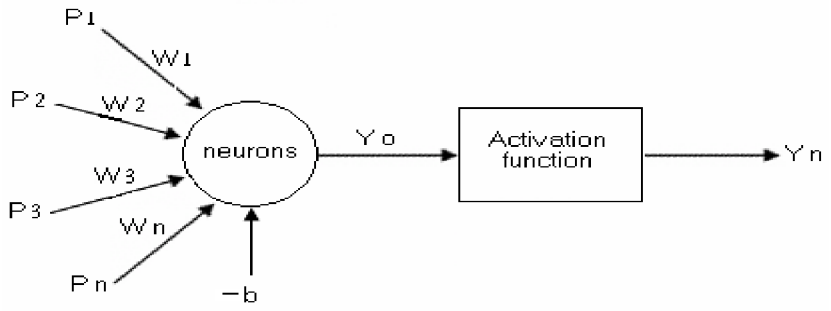


Fig (1)

To implement each part of neural network by analogue devices like the weight and the neural body and the activation function, first the each part is realized and tested individually, the overall is constructed later.

3- The analogue circuit implementation of neural network

The analogue circuit that implemente the simple neural network can be build with operational amplifier as shown in fig (2), where the inputs are P1----P3 and weight function is produced by the ratio R1/Rx, and the output of operation amplifier is given as:

$$U = \frac{R_1}{R_{X1}} P1 + \frac{R_1}{R_{X2}} P2 + - - - - - - - \frac{R_2}{Rxn} Pn \qquad (2)$$

This outputs is becomes inputs to the activation function, which in this case linear type.

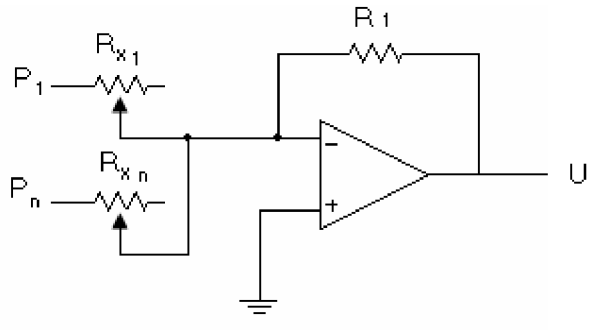


Fig (2)

4 – The weight function implementation

The weight function can be realized with different methods:

4-1 Potentiometer as weight function.

For simple neural network without back propagation a potentiometer can be used for useful purpose, as in fig (2) . The potentiometer adjust manually , and in case of back propagation , aservo motor or steper motor can be utilized to adjust the resistance value as a position control.

$R = f(\Theta)$ (3)

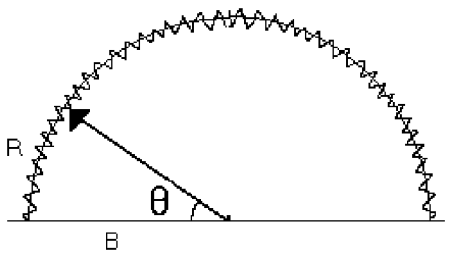


Fig (2)

4-2 Capacitor storage method

The weight function can be also implemented by use of capacitor , The voltage across the capacitor when it charged is function of charge current and voltage across it.

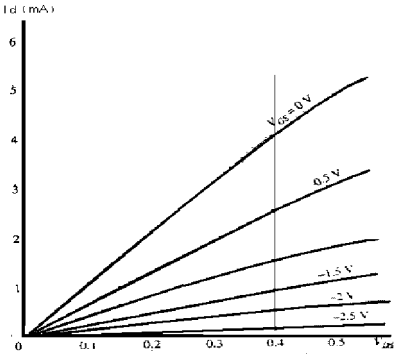
4-3 Field effect transistor (fet) as voltage controlled weight function

The drain source voltage Vds and drain current Ids characteristic of fet transistor that shown in fig (3) for various value of gate to source voltage Vgs , By choosing the linear region of these characteristic the resistance between drain and source given by [4]

$$R_{DS} = \frac{V_{DS}}{I_D} \Big\|_{GS} \qquad (4)$$

The resistance value is given in the table (1) for fixed VDS = 0.4 and for VGS between 0 to – 2.5v , Theoretically the resistance is given as :

$$R_{DS} = \frac{Ro}{(1 - \frac{V_{GS}}{V_P})^2} \qquad (5)$$



Where Ro is the minimum resistance value when VGS = 0
Vp is the pinch off voltage of the transistor

Fig (3)

V_{GS} (v)	0	- 0.5	-1	-1.5	-2	-2.5
R_{DS} (Ω)	100	160	267	444	800	3.3k

Table (1)

5 - Neuron implementation using FET transistor

The circuit diagram for the weight function using field effect transistor FET is shown in

figure (5) , the out put voltage is given as,

$$Vo = -\frac{Rf}{Rds} Xi \qquad (6)$$

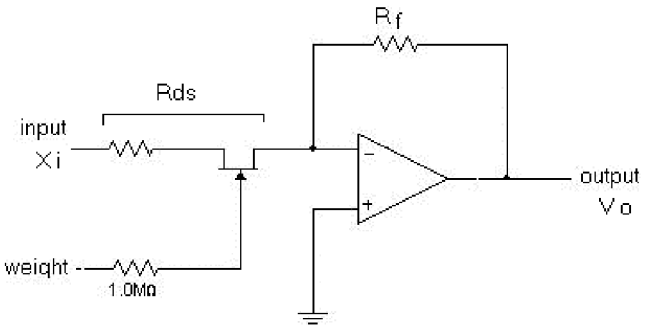


Fig (5)

5 – 1 Neuron weight adjust

The neuron weight can be adjusted by change the gate to source voltage of the FET transistor V_{GS} then the output can be expressed as:

$$Vo = -\frac{Rf}{Rds} Xi$$

$$Rds = -\frac{Rf}{Vo} Xi$$

using expression (5) then output voltage

$$Vo = -\frac{Rf}{Ro}(1-\frac{V_{GS}}{V_P})^2 X_i$$

$$Weight(W) = -K(1-\frac{V_{GS}}{V_P})^2$$

Where K is constant (7)

5 – 2 Building the neural network

The neuron is built using field effect transistor type N channel and operational amplifier.[5] The weight versus voltage V_{gs} is plotted in figure (6) this characteristic can used to adjustthe weight of the neural by chosing appropriate Vgs .Figure (7) shows 3 input neural network realization as in is construct of three neuron and adder.

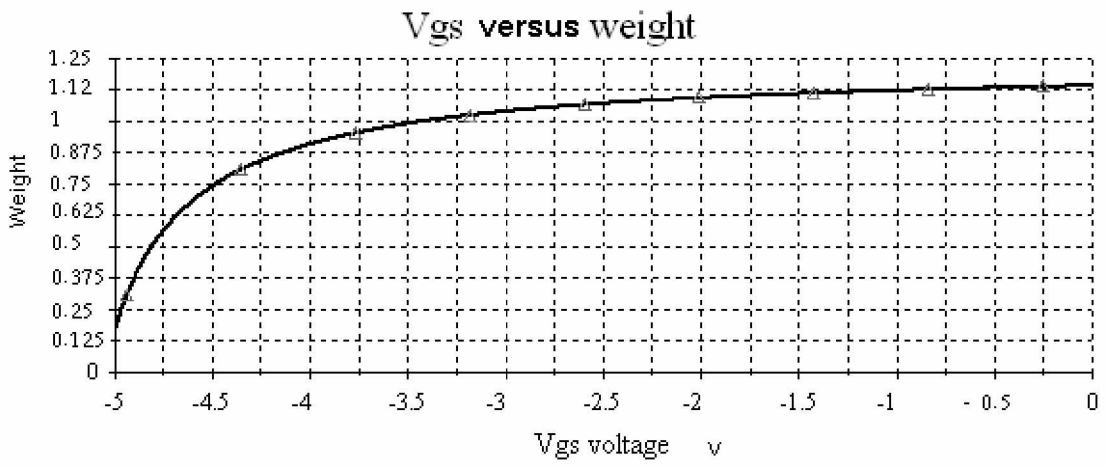


figure (6)
The relation ship between weight (W) and V_{GS}

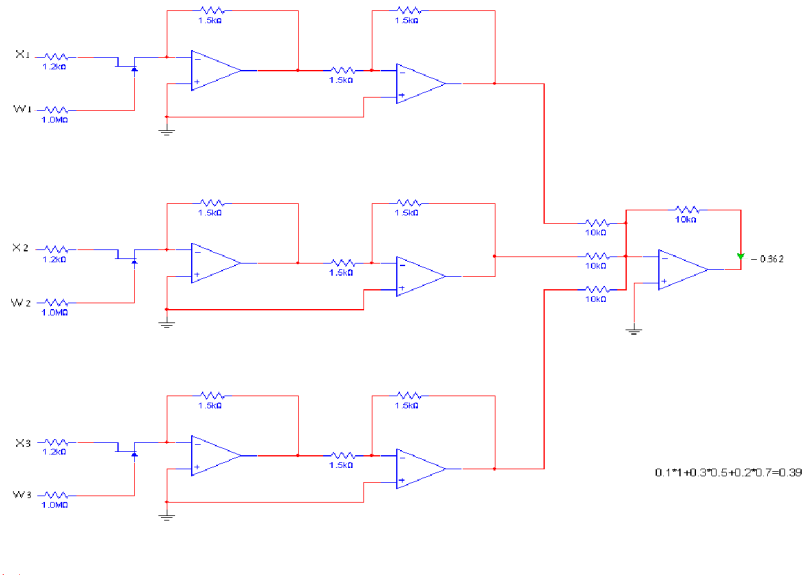


Figure (7)
Three input neural network practical circuit

CONCLUSION:

The practical circuit has been built in this paper for very simple three input neural network which is a cheep devices that is only one chip of operational amplifiers and a little component are used. This network is useful and easy so it can be implemented generally any neural network.

Field effect transistor FET characteristic between drain and source can be utilized in the linear region to be as voltage controlled weight function of neural network. Self adjustment of the weight can be done via gate source voltage Vgs .

Any self-taught net with more than a few dozen neurons is virtually can be realized and constructed.

Reference

[1] Jin liu." Fully.Parallel Learning Neural Network Chip For Real-Time Control ". Ph. D. Thesis Presented to the Academic Faculty, School of Elect. & Comp. Eng. Georgia Inst. of Tech. 1999.

[2] B. M. Wilamowski, J. Binfet, and M. O. Kaynak. "VLSI Implementation of Neural Networks" 24th IEEE Int. Industrial Electronics Conference IECON98. 31 Aug. – 4 Sept. Achen, Germany, Vol. 1, pp. 35-149.

[3] Wikipedia, the free encyclopedia,"Neural network". http://en.wikipeda.org

[4] Robert L. Boylestad, Louis Nashelsy. "Electronic Devices and Circuit Theory".MagroHill.2000

[5] Ronald S. Burns, "Advanced Control Engineering" .Printec.Hill.1998.