Military Technical College
Kobry El-Kobbah,
Cairo, Egypt

6th International Conference
on Electrical Engineering
ICEENG 2008

Characterization and modeling of novel large gate periphery InGaAs/ InAlAs pHEMT for ultra low noise radio astronomy applications

By

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Abstract:

Novel high breakdown 1 µm strained gate InGaAs-InAlAs-InP pHEMTs with different gate periphery have been fabricated. Their DC, RF, and noise performances have been successfully characterized for investigating the optimum gate area for the best noise performance in the L-band. Extensive experimental device characterization together with numerical simulations using suitable linear and non-linear transistor models has been carried out for the new devices. Excellent agreements with experimental data were found on different transistor processes. DC, RF, and noise behaviours of the new devices were successfully modeled.

Keywords:

Modeling, pHEMT, InGaAs/InAlAs, Low noise

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1. Introduction:

Due to their excellent microwave noise performance, the InP-based InGaAs/InAlAs pHEMTs are promising candidates for the next generation ultra-high-speed wireless, optical communication, and space-born applications. However, the selection of the right transistor is crucial step in the design and fabrication of front-end low noise amplifiers (LNAs) for radio astronomy applications. One of the most important parameters that control the noise behaviour of the transistor is the noise resistance Rn. Actually Rn plays a very important role in the design of LNAs because it measures the level of noise factor deterioration with increasing mismatch. Small Rn value is always preferred because it indicates a relatively insensitive system; in terms of noise level variations, and also facilitates the circuit design because of the reduced mismatch between NF and NFmin. In order to investigate the optimum gate size for the lowest possible noise resistance in the L-band, a family of InP-based InGaAs-InAlAs pHEMTs with different gate periphery (up to 800 μm) have been fabricated and measured. Extensive experimental device modeling, together with numerical simulations using suitable linear and non-linear transistor models has been carried out for characterizing the DC, RF, and noise performance of the devices.

2. Experimental Work:

The structure under investigation was grown in-house using solid-source Molecular Beam Epitaxy (MBE) on an Oxford Instruments V100H system (sample XMBE-106). Considering the epitaxial structure from bottom to top, an InAlAs buffer layer was grown on top of lattice-matched InP semi-insulating substrate. Above the buffer a strained In0.7Ga0.3As active channel, thin undoped InAlAs spacer, δ-doped InAlAs supply, and undoped InGaAs cap layers were grown on top of each other. More details about the epitaxial structure and processing technique used can be found in **[1]**.

Based on this composition, devices of different gate geometry have been fabricated, with two gate fingers of width 100μm to 400 μm each and gate length of 1 μm.

In this work, two different modeling techniques were employed to characterize the performance of fabricated devices namely, the commonly used small-signal linear model and the EE-HEMT nonlinear large signal model. The linear small-signal models parameters were analytically extracted from the measured S parameters **[2]**. The 7 intrinsic model parameters were obtained from hot (active) device bias setups, while the 8 extrinsic (parasitic) elements were obtained from cold (pinched) device measurements. The equivalent circuit of the linear model is shown in Figure 1. The final element values for this model were determined by applying CAD optimization techniques to the initial values obtained, until the model accurately fitted the measured data.

Also, aided by the modeling and measurement automation software package, IC-CAP, the EE-HEMT large-signal nonlinear models of the fabricated devices were extracted and optimized using the Agilent's ADS in order to fit the measured date.

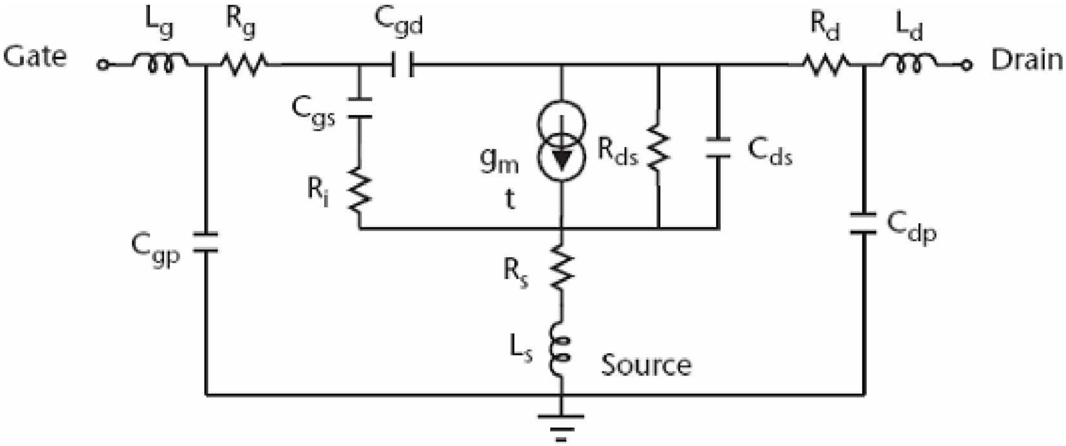


Figure: *(1) Linear small-signal equivalent circuit model of the fabricated devices*

3. Results and Discussion:

Figure 2 shows a comparison between the measured and modeled transistor DC characteristics extracted using the non-linear model. Excellent agreement has been found between the two sets of data, which tends to confirm the validity of the non-linear model. However, slight deviations may be found at low drain-source voltages that are due to the fact that the kink effects are not taken into account in the model.

Figure 3 shows the measured and modeled S-parameters as a function of frequency. Again, very good agreement obtained between linear model, non-linear model and measured data. The very good match obtained for the 3 data sets of the device characteristics tend to reinforce the validity of the linear and non-linear models.

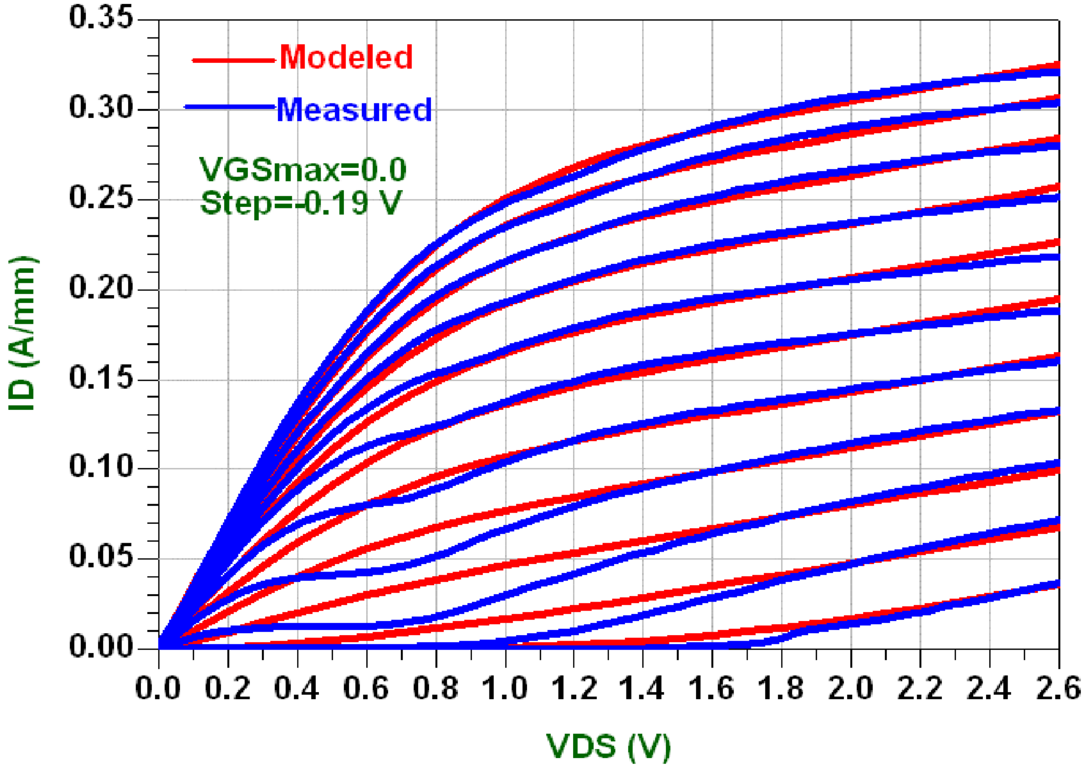


Figure: *(2) Modelled and measured DC I-V curves for the 2×100 µm InGaAs/InAlAs pHEMT. The intensity has been normalised to 1 mm.*

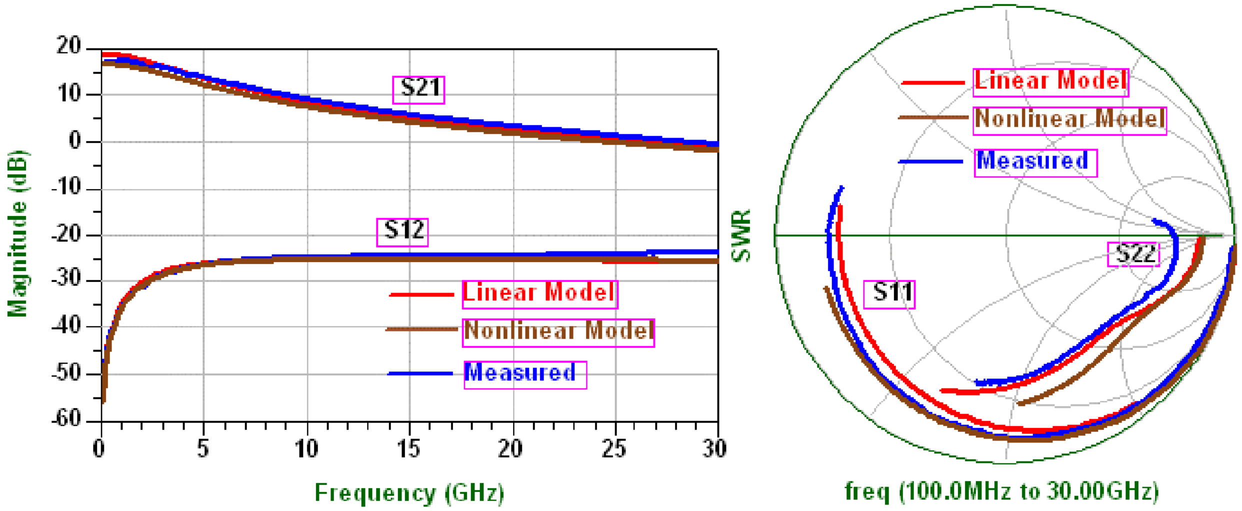
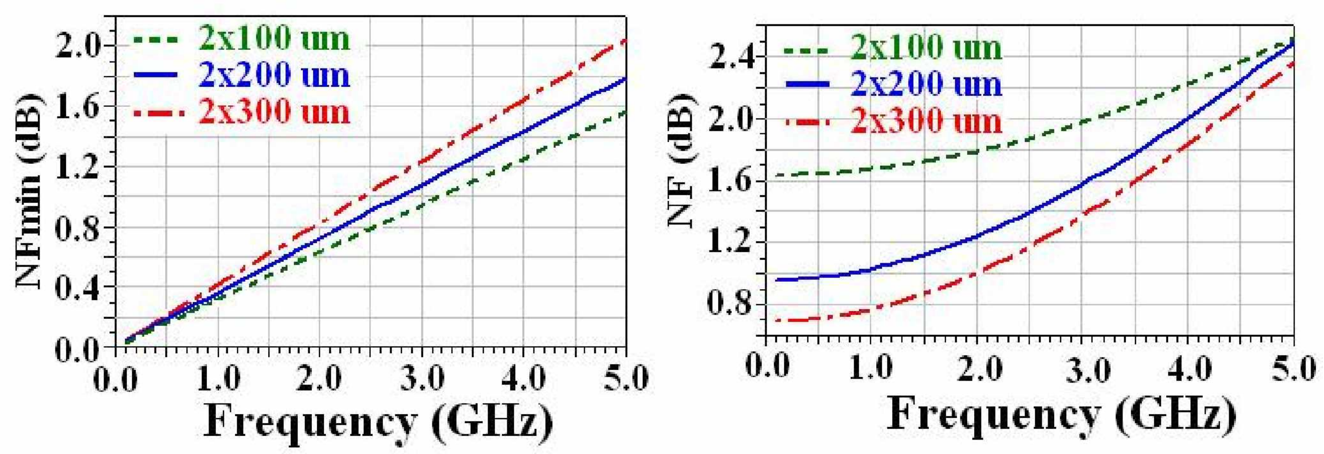


Figure: *(3) Modelled and measured S-parameters for the 2×200 µm InGaAs/InAlAs pHEMT.*

The noise characteristics have been extracted from the non-linear model, as shown in Figure 4. At 2 GHz, the minimum noise figure NFmin reaches 0.63 dB, 0.72 dB and 0.83 dB for the 200 µm, 400 µm and 600 µm gate width devices, respectively. These values are in excellent agreement with those calculated from the linear model using Fukui's analysis **[3]**.



(a) ***(b)***

Figure: *(4) Evolution of NFmin (a) and NF (b) as a function of frequency for three fabricated InGaAs/InAlAs pHEMT of different gate width at room temperature. The data have been extracted from the non-linear models.*

NFmin increases with increasing frequency. Figure 4(b) shows the evolution of the noise figure NF for the same devise as a function of frequency. At 2 GHz, NF reaches 1.8 dB, 1.25 dB and 1.0 dB for the 200 µm, 400 µm and 600 µm gate width devices, respectively. The noise figure is improved when the device is widened.

The opposite trend in the evolution of NFmin and NF with the gate width is due to the change in the noise resistance of the devices, as shown in figure 4. This parameter shows that at low frequency (below 2GHz) the noise performance of the transistor is dictated by its noise resistance Rn rather by NFmin only. On the other hand, Rg increases with increasing gate width and increases NFmin. Therefore, in order to reach ultra low noise at low frequency (below 2GHz), increasing the gate width together with keeping Rg low is the key.

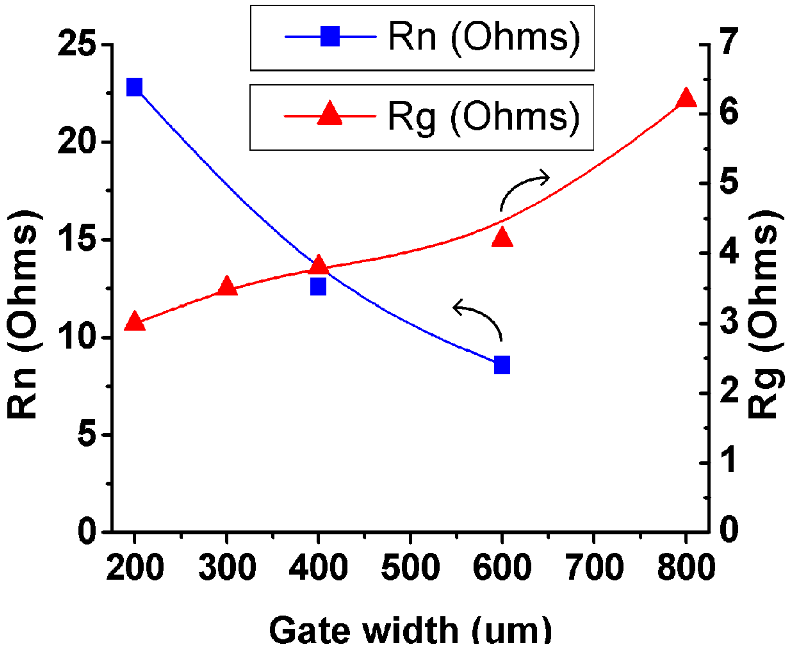


Figure: *(4) Evolution of the noise resistance Rn (squares) and gate resistance Rg (triangles) as a function of the gate width for the fabricated InGaAs/InAlAs pHEMTs. (Note: Lines are guides to the eyes)*

4.Conclusion:

Device modelling was performed on InP-based InGaAs/InAlAs pHEMTs fabricated with various gate widths. Excellent agreement between the measured and modelled data was obtained for DC and RF characteristics using the linear and non-linear models. It is shown that increasing the gate size leads to better NF at low frequency which is attributed to Rn. Larger devices could be the key to low cost ultra low noise performance required for radio astronomy applications. The use of air-bridges (multi-gate fingers) on large devices would be beneficial in reducing Rg and Rn, and is now being investigated.

References:

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