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Digital Testing of Analog Circuits

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Abstract

This research exploits digital techniques to test analog circuits. A novel test methodology and an optimization algorithm to generate the stimulus have been developed. The aim is to detect as many manufacturing defects as possible, which might occur during the production process of mixed-signal systems. The test stimulus is a discrete-interval binary sequence identified by the optimization algorithm. Response from the analog circuit under test (CUT) is digitized with one-bit resolution by a comparator. Digitized responses from the actual circuit and from fault-free simulation are compared for fault recognition. A figure-of-merit, to measure the ability of a specified binary sequence to detect all possible faults, is defined. Input sequences with good performance will generally be too long to permit exhaustive search of all candidates. Instead, iterative optimization is employed. An optimum sequence has been discovered when no further modification can improve the figure-of-merit. This process of optimization is performed with computer-based simulation of the circuit under test. Consequently, faults and tolerances can be introduced as required and all aspects of behavior can be modelled under controlled conditions. The digitized response of the optimum sequence is stored to be used in actual test application. The methodology has been validated using analog filter. All catastrophic and parametric (deviations of component values from nominal by more than six times the normal tolerances) failures can be detected, with detection probability greater than 98%. Benefits of the methodology include ease of introducing binary signals to analog subsystems and reduction of the hardware required for both stimulus generation and response processing.

Keywords

Analog testing, Analog test stimulus, Binary sequences, Digital testing, Fault detection, Hamming distance, Mixed analog–digital integrated circuits, Optimization of Binary sequences, Testing.

Introduction

An approach to avoid using two separate testers for mixed-signal systems is to test analog functions using digital-based techniques. These techniques can be categorized into two main divisions: digital modelling of analog circuits; and the use of digitally compatible signals (e.g., binary signals) as stimuli [1]. Fig. 1- Summarizes possible analog and mixed-signal test strategies according to the type of measurement and method of accessing the CUT inputs/outputs. It should be noted that both specification-based and fault-based testing could be applied for any test methodology depicted in Fig. 1- The bold path in Fig. 1- Represents the rout of the proposed test methodology.

Digital modelling of analog circuits requires the transformation of the analog CUT into an equivalent digital circuit. The well-established digital test generation techniques are then applied to the transformed circuit. There are two main approaches for testing analog circuits using digital modelling [2]. In the first approach an equivalent circuit is used to generate suitable test sequences, and then these sequences are applied directly to the CUT. In the second approach, the digital test sequences are converted to analog waveforms and then applied to the CUT. This technique suffers from the following main drawbacks:

- The inaccuracies associated with transforming analog circuit behavior to digital circuitry. These inaccuracies are further increased because there is no account of tolerance.
- The inability to fully exercise the analog functions, s ince it targets only catastrophic faults.
- The lack of suitable digital equivalent circuits for mo st analog blocks.

Several methods (Table 1) for testing analog and mixed-signal circuits using binary test signals have been developed for fault detection or location. Impulse, step, square wave, or Pseudorandom Binary Sequence (PRBS) are examples of binary test signals [3], [4], [5].

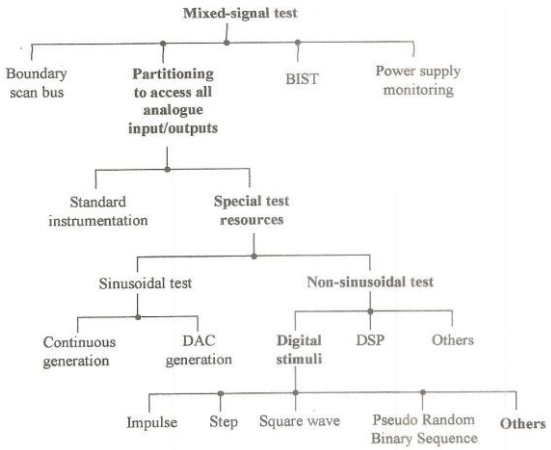

Fig. 1- Broad summary of mixed-signal test strategies

Table 1- Comparison between digital-based methods of analog testing [6], [7]

Criteria / Method	Spectrum of the test signal	Characteristics of the test signal	Stimulus generation: Hardware	Stimulus generation: Complexity	Response processing: Hardware	Response processing: Complexity
Impulse response		-The CUT May overload. -Constant spectrum	-Arbitrary function generator -LFSR and Multi-convolution	-Low -High	-ADC and cross-correlator	-High
Step response		-Constant spectrum	-Arbitrary function generator	-Low	-ADC	-Low
Square wave		-Odd harmonics only	-Arbitrary function generator	-Low	-Has not been proposed	
PRBS		-Fixed shape and variable scaling of the spectrum	-LFSR -LFSR and DAC	-Medium -High	-ADC -ADC and signature analyser -A comparator and signature analyser	-Low -High -Medium

- **TEST METHOD**

As for any test strategy, the proposed test method is composed of two modes of operation: test development and test application. Development mode includes three basic steps: determination of a potential fault list (catastrophic and parametric), identification of a test stimulus of adequate performance, and storage of a reference pattern for fault detection. The input test pattern is used to derive a reference output pattern for the fault-free CUT. Every CUT
will have its unique input and output reference patterns. These circuit-dependent patterns are stored in a database for comparison purposes during test application mode.

During test application mode, a similarity or comparison measurement between the actual response and the stored reference pattern is performed. If they are sufficiently different, then the CUT will be declared faulty.

The proposed test system architecture is illustrated in Fig. 2- The input test signal is a discrete-interval binary sequence of duration N bits [8]. This input sequence is fed through a buffer from digital signal generator. The buffer matches input impedance of the CUT and scales the sequence amplitude to prevent overloading the CUT. Output analog response of the CUT is reduced to threshold crossings using comparator. The output of the comparator is either logic high or logic low depending upon result of the comparison between the CUT response and the comparator threshold. Discontinuities in the output of the comparator occur at crossing times of the threshold with respect to CUT response. The comparator output forms the output binary sequence, which is fed to the digital recording and processing block. In this block, the output binary sequence is over-sampled and compared to a reference sequence for fault detection.

For given input binary sequence, the output binary sequence for fault-free circuit is stored as a reference. For successful testing, it is required that, the faulty circuit should produce a different output sequence from the reference. The Change in output sequence due to a fault is detected by comparison with the reference sequence. One way to measure the difference between the output and reference sequences is the Hamming distance [8] between them.

The Hamming distance between two binary sequences is the number of digits in one of the two sequences that has to be changed to make it the same as the other. The simplest way to measure the Hamming distance is by counting the ones in the output of an EX-OR operation between any two binary sequences. After taking into account the effect of tolerances, if the resulting Hamming distance is greater than zero, then fault is detected.

Various fault measures (e.g. Hamming distance) for each fault are combined to form an average figure-of-merit for the given input binary sequence. Furthermore, every input sequence will have a detection ratio (ratio of detected faults to total number of faults). The figure-of-merit and/or detection ratio are related measures of effectiveness of the input binary sequence in detecting faults. The proposed technique employs an analog figure-of-merit analogous to the digital Hamming distance, which represents quantitatively how well and how many faults are detected.

Both the input binary sequence and its steady-state response of the CUT are periodic. Therefore, after transient settling, all available information is contained within one cycle of the response. Repeated sequences of binary bits of input and reference are pre-determined in advance and stored in a PC memory, ROM or on-chip memory. These sequences can be retrieved and recycled using simple digital commands.

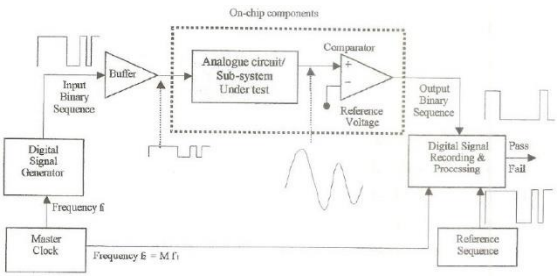

Fig. 2- Test system overview

BINARY SEQUENCES FOR TESTING ANALOG CIRCUIT

A binary sequence with predetermined characteristics (Fig. 3) stimulates fault-free and faulty CUTs. Possible faults are predefined and modelled to be used in simulation. Circuit simulation predicts behaviour of CUT for a given stimulus. Relevant properties of Issues of fault modeling can be summarized in the following points [9]:

- Single fault assumption does not lead to severe inaccuracies in determining effectiveness of a test set.
- Types of faults in analog circuits are either catastrophic or parametric.
- Using op-amps for modeling analog circuits reduces the number of faults that may occur in those circuits without scarifying the effects of most faults in internal transistors.
- The transfer function describing a faulty circuit should meet the stability criteria.
- The fault model value is chosen to ensure relatively small settling time for steady state testing.

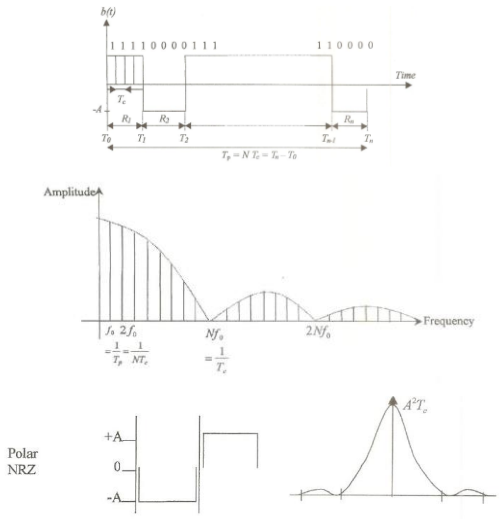

Fig. 3- Binary sequence characteristics

FIGURE-OF-MERIT OF BINARY SEQUENCES IN FAULT DETECTION

The problem of finding the best-input binary sequence that has high fault coverage will be addressed throughout the remaining parts of this paper. There are two approaches can be used to identify the best-input sequence. The first approach is evaluation of all possible and useful binary sequences of a given length. The advantage would be that obtained results will be the best possible solution to the given test generation problem. However, computations necessarily for generating and evaluating the full range of all possible and useful binary sequences are likely to be practically unfeasible. Other approaches for finding the best-input binary sequence are by an optimization algorithm. However, there is a risk that the result will be localized not a global optimum over the whole search space.

The proposed test method is composed of two modes of operation: test development and test application modes. Test application mode, shown in Fig. 4- Consists of the following steps:

- The CUT is stimulated by an optimized input binary sequence.
- The comparator is set at an optimized threshold level.
- Hamming distance (Number of different bits) between the actual one-bit quantized response (binary sequence at output of the comparator) and reference output binary sequence(s) is calculated.
- Reference output binary sequence is the one-bit quantized response(s) of a good CUT to the optimized input binary sequence.
- After considering tolerances, a non-zero Hamming distance indicates that the tested CUT is faulty.

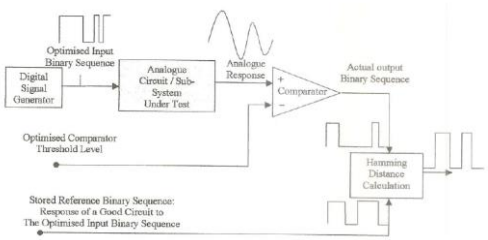

Fig. 4- Block diagram of test application mode

In development mode, optimization procedures are made to identify a robust binary sequence(s) and associated comparator threshold level(s). Optimized binary sequence(s) should be capable of detecting most of all possible faults within an analog CUT. The optimization procedure aims to find an optimum input binary sequence(s) for detecting faults. In development mode, optimization procedures are made to identify a robust binary sequence(s) and associated comparator threshold level(s). Optimized binary sequence(s) should be capable of detecting most of all possible faults within an analog CUT. The optimization procedure aims to find an optimum input binary sequence(s) for detecting faults. Differences between good and faulty behaviours are combined to form a composite figure-of-merit. This figure is a measure of effectiveness of that binary sequence in detecting all faults.

Fig. 5- illustrates generalised block diagram for measuring the figure-of-merit of a binary sequence as a test signal. This block diagram is a diagrammatic representation of methodology that is implemented in software. Therefore, whilst it shows blocks of components such as adders and comparators, it should be appreciated that physical components are not used, but instead are modelled using computer-based software, e.g. MATLAB. For a given test stimulus (binary sequence), the goal is to evaluate how well the stimulus performs as a test for the CUT. This figure-of-merit is used to drive the search for optimal test stimulus. Sample of the results are shown in Fig. 6- The optimization procedure is discussed in the next section

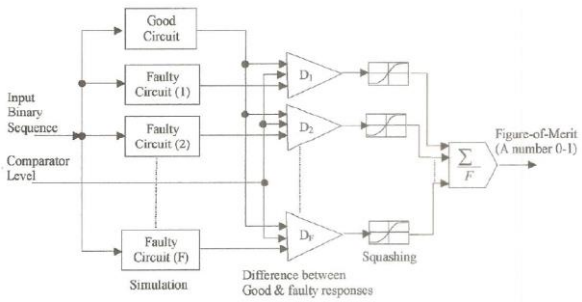

Fig. 5- Block diagram of measuring composite figure-of-merit

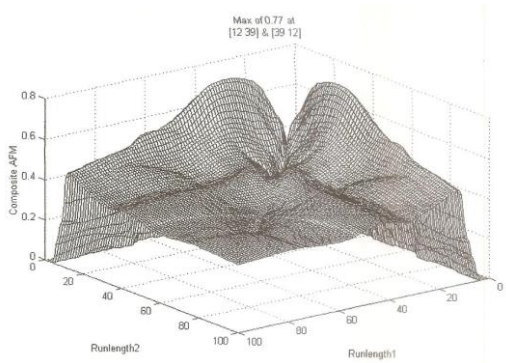

Fig. 6- Composite analog figure-of-merit using non-linear squashing of analog responses and individual fault measure in LPF, both are scaled by ten.

OPTIMIZATION OF BINARY SEQUENCES

The optimization problem has the following obvious characteristics:

- It is a complex n-dimensional problem. Each dimension corresponds to one runlength of input binary sequence [10], [11].
- Shape of the surface is completely unpredictable due to the complexity of the figure-of-merit and may have more than one peak.
- No a priori knowledge about the optimization problem is available, e.g. optimum number of variables.
- The objective function is a black box, where inputs and output are the only available information and is evaluated through computer simulation.

The above characteristics should be considered in the selection of an optimization method. The selected method may be modified to suit the specific nature of the addressed problem [12].

Hooke and Jeeves local search algorithm [13]

This pattern search algorithm represents a deterministic local optimization method that was developed by Hooke and Jeeves in the early 1960s. In addition, it is a direct search method exclusively uses objective function values to guide the optimizations process. The direction of increasing (respectively decreasing) values of the objective function is calculated according to deterministic rules without any explicit calculation of gradients. It is a widespread local optimization method because of its excellent performance characteristics. This method is modified to suit the current problem as shown in Fig. 7.

Two distinct adjustments to variables (run lengths) are made, which are defined by:

- Exploratory moves: each runlength is considered in turn, adjusted by predefined step and the composite figure-of-merit is calculated. If an improvement occurs, then the adjusted runlength is kept and the algorithm moves to the next runlength until all runlengths are explored.
- Pattern move: which exploit the directional information obtained from exploratory moves. This move is conducted only if exploratory moves

were successful in improving the composite figure-of-merit.

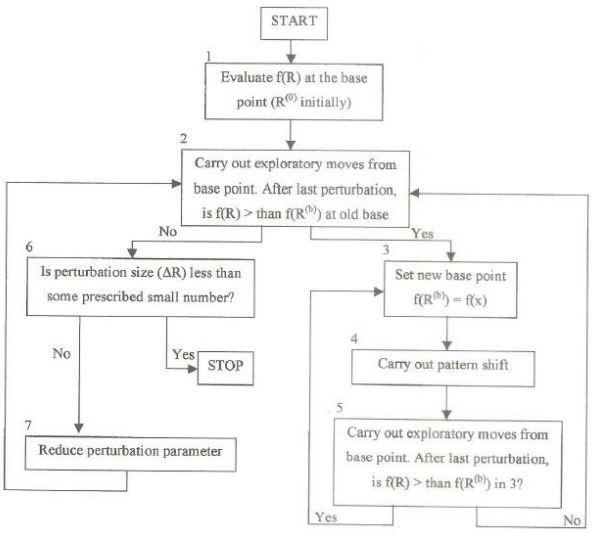

Fig. 7- Flow diagram of local search module of Hooke and Jeeves

The local search algorithm of Hooke and Jeeves is modified and implemented in MATLAB. The exemplar LPF with 20 faults is used to test the feasibility of this algorithm. It should be noted that the output comparator is set at zero voltage and the component tolerances are not included. Result of the local search algorithm is compared against that of exhaustive evaluation of two runlengths. With two runlengths, the search space is small enough to evaluate exhaustively. Therefore, the global optimum can be obtained. Different starting sequences and step sizes are used to test the efficiency of the algorithm in locating the best answer. Finally, the algorithm is compared with another simple iterative algorithm. The comparison is made with respect to the obtained result and running time, with the same starting sequence applied to both algorithms.

TEST SYSTEM EVALUATION

The proposed test strategy is simulated in MATLAB. The optimization procedure is tested against one of benchmark circuits to generate optimum binary signals with associated comparator threshold levels capable of detecting most of possible faults.

IEEE Mixed-Signal Technical Activity Committee developed a common set of benchmark circuits for use in evaluating all aspects of testing mixed-signal circuits [14]. Fault models, list of standard faults and range of acceptable component variations for these benchmark circuits were specified. Generally, benchmark circuits are used to compare effectiveness of different test methods as applied to the same type of circuits. Comparison can only be made under the condition that same fault list is used in the compared methods. The generality of a method can be achieved if a variety of circuits (different functions and realizations) is used for validation. Alternatively, if others use the same circuits for validation for their new methods, then these circuits prove the general applicability of the validated methods. Fig. 8- Shows a second order low pass active filter, Sallen-Key realization and Butterworth response, with cut-off frequency of 2 kHz. Component tolerances are ±5% around the nominal value. The gain bandwidth GB product of the op-amp is 10 MHz. Twenty faults including parametric deviation, open, and short-circuits were considered for simulation. Values of faults (shorts and opens) were chosen to satisfy the stability condition of the LPF. Table 2- Lists twenty considered faults for simulation.

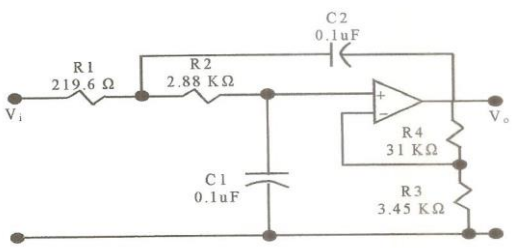

Fig. 8- Second order Sallen-key LPF with nominal component values

Table 2- Fault list of LPF

Component	Considered faults	Number of faults
R1	Short, ±30%, +60%	4
R2	Open, ±30%	3
R3	Open, ±30%	3
R4	Short, ±30%	3
C1	Short, ±30%	3
C2	Open, ±30%	3
Op-amp GB	10k	1
Total number of faults		20

Analysis of the results show that the minimum detection probability of faults is 98%. Therefore, the proposed methodology can detect all catastrophic and parametric (more than ±30% deviation) failures with detection probability greater than 98%. Fig. 9, 10- are some results.

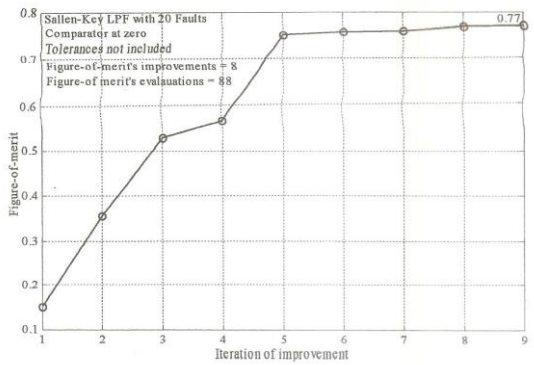

Fig. 9- Optimization of two runlengths

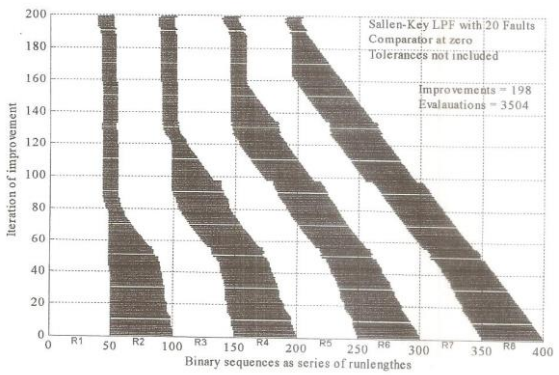

Fig. 10- Fine search optimization of eight runlengths

CONCLUSIONS AND RECOMMENDATIONS

This research, after further development, can be utilized as an automatic test generation tool for production testing of analog and mixed-signal circuits or systems. In production testing, measurements are made to decide whether an Integrated Circuit or device is functioning or not. Based on the specified test procedure, the test generation algorithm identifies an optimum stimulus to test real circuits.

There are three main research contributions [15], [16], [17]. Firstly, a new test method for analog subsystems embedded in a complex mixed-signal system has been proposed. This method is based on a novel concept for reducing complexity of test signals to binary signals at the input and output of each analog subsystem. Secondly, a robust figure-of-merit is defined to measure the effectiveness of a given input binary sequence in detecting faults within the constraints of binary signals at the input and output. This figure-of-merit is immune against irrelevant characteristics of output signals and prevents fault domination. The third original contribution has been the development of a new optimization algorithm for the test method of the first contribution. A hill-climbing optimization algorithm has been designed and implemented to find an optimum binary sequence with associated comparator threshold, which has the highest figure-of-merit, and hence the highest fault coverage.

The key results of this research can be stated by the following findings: with the specified test procedure, failures in analog circuits can be detected using binary signals at input and output; and optimization of binary sequences for the specified test procedure is possible. However, there is more work to be done to commercially exploit the proposed methodology. The recommendations for future work can be stated as:

- Realistic verification and validation
- Transient response testing
- Functional testing of analog circuits
- Reduction of development time
- Test procedure automation
- Adaptive figure-of-merit
- Clock frequency optimization
- Alternative optimization methods

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