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A digital simulator for testing over-current relay immunity against decaying DC offsets in the current waveform

By

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Abstract:

A major requirement of a protective system is to be secure. Through a proper design of both algorithm and hardware of relay circuits, a secure protection system could be achieved. However, setting of the protective relays is done according to steady state short circuit calculations; although relays are always subject to disturbances that contain transient waveforms of both voltage and current. For over-current protective relays, the decaying DC offset is one of the well known components that appear in the currents seen by the relay. Some types of relays might be affected or show a very bad response towards this DC offset; especially static and electromechanical relays. Other types, like digital relays, are expected to be more secure towards the DC offset. Even relays of the same category (i.e. static) might respond in a different way for the same current.

It is important for protection engineers to have a capability to test the performance of protective relays when a DC offset appears in the current waveform. Commercially available testers, with playback function, allow the injection of a current signal with decaying DC offset. However, this injected signal is extracted from other simulation programs such as EMTP or from recorded data. In order to test the relay using the commercially available testers, it would take a huge time and large hard disk space to accomplish the test as this requires to: create the signal, converting it to a COMTRADE format then injecting the signal (using the tester) for each possible time constant and amplitude of the decaying DC offset. These steps are then repeated for each setting of the relay; which is not practical.

This paper introduces the design of a simple and cheap relay tester based on hysteresis current control of a half bridge inverter. The tester is capable of performing a complete test of the relay behaviour towards the decaying DC offset by injecting a current signal with a variable amplitude and time constant as well as a variable steady state value of the current. The values of the amplitude and the time constant are changed according to their practical ranges. The testing program is also introduced. The test results are compared with those obtained by commercially available testers and the difference was found to be negligible. The tester can be used also for injecting steady state waveforms of current. It is suitable for usage at laboratories or relay manufacturers testing facilities.

Keywords:

Digital Simulators, Relay Testing, Transient Testing, Half Bridge Inverter, Hysteresis Control, DC Offset, Decaying DC Component, Relay Characteristics.

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1. Introduction:

Relay testers have passed through several stages. First, the testing of relays was done manually using elements like variac in order to change the injected current value. After that, a new type of testers called pre-assembled testers were used to simplify the process of testing by using power electronic elements like inverters to inject the required current. However the inverter control was done manually. Lastly, by the use of modern micro-controllers, a new type of testers were manufactured. These testers are called programmable/Automatic testers. By using this new technology the tester can test the relay automatically and accurately. It is also possible to make these testers make a sort of playing back to a recorded current or voltage waveform. This type of testing can be utilized to check the relays performance when transients occur in the power systems.

This paper will present a design and implementation of a simple relay tester of the last type (programmable/Playback). The main design factors are explained and the inter-relation between these factors is also introduced. Then, and after the practical implementation of the proposed tester, the test results of different relay types is shown and compared to those obtained by the already existing commercial testers. Although the design is simple, it satisfies the general specifications of relay testers. This simplicity makes the tester of less price and more reliability.

2. Automatic Relay Testers:

Figure (1) [1] depicts the general block diagram of automatic/digitalized relay testers. The PC is mainly used for one of two purposes: to set the value of the current to be injected or to send a waveform of the current to be played back by the power amplifier. The I/O interface receives the response of the relay (Trip).

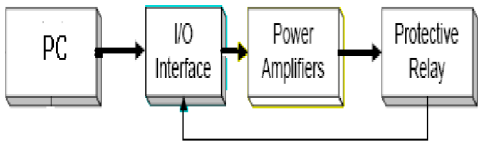

Figure (1): *General Block Diagram*

Power amplifiers are the current or voltage amplifiers that can inject high value of current or voltage in the relay coil. However, current amplifiers are only considered within the following explanation.

2. Specifications of Power Amplifiers:

Reference [2] shows the typical specifications required the power amplifier. In the paper proposed here, the maximum output current and total harmonic distortion (THD) ratings will be taken into account for the implementation of the hardwired proto-type. Other data in the specifications will be considered in further modifications of the proto-type.

3. Main Blocks of the Current Source Circuit:

The main circuit of the current source is a half bridge inverter with hysteresis current control technique [3]. Figure (2) depicts the block diagram of the tester. Each block is made out of either existing lab modules or is assembled using commercially available components like op-amps, resistors, micro-controllers,...etc.

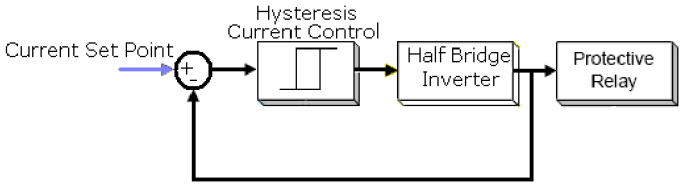

Figure (2): *Building Blocks of the Current Source*

The current set point shown in Figure (2) is generated by a digital to analogue converter (DAC). The DAC receives its digital input from a PC connected to it. A general set point waveform is shown in Figure (3).

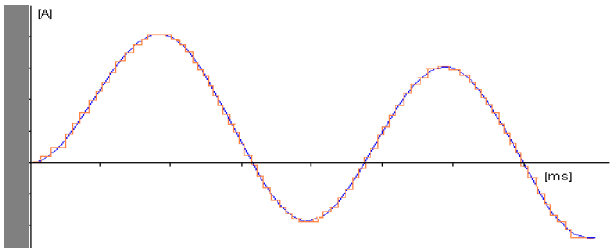

Figure (3): *General Set Point Waveform*

It should be noted that:

1. The step size is dependent on the number of bits of the digital to analogue converter.
2. The hysteresis current control circuit and the half bridge inverter have to trace each step of the reference waveform.
3. The output current (at the protective relay terminal) should satisfy the specification requirements.

3. Design Parameters:

Figure (4) shows the half bridge inverter circuit where several parameters or variables should be carefully designed so as to fulfill the specifications requirements.

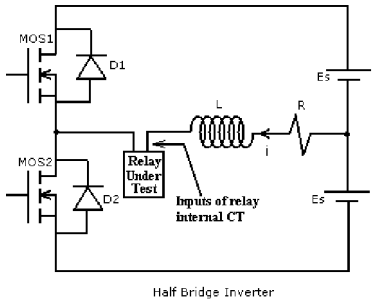

Figure (4): *Half Bridge Inverter*

The parameters or variables to be designed include: R, L, f_{MOS}, s, V_{sr}, I_{sr} and h. All parameters are dependent on each other, so the change of any of them will affect the rest; hence, will affect the THD. And so, with a simulation tool like SIMULINK it is possible to study the effect of the different parameters on each other or on the THD.

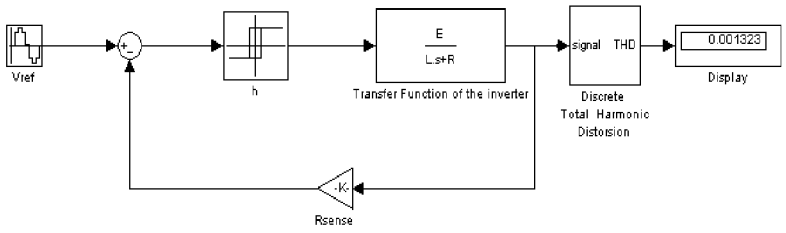

Figure (5): *SIMULINK Equivalent Circuit*

By using the current control circuit in Figure (5), it is possible to change the values of the different parameters and evaluate their effects.

At the beginning, the values of R and L only will be varied because their values have a major effect on the value of THD. This fact is supported by Figure (6) where it is clear that an intersection area between the required waveform (reference) and the actual waveform might result if R and L are not properly selected. This intersection area makes the waveform highly distorted. During this period of intersection the half bridge inverter is not capable of delivering current equal to the reference value. This might occur due to the high value of L. The intersection area gets higher as L increases.

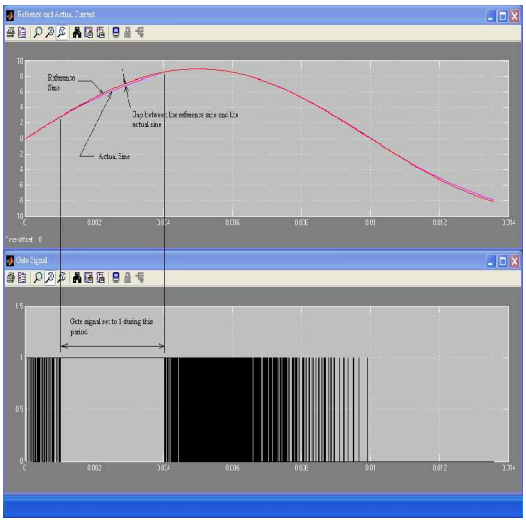

Figure (6): *Intersection Area*

It is then required to get, for each value of R, the maximum permitted value of L after which intersection would occur. The value of the used L in the actual circuit should be then less than this maximum value. Figure (7) [1] depicts the relationship between R and L.

The relationship in Figure (7) was drawn with the assumption that the reference current will not exceed 3A peak. Figure (7) also shows the relationship but for a reference sine wave with a decaying DC offset.

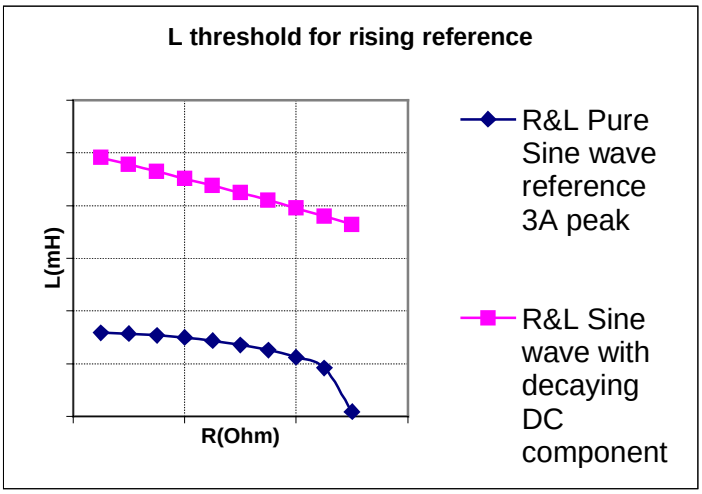

Figure (7): *R and L_{max} Relationship*

Since the first 2 design parameters (R and L) are now more concise, the next design

parameter (f_{max}) could be studied. A base frequency (f_b) will be used to refer to the reciprocal of the step size s. However, The general frequency (f_{mos}) can be greater or less than f_b provided that it shall not exceed the maximum rated frequency of the power MOSFET.

Figure (8) shows the actual hysteresis current waveform. At a certain step the current will oscillate around the reference current within hysteresis band h with a periodic time of T_{mos}. If the shown step is located near the peak of the sine wave then there is a possibility that the actual current would saturate causing f_{mos} to decrease. This suggests that f_{max} is located at the initial steps of the reference current. Also, at a certain step with certain value of L, if h is decreased then f_{mos} would increase.

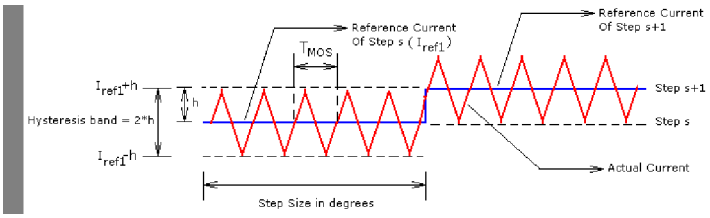

Figure (8): *Switching Frequency*

It is now clear that both L and h affect the value of f. Figure (9) [1] shows the relationship between the 3 variables using the previously mentioned SIMULINK blocks.

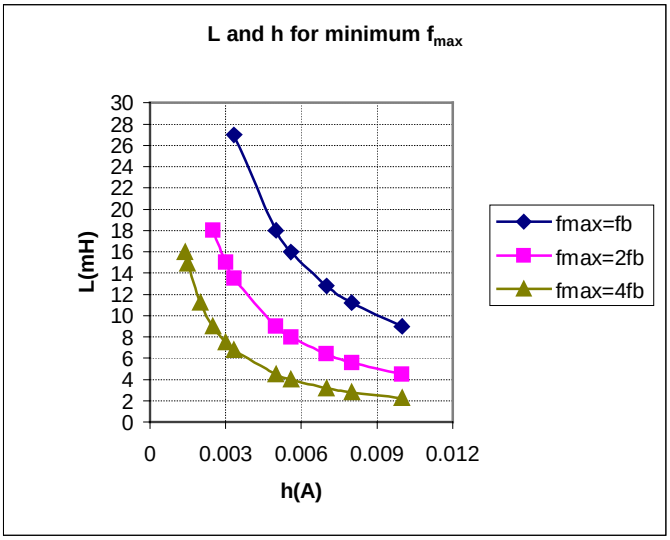

Figure (9): *L and h for minimum f_{max}*

It is then possible to set the minimum f_{max} to a certain value below the MOSFET

frequency rating and this would in turn define one of the shown curves in Figure (9). After that the choice of L and h will have a range of selected values. But it is not possible to do that without studying the effects of L, h, f_{max} on the value of THD or the effects of h, f_{max} on THD as long as Figure (9) has already defined the relationship between L and h.

In Figure (10) [1], the relationship between h, f_{max} and THD is shown in case of 8-bit and 16-bit DAC.

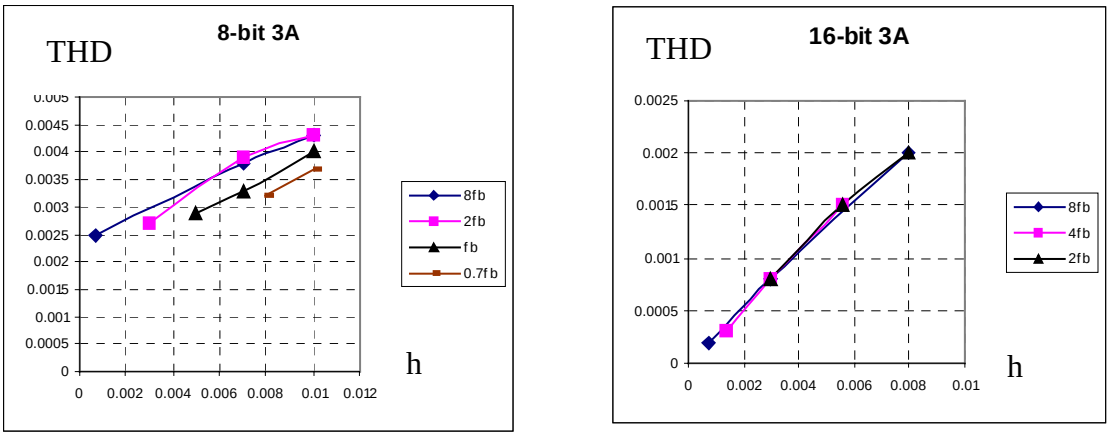

Figure (10): *THD in case of 8 and 16-bit DAC*

Figure (10) clarifies that it is not possible to reach the specified value of THD of 0.1% in case of 8-bit DAC. In case of 16-bit DAC, the THD value of 0.1% can be obtained. There are here several choices of f_{max} and the best choice could be to let f_{max} equal to the most minimum which is equal to $2f_b$ as shown in Figure (10). In this case the value of h will be of 0.003 and from Figure (9), L will be in the range of 7mH. Lastly R can be selected from Figure (7). It should be noted that the value of h here is set as a voltage value, hence h will be recalled as h_v to indicate it as a voltage value or h_i to indicate a current value.

4. Practical Implementation:

From simulation, it is possible to set any value to any variable. But due to some practical limitations of the used lab driving circuit of the MOSFET, it is not possible to set the value of h_v to less than 0.1 Volt as shown in Figure (11) [1].

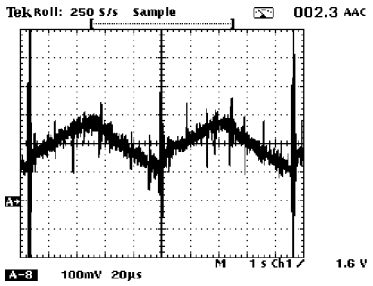

***Figure (11):** Minimum Hysteresis Voltage*

This will result in a value of h_i that is dependent on the value of the measuring resistor R since $h_v=R*h_i$. It is noted from this equation that the value of h_i will decrease as R increases. The following table shows how the value of THD, using the SIMULINK program, will be affected by changing R.

***Table (1):** Effect of R on THD*

L \ R	0.5	1	2	3	4
10.4mH	12%	5.7%	3%	2%	1.5%

In Table (1), the value of THD was calculated at current of 1A. It was observed that at different values of L the value of THD doesn't change and this is of course due to the high value of h_i. From Table (1), the value of THD doesn't change dramatically after R=3 Ohm. Hence, $h_i=0.1/3=0.0333$ A.

5. Verification of THD Due to the Laboratory Assembled Hardware:

Table (2) compares between the value of THD from SIMULINK and from the hardware at values of R equal to 1, 2 and 3 Ohm. The difference between these values could be due to the Electro-magnetic interference (EMI), due to the switching of MOSFET, which affects the reference signal. But it is clear that THD is enhanced as R is increased –in both SIMULNIK and the actual circuit.

***Table (2):** Comparison between THD from SIMULINK and Hardware*

R	1	2	3
THD (SIMULINK)	5.7%	3%	2%
THD (Hardware)	6.3%	4.8%	3.7%

The selected value R will be 3 Ohm (h_i= 0.03333A), as mentioned before. From Fig 4.5, the value of L can change from 0 to 12.5 mH. Any value of L can be selected because

THD will not be affected as h_i is high. A value of 10.4mH will be assigned to L. The values of f_{min} and f_{max} will be 7 kHz and 10 kHz respectively.

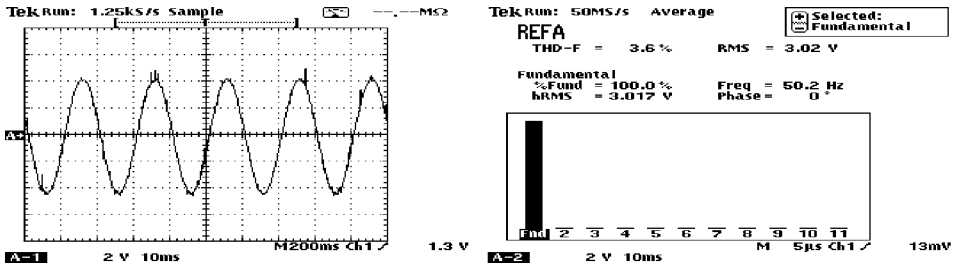

Figure (12): *Current Waveform and the Resultant THD*

Figure (12) shows the output current multiplied by 3 (measuring resistor). The r.m.s. value of this signal is around 3V and so, the r.m.s. value of the injected current in the relay terminals is 1A.

Figure (13) shows the tripping contact and drop out of the relay.

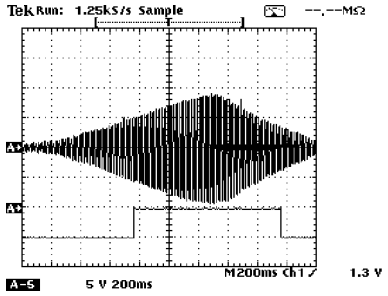

Figure (13): *Relay Trip and Drop Out*

The operation of the relay, due to steady state waveform is acceptable. The value of the injected current can be set through the software from 0 to 4A. The decaying DC component test can be achieved using the same software program; by changing the current equation.

6. DC Offset Test:

As mentioned before, it is possible, using this tester, to inject a certain required waveform of current. For example, Equation (1) [4] represents a current waveform with a decaying DC offset.

$$i(\omega t) = I_{max} * \left[\sin(\omega t + \alpha - \theta) - e^{\frac{-t}{\tau}} * \sin(\alpha - \theta) \right] \quad (1)$$

Where:
α - the fault inception angle on the voltage waveform in degree.
θ - the fault impedance angle in degree.
A - the DC component initial amplitude and is equal to ($-I_{max} \sin(\alpha - \theta)$) in Ampere.
τ - the time constant of the system in seconds.
i_{ss} - the steady state current value and is equal to Imax sin ($\omega t + \alpha - \theta$) in Ampere.

Equation (1), using a PC program, is sampled and sent via PC to the DAC to generate a current waveform with a decaying DC offset. The result is shown in Figure (14).

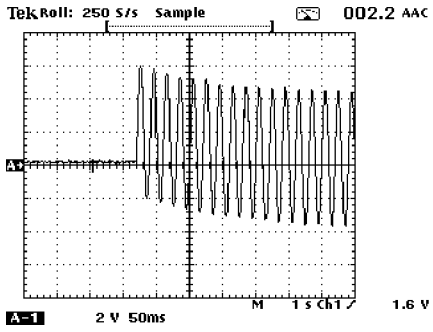

Figure (14): *Current with decaying DC component*

It is easy using the PC to change any of Equation (1) variables in order to get a wave form with a variable DC offset. This makes it possible to test protective relays immunity against decaying DC offsets.

Three types of relays were tested (i.e. electromechanical, static and digital) to check their performance when a decaying DC offset appear in the current waveform.

In these tests the steady state current is kept below the relay setting. This means that the relay shall not trip. If the relay trips then this would be due to the decaying DC offset at the beginning of the injection of the current. It should be noted that relays are normally designed so that the effect of the decaying DC offset is minimum or nearly has no effect at all and by the decaying DC offset test proposed here it is possible to check by how much the relay is resistant to the decaying DC offset.

The following sequence shows this procedure [5]:

A. A certain time constant is selected. Then the DC component is set to its maximum.
B. The steady state current is set to be equal to the relay setting. The relay is supposed to trip here.
C. The steady state current is then decreased until the relay issues no trip.
D. The value of the steady state current at the threshold between trip and no trip is selected to be the current threshold value.

The following waveforms in Figure (15) [1] show the described sequence for 1A setting.

From these waveforms, although the relay settings were at 1A, it tripped at a steady state current of 0.92 A as shown in the waveform 4 of Figure (15).

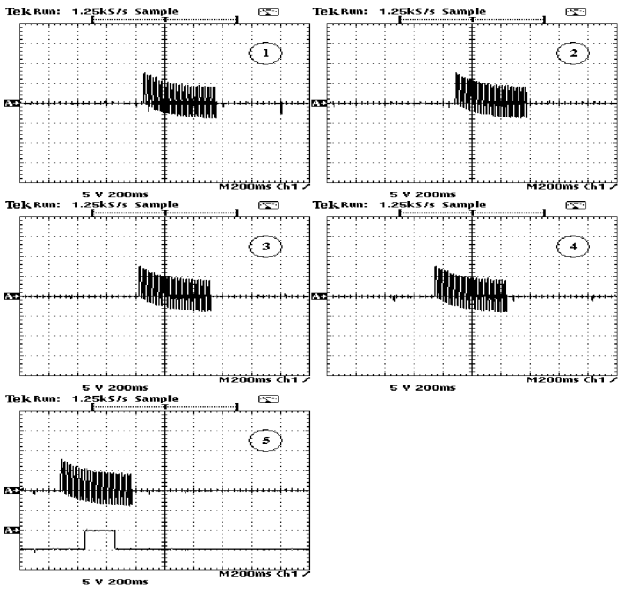

Figure (15): *Test Sequence*

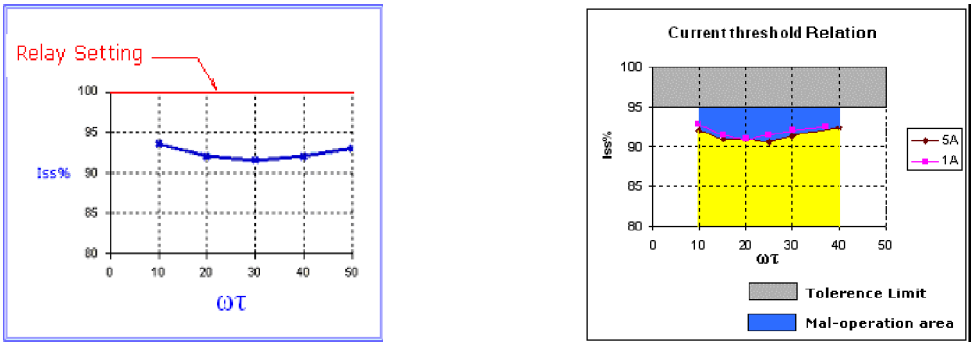

Figure (16): *Deviation using the assembled and the commercial tester*

The previous test was carried out at a setting of 1A & 5A (using the commercially available tester and a static relay) and the threshold at which the relay tripped was found to be 0.92A and 4.5A in case of the 1A & 5A setting respectively. Figure (16) [6] shows these deviations.

It is clear from Figure (16) the result using the assembled tester (to the left) is nearly the same as those obtained by the commercially available testers. It is also shown that as the setting of the relay increases the deviation increases (5A case). This test was done also at setting of 10A and the relay tripped at 8.5A.

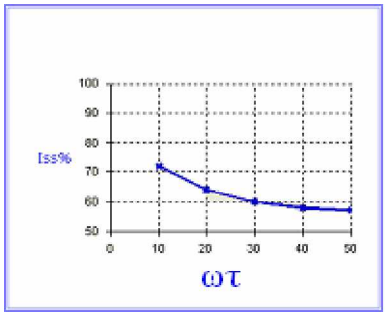

Figure (17): *Results for Electromechanical Relay*

Figure (17) [1] shows the results of the same test but applied to an electromechanical relay and as observed, the relay characteristics was seriously distorted. Digital relays have not been affected by the existence of decaying DC offset. This is due to the existence of special filters that eliminate the decaying DC offset from processing.

7. Conclusions:

This paper presents the design of a simple programmable relay tester. The tester operation is based on a half bridge inverter with hysteresis current control technique. The different design parameters have been introduced. The interrelationship between these parameters were explained. And different design factors have been shown so that accurate current waveform could be obtained.

It has been explained also how practical considerations or limitations could affect the design parameters and lead to some deviation from the basic principle of the design.

The presented design did not – yes – cope with all specifications requirements. However, specifications requirements were not meant to be fulfilled here because the main goal is to implement a proto-type to show that the basic design criteria are working. It is hoped to reach a final product stage in the future.

On the other hand, the tester was used to test different protective relays to check their operation when a decaying DC offset exists in the current waveform. The results show that some types of relays like static or electromechanical are affected and their operating characteristics deviate to give a bad performance. Also, the deviation increases as the current setting increases. Other types like digital relays are not affected due to their strong algorithm which excludes the decaying DC offset before processing.

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Nomenclatures:

R	Current sense resistor in Ohm.
L	Circuit inductance in Henry.
f_{MOS}	Inverter switching frequency (equivalent to 1/ T_{MOS}) in Hertz.
s	Reference wave step size in degrees.
V_{sr},I_{sr}	Power supply ratings (voltage,V_{sr}, and current, I_{sr}).
h	Hysteresis band in Ampere.