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Novel control algorithm of VSC based shunt active power filter

By

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Abstract:

Active power filters (APF) have been developed for over the past thirty years as a possible replacement for passive L-C power filters. Over the course of its development, many configurations have been designed. The shunt active power filter is one type of active power filter. A detailed generic development system for Shunt Active Power Filter is introduced in this paper, and its simulation model is presented in MATLAB / Simulink environment. The model presented considers several issues like: the practical range and accuracy limitations on the obtained real world measurements by the real time controller, a proposed starting procedure for the APF to as a self-tuning technique and an improved zero crossing compensator independent of the sampling frequency. Also, a new space vector based control algorithm is tested on this model and its simulation results are presented.

Keywords:

Shunt active power filter, Zero crossing compensation, self-tuning, Space vector control

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1. Introduction:

Solid-state control of ac power using thyristors and other semiconductor switches is widely employed to feed controlled electric power to electrical loads, such as adjustable speed drives (ASD's), furnaces, computer power supplies, etc. Such controllers are also used in HVDC systems and renewable electrical power generation. As nonlinear loads, these solid-state converters draw harmonic and reactive power components of current from ac mains. In three-phase systems, they could also cause unbalance and draw excessive neutral currents. The injected harmonics, reactive power burden, unbalance, and excessive neutral currents cause low system efficiency and poor power factor. They also cause disturbance to other consumers and interference in nearby communication networks. Conventionally passive *L-C* filters were used to reduce harmonics and capacitors were employed to improve the power factor of the ac loads. However, passive filters have the demerits of fixed compensation, large size, and resonance.

The increased severity of harmonic pollution in power networks has attracted the attention of power electronics and power system engineers to develop dynamic and adjustable solutions to the power quality problems. Such equipment is generally known as active power filter.[7]

Active power filters may be constructed out of single phase or multi-phase converters using either voltage or current source converter topologies. To provide filtering action at frequencies above the fundamental, converters must employ a switching frequency of several kHz or more. Only a very limited set of high power semiconductor devices are capable of operating at these frequencies, with the IGBT being the only device commercially available from a wide range of manufacturers. Intrinsic characteristics of the IGBT make these devices better suited for voltage source converter applications. Voltage source converters themselves are available in various configurations and include: single-phase, 3-wire 3-phase, 4-wire 3-leg 3-phase or 4-wire 4-leg 3 phase. Decision on the specific configuration is based on application, cost, complexity, and modularity of design. Of these four, it is the 3-phase, 3-wire converters that are typically the most cost effective, but with the caveat that they are unable to provide compensation of zero-sequence current components.

Depending on application, either a fixed switching frequency scheme, such as sinusoidal pulse-width modulation and space vector modulation, or a variable switching frequency Hysteresis control scheme may be selected. Hysteresis based control schemes are documented to suffer from inter-phase distortion and the possible existence of undesirable limit cycle behavior. Even if limit cycle behavior is avoided, hysteresis control still generally results in an unpredictable average converter switching frequency that varies with the operating conditions; which will make it much more difficult to filter out the switching frequency harmonics using a small passive filter unlike the fixed switching frequency scheme.[1]

Although fixed frequency control schemes offer many advantages as compared to hysteresis control schemes, they suffer from more severe bandwidth limitations due to increased controller latencies. Thus, for compensation of harmonic producing loads, harmonic prediction must be used to compensate targeted harmonics with a high degree of accuracy[1]. Either through the last cycle history or by compensating the phase of each harmonic computed by FFT for the controller latency.
For compensation of loads with rapid time rate of change, such as welders or various other arcing loads, harmonic prediction is impossible. In these applications the active filter must dynamically compensate the *entire* load current, excepting the fundamental frequency component. Complete elimination of harmonics is not achievable due to digital controller latencies and the limited response time of the converter.
Despite the large body of work on active power filters, there exists a lack of simulation models to study generalized transients reponse and filter/system interactions.
MATLAB / Simulink environment is chosen to simulate the APF due is powerful simulation capabilities covering the areas of the passive electric elements, discrete devices, multi rate discrete time controllers and the fixed point CPU performance. Also the Simulink contains many analysis tools which enable us to judge the performance of the tested control algorithms. Another remarkable feature of Simulink is that it can be used in conjugant with the Real Time Embedded Target Toolbox to automatically generate the required C code of the control algorithm to be compiled and downloaded on a MUC or DSP.[9]

2. General principles of operation of shunt APF:

Fig. 1-(a) shows a generic harmonic load connected to a simplified model of an ac network. Load current harmonics directly translate into source current harmonics. Source current harmonics, in turn, cause a harmonic voltage drop across the source impedance, resulting in harmonic distortion at the point of common coupling (PCC) which will affect this nonlinear load and any other loads connected to the same PCC.
The principle behind shunt active filters is having the filter act as a current source, parallel to the load as shown in Fig 1-(b). It is designed to act as a current source to inject harmonic current into the system at a reversed phasing with the same magnitude of the harmonics being produced. In doing so, the original distortion could be cancelled. In addition, the load reactive power requirement can be supplied from the APF through an additional fundamental frequency component in the APF injected current. Also, the load current unbalance can be corrected by the APF. The core component to a shunt active filter is either a voltage source or current source converter. It's more common to utilize the voltage source converter due to the bulky size and the relatively higher losses of the DC link inductor of the current source converter [5]. The basic configuration of the voltage source converter (VSC) shunt APF is shown in Fig. 2.

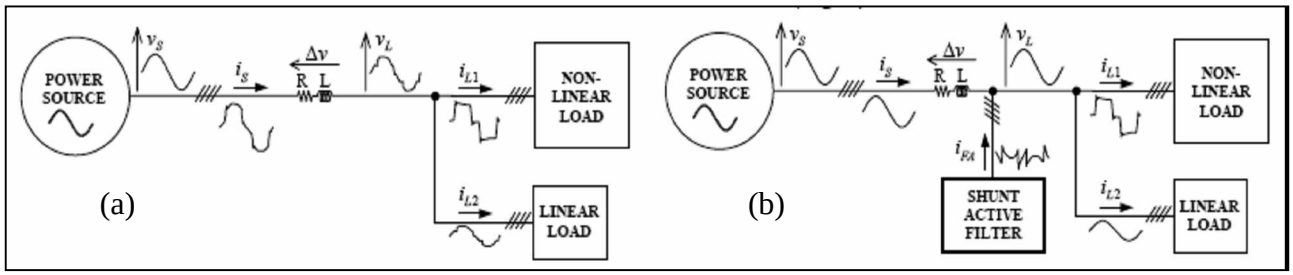

Figure (1): *Generalized configuration of a power system supplying non-linear load (a) in absence of shunt APF, (b)with shunt APF*

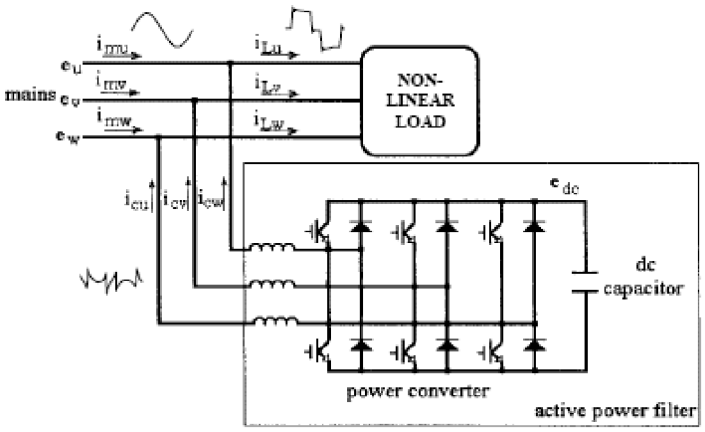

Figure (2): *VSC shunt APF configuration*

3. The proposed development system :

The proposed system can be used in development and testing the new algorithms and converter topologies. As shown in Fig. 3, the power circuit configuration proposed is similar to the regular configuration except that a step down variable auto transformer is added at the supply side to perform the tests of the control algorithms or topologies with minimum possible damage to the used components at gradually increasing operating voltage. And to limit the short circuit current in case of any failure or malfunctioning of the controller. Another benefit of the transformer is to simulate the conditions of a weak network which are a more restricted testing conditions and closer to the practical case. The nonlinear load used is a three phase controlled rectifier with smoothing reactor to provide a deferent level of harmonics distortion and reactive power requirements of the load current by varying the firing angle. Also a three phase passive high pass current filter tuned at frequency near the switching frequency to filter out the switching frequency component of the converter current and reduce the its effect over the supply voltage, considering that the impedance of the step down transformer is relatively high and thus a significant voltage distortion could be produced. Finally, the used converter

is a three phase inverter built by IGBT modules. The AC output terminals are connected to the PCC through an interface inductor and the DC side is mounted to a large capacitor in series with a charging resistance which can be shorted out by a contactor.

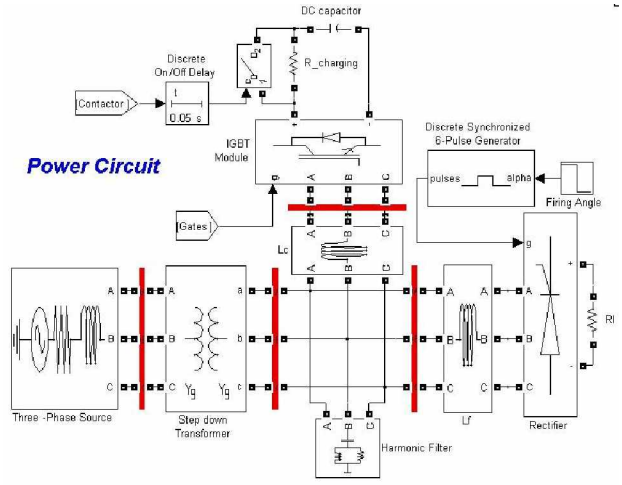

Figure (3): *The power circuit of the proposed system*

Table (1): *The power circuit specifications*

Supply			
Short circuit level	1 MVA	*Rated line Voltage*	380 v
Supply frequency	50 Hz		
Step Down Transformer			
Rated line voltage	380 v	*Rated current*	20 Amp
Series impedance	0.004+J 0.4 PU		
Controlled Rectifier			
DC load	25 Ω	*Smoothing reactor*	1mH
APF Converter			
IGBT R_{on}	10 mΩ	*Diode* R_{on}	10 mΩ
IGBT t_{on}	2 µsec	*IGBT* t_{off}	1.5 µsec
Interface inductor	1680 µH	*DC link Voltage at nominal line voltage*	700 v
DC capacitor	1800 µF		
Charging resistance	15 Ω	*Contactor delay time*	50 msec
Passive High Pass Filter			
Tuning frequency	6000 Hz	*Rated reactive power*	300 Var
Quality factor	3.75		

4. The proposed control algorithm:

The control algorithm used depends on performing all the needed calculation in the synchronously rotating frame (d-q) where all the fundamental components of the current waveform are dc values but any other harmonic components are ac ones. This dc value can be extracted easily in (d-q) frame by a low pass filter. If the (d-q) frame is to be taken in synchronous to V_a by a proper Zero Crossing Detection (ZCD), then ($V_d = V_{paek}$ & $V_q = 0$) and so the d component of load current is referring to the active power supplied and the q component is referring to the reactive power supplied be the source. Thus, the requirements of the control algorithm:

- Eliminate the superimposed ac components on the d component average value of the supply current to mitigate the current harmonics.
- Eliminate the whole q component of the supply current to maintain unity power factor.

The algorithm is based on the Digital Motor Control library (DMC) from Texas Instruments. All calculations were made in the fixed point notation of 32 bit word size. The sampling frequency was chosen at 6300 Hz or 126 samples per cycle of the 50 Hz electric system. These parameters was selected based no the real time controller to be used which is TMS320C2812 digital signal processor DSP and the size of generated code. Also, this particular number of samples, 126 samples per cycle, must be a multiple of six to avoid the non-characteristic harmonics in case of using the space vector modulation [8].

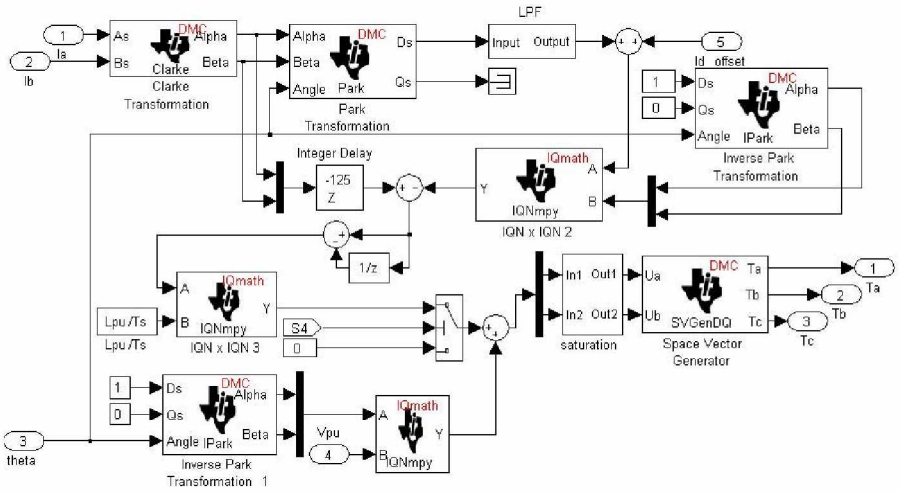

Figure (4): *The controller block diagram*

The following section describes the main part of the control algorithm. The load currents is transformed into the stationary frame (α-β frame) by Clarke Transformation

and then into synchronous rotating frame (d-q frame) by Park Transformation according to the following equations:

Clarke Transformation:

$$\begin{bmatrix} I_\alpha \\ I_\beta \\ I_o \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ 0 & \sqrt{3} & -\sqrt{3} \\ 1 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \quad (1)$$

And with the absence of the zero sequence in the three wires system

$$\begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 1/\sqrt{3} & 2/\sqrt{3} \end{bmatrix} \cdot \begin{bmatrix} I_a \\ I_b \end{bmatrix} \quad (2)$$

Park Transformation:

$$\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} \quad (3)$$

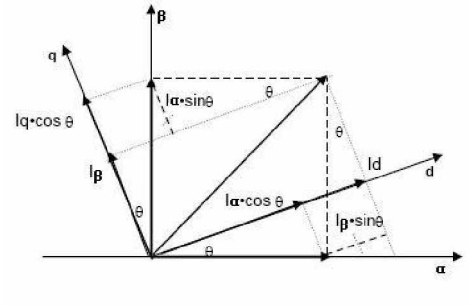

Figure (5): *Illustration of the Park transformation into the rotating frame*

The d component is filtered to extract the fundamental component and added to an offset valve which will be explained later. And by equating the q component to zero the complete image of the supply current is completed to be harmonics free current and in phase with the supply voltage. The reference converter current is obtained from the load current and the reference supply current. Then the converter output voltage in calculated as follows:

$$\begin{bmatrix} Vc_d \\ Vc_q \end{bmatrix} = L \cdot \begin{bmatrix} d/dt & -\omega \\ \omega & d/dt \end{bmatrix} \cdot \begin{bmatrix} Ic_d \\ Ic_q \end{bmatrix} + \begin{bmatrix} Vs_d \\ Vs_q \end{bmatrix} \quad (4)$$

The calculations are performed in the stationary frame ($\omega = 0$) to decouple the above equation components. The above equation is discretized to the following form:

$$\begin{bmatrix} Vc_\alpha \\ Vc_\beta \end{bmatrix} = \frac{L}{Ts} \cdot \left(\begin{bmatrix} Ic_\alpha \\ Ic_\beta \end{bmatrix} - Z \cdot \begin{bmatrix} Ic_\alpha \\ Ic_\beta \end{bmatrix} \right) + \begin{bmatrix} Vs_\alpha \\ Vs_\beta \end{bmatrix} \quad (5)$$

The control algorithm has one step time delay. So, the load current samples need to be time advanced by one step and this can be done by using the sample in the previous cycle successive to the current sample, i.e. we need 125 steps time delay not 126 steps.
These components will be fed to a space vector generator to produce the gating pulses timing. And using a pulse width modulator this timing is translated into necessary driving pulses. The carrier frequency is set at 6300 Hz equal to the sampling frequency to avoid the non-characteristic harmonics. All calculations are performed in PU system normalized at voltage base of $V_{DC}/\sqrt{3}$ and current base of 25 A.
It is required to regulate the DC bus voltage to maintain constant suitable DC bus voltage level sufficient to bush reversed current harmonics and supply the compensation reactive power to achieve unity power factor. The reference value of the DC bus voltage depends on the operating AC voltage level and the sharpness of the converter reference current which is translated to excessive voltage across the interface inductor. The output of the controller is introduced as an offset value to the required supply current d component which represents the active power supplied through the fundamental component to compensate the converter losses.
The DC bus voltage across the capacitor bank is measured and this measurement is filtered. The used filter is digital second order low pass filter tuned at 25 Hz to avoid introducing considerable phase shift which will reduce the phase margin. The used controller is digital PID controller with output saturation and antiwindup correction as shown in Fig. 6.

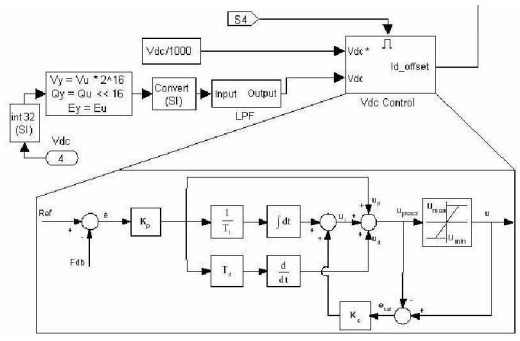

Figure (6):*The DC voltage control block diagram*

5. The proposed self-tuning technique:

To get satisfactory results of harmonics reduction and reactive power compensation, accurate values of PCC voltages, load current and zero crossing synchronization must be obtained accurately. And at this stage we may face number of problems:

- The supply voltage measurements have inhibited offset in case of using unipolar ADC. This offset may not completely be removed due to the accuracy limitations.

- The same argument can be applied on the load current measurements. But this issue is solved through using the synchronous rotating frame (d-q frame) where the fundamental component is transformed to DC value and the DC component, if exists, is transformed to 50 Hz component of negative sequence according to Eq(3). So, the image of the DC component is filtering out among the harmonics components to get the fundamental of the load current. And about the remaining DC component in the load current measurement in (α-β frame), it has no effect since it will differentiated according to Eq(5).
- There is inhabited error in ZCD will vary between zero and one step delay.
- It is not possible to acquire the PCC voltages from the step down transformer secondary due to the huge amount of voltage distortion originated from the relative high series impedance of the transformer which will result in misleading ZCD. The available way is to acquire these measurements from the primary side. And so we are forced to compensate the magnitude error between the supply voltage and the PCC voltage. Also we need to compensate for the phase error between these two voltages.

To solve these issues the following self tuning is proposed; the offset DC component in the supply voltage measurements can be removed be the same concept of filtering the DC component image in the d-q frame using a low pass filter. Then the values of the PCC voltages needed in Eq(5) are reconstructed form the phase peak value of supply voltage at the filter output using inverse Park transformation after scaling by the detected step down transformation ratio which will be explained later. When this technique is compared to the moving average window, it was found that the proposed technique has higher computation overhead but it has faster response than the later one which needed a complete cycle to obtain the DC component.

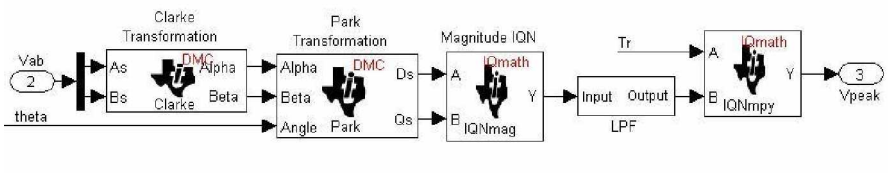

Figure (7): *Obtaining the peak value of PCC voltage after cancelling the DC offset*

To compensate the inhibited (ZCD) error, the value of the q component of supply voltage can be used. This value must be equal to zero if the ZDC is synchronized accurately. Hence, this fact is utilized to compensate theta values by an offset produced from a PI controller is feedback is the supply voltage q component and its reference is zero. The remaining used self-tuning techniques to solve the magnitude and phase errors produced from using the step down transformer are performed in the starting stage of the APF. They will be discussed in the starting procedure section.

6. The proposed staring procedure:

This section describes the proposed starting procedure to avoid problems like the mistuned parameters, inrush charging current and instable starting which may result in permanent damage to the APF components. This procedure is presented as steps sorted by its time sequence:

A) Transformer ratio detection stage:

In the beginning of the operation, the capacitor is charged through the anti-parallel diodes of the IGBT modules to the peak of the line voltage of PCC. To limit the charging current, the charging resistance is introduced in series with the capacitor. The measured DC bus voltage with the calculated peak phase voltage of the PCC can be used to obtain the transformer ratio. This is done by using a PI controller its feed back is the calculated peak value of the PCC phase voltage multiplied by $\sqrt{3}$ and its reference is the DC bus voltage. This stage is completed before enabling the driving pulses.

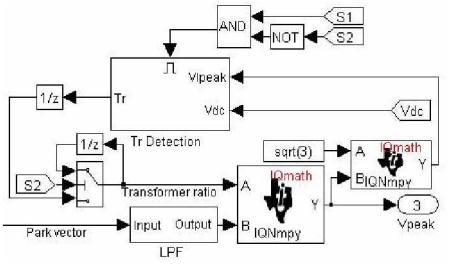

Figure (8): *Transformer ratio detection*

B) Phase error correction stage:

To compensate the transformer phase error, we depend on the fact that when the space vector modulator is fed with a unity vector synchronized with PCC voltage, the converter output voltage will have a fundamental of $V_{DC}/\sqrt{3}$ peak value equal to PCC phase voltage and synchronized with it. This results in no active or reactive power exchange through the interface inductor keeping the DC bus voltage constant at peak of PCC line voltage. Thus, a PI controller is used, its reference is the peak value of the PCC phase voltage multiplied by $\sqrt{3}$ and its feedback is the DC bus voltage. The PI output is additional offset to the theta ramp. During this stage the charging resistance must be shorted out to exclude its power losses. By the end of this stage, the controller is fully tuned and ready to operate the APF.

C) Boosting up the DC bus Voltage:

The dc bus voltage must be increased to a level capable to compensate the load harmonics and the reactive power requirement. This level is set at 700 v at full PCC

voltage. During this stage the charging resistance is returned back to damp the system dynamics, stabilize the system and limit the charging current. By the end of this stage, the starting procedure is completed and the charging resistance is eventually removed.

7. Simulation Results:

The results to be demonstrated over the used self-tuning techniques, the starting procedure, steady state operation and the load switch ON transient response.

a) The self-tuning techniques:
The different versions of theta variable are shown in Fig. 10. There are two offsets are added to the original theta ramp; one to compensate the delay due to the ZCD error and the other is to compensate the delay originated from the transformer.

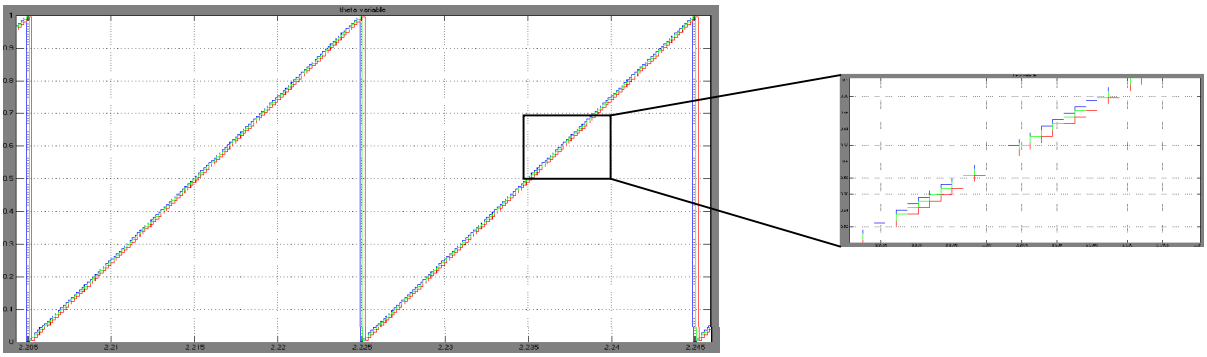

Figure (9): *Theta ramp compensation*

Different transformation ratios are used to test the transformer ratio detection technique. As shown in Fig. 11, the transformation ratio is determined accurately within time range less than one second.

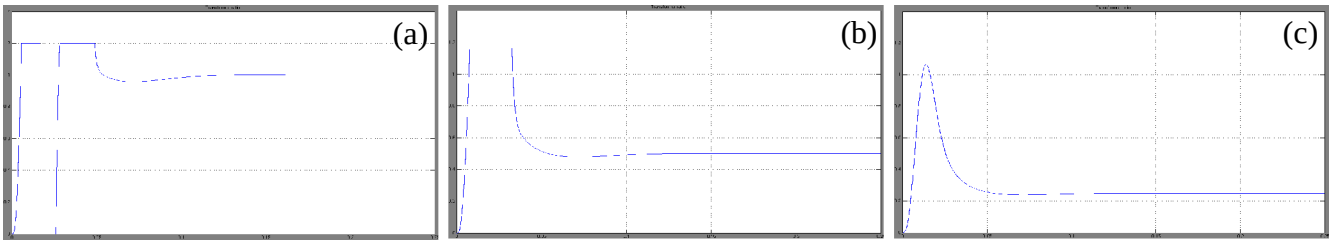

Figure (10): *Transformer ratio detection results with a)1 b)0.5 c)0.25 ratios*

b) The starting procedure:
The stages of the starting procedure are visualized on the DC bus voltage as shown in Fig. 12. also we can see that the charging current is limited within the safe limit

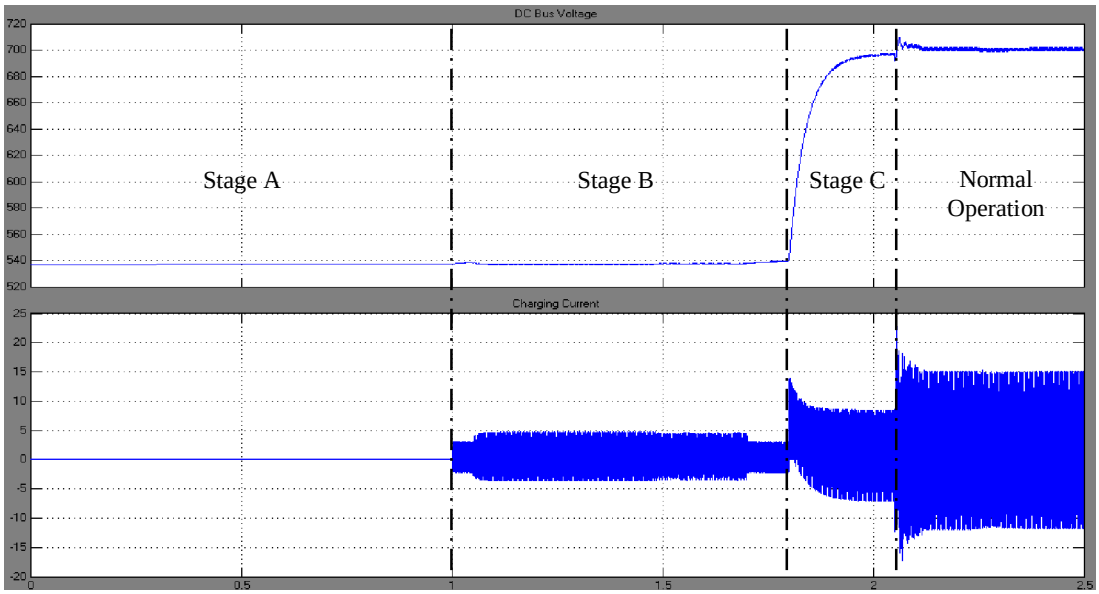

Figure (11): *The DC bus voltage and the charging current during the starting stages*

c) The steady state operation:

The steady state operation of the proposed APF under the following condition: rectifier firing angle of 30˚, transformer ratio of 0.9 and DC bus voltage of 630 v, is presented in Fig. 13. As shown the supply current is free of the low order harmonics and all the existing ripples are around the switching frequency. These ripples are reduced by the passive filter and can be farther reduced by using larger interface inductor. APF is capable to compensate the load reactive power requirement to achieve unity power factor at the supply.

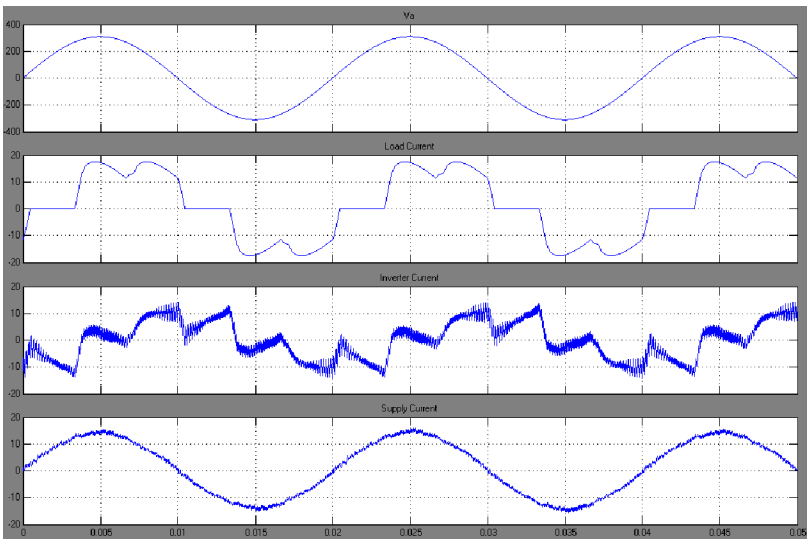

Figure (12): *The waveforms of the load, inverter and supply current in phase a*

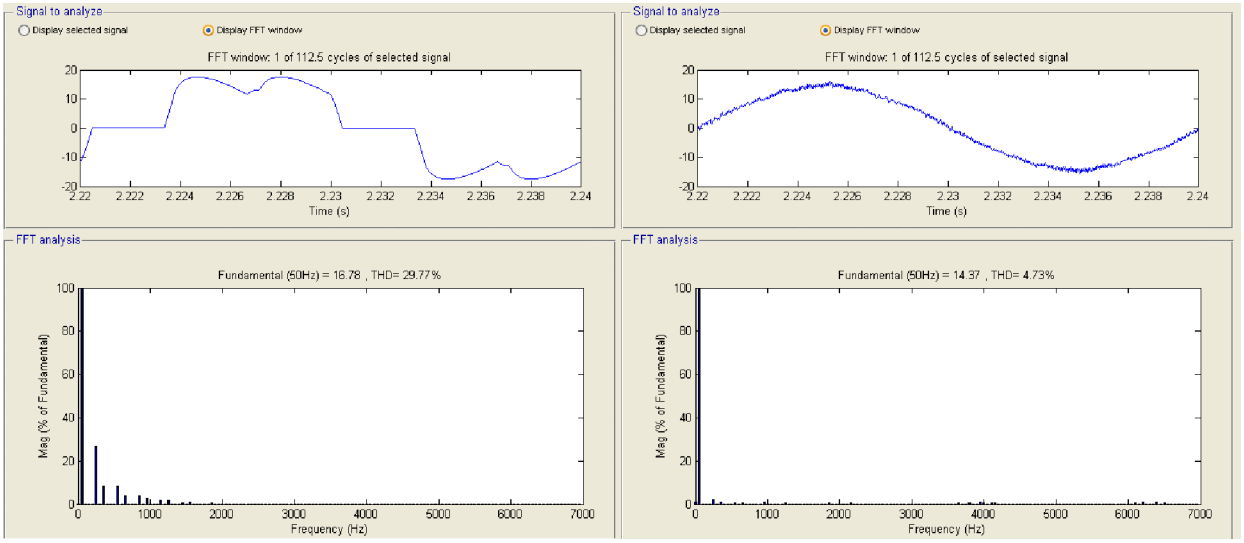

Figure (13): *The harmonic spectrums of the load and the supply currents*

The harmonic spectrums of the load and supply currents are shown in Fig. 14. The THD is reduced from 29.77% at the load side to 4.73% at the supply side. And these harmonics component of the supply current fulfill the current distortion limits provided in IEEE Std 519-1992 [7].

d) Load switch ON transient response:

Fig. 15 shows the transient response of the load switch ON, the controller need one cycle to start to track sinusoidal supply current. Once the DC bus voltage is fully stabilized, the supply current takes its steady state waveform.

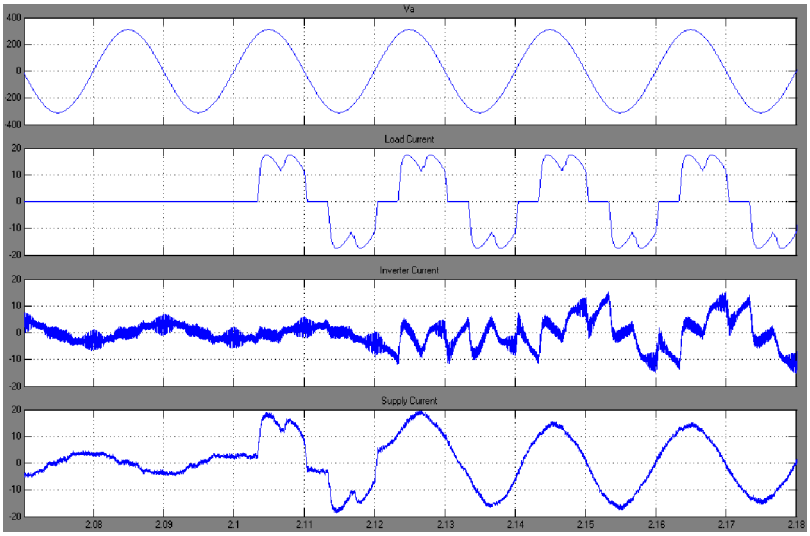

Figure (14): *Load switch On transient*

8. Conclusions:

This paper introduces a development system for the testing purpose of new control algorithm and new topologies of the APF. A Simulink model was built for this system to test a new space vector based control algorithm for VSC shunt APF. Also, self-tuning techniques for this controller were discussed and a starting procedure was proposed to avoid common starting problems. The simulation results were presented to demonstrate the self-tuning techniques performance and the starting procedure stages. These results show the ability of the controller to reach the tuned parameters in deferent operating conditions. The steady state performance results indicate that the propose algorithm was successful in reducing the harmonic distortion to the standard limits. Transient response results show that the system can start its proper operation in about 1 to 2 cycles.

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Nomenclatures:

V_d, V_q..	Direct and quadreture voltage components respectively.
V_a ……	PCC Voltage of phase a.
I_a, I_b, I_c	Three phase load current values.
I_α, I_β …	Alpha and beta load current components in stationary frame respectively.
I_d, I_q …	Direct and quadreture load current components in synchronous rotating frame respectively.
θ , ω	Angular position and velocity of the synchronous rotating frame respectively.
Vc_d, Vc_q	Direct and quadreture converter output voltage components respectively.
Vs_d, Vs_q	Direct and quadreture supply voltage components respectively.
Ic_d, Ic_q	Direct and quadreture converter output current components respectively
L	Interface inductance.
Ts	Sampling time.
V_{DC}	The DC bus voltage.