



ISSN 1110-0451



(ESNSA)

Performance Enhancing of Nano-scale Technologies in Nuclear Applications Using C-MOS and FS-GDI HhybridApproach

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ARTICLE INFO

Article history:

Received: 29th Oct. 2023

Accepted: 21st Mar. 2024

Available online: 1st Apr. 2024

Keywords:

Nano-scale technologies,

45 nm Technology,

65 nm Technology,

C-MOS,

CPL,

FS-GDI.

ABSTRACT

Nano-scale technologies have gained significant attention in various industries, including the nuclear field, due to their unique properties and potential benefits such as miniaturization and improved performance, radiation-hardened electronics, sensors, and detectors. This paper studies the performance of the different Nano-scale technologies in electronic elements fabrication using the different Full Adder (FA) circuits with respect to different realizing methods. Four main parameters; delay time, consumed power, simplicity of hardware (number of transistors), and Power Delay Product (PDP) have been used for evaluating the different FA circuits efficiency in 45nm and 65 nm Nano-technologies and utilizing the Complementary Pass-Transistor Logic (CPL), Complementary Metal-Oxide-Semiconductor (C-MOS), Full-Swing Gate Diffusion Input (FS-GDI) hybrid approaches. The experiments are carried out using a simulator package (Cadence Virtuoso) for 65nm nanotechnology. The results revealed the performance of the FA circuits at the lower Nano-scale performed better than the higher nanoscale. C-MOS approaches provide better improvement in the 45 nm technology compared to the 65 nm technology and the other realizing approaches.

1. INTRODUCTION

The rapid advancements in Nano-scale technologies have opened new avenues for enhancing the performance and capabilities of electronic systems in various industries, including nuclear applications. Nano-scale electronic devices offer unique advantages such as Miniaturization and improved performance whereas Nano-scale fabrication techniques allow for the miniaturization of electronic components, leading to smaller and more efficient devices. In the nuclear field, this can be particularly useful for developing compact and portable radiation detectors, monitoring systems, and control devices for nuclear reactors. Moreover, they can provide increased integration density, and enhanced radiation resistance which makes them highly suitable for deployment in nuclear environments. In high-performance systems, the ability to increase clock speed and circuit density is limited by power constraints. This is due to the challenges involved in delivering power to the circuits

and dissipating the generated heat. The power consumption is a critical factor in portable battery-operated devices like sensor networks, cell phones, and bio-medical devices, as it directly affects the life of the battery. To address the growing demand for low-power VLSI (Very Large Scale Integration), various levels of design, including circuit architectural, and process technology levels, are focused on achieving power efficiency. At the circuit design level, significant power savings can be achieved by selecting an appropriate logic style for implementing combinational circuits. The selection of a particular logic style has a significant impact on important factors that affect power dissipation. These factors include switching capacitance, transition activity, and short circuit currents. The relative importance of these performance aspects varies depending on the specific application, the type of circuit being implemented, and the design technique employed [1-3].

The computational complexity of the circuits and the wireless communications systems is related to the area, number of components in the circuit, and power that is consumed. The consumed power is considered the main constraint in most design applications, where the design with low power will increase the life of the designed system and enhance the power efficiency of the systems. Radiation-hardened design with FA cell on 45-nm technology is studied on [4]. For critical safety or radiation-exposed applications; Vidhyadharan et al., in [5] used Carbon Nanotube Field-Effect Transistor (CNTFET) based low power design that consume a power equal to 66 nW and this achieve 84-98% power consumption reduction compared to CNTFET. In [6], the authors introduced an analytical method for estimating jitter in CMOS inverters considering the presence of Ground Bounce Noise. An effective analysis and modelling technique that allows designers to evaluate the timing characteristics of hybrid full adder circuits at the block level is discussed in [7]. In [8], Ceschia et al. discuss the development of a comprehensive and integrated sizing approach for fuel cell/battery hybrid power systems. This approach takes into account various performance indexes to optimize the sizing of these hybrid systems. In [9], a different topic is explored. The authors delve into a study that goes beyond the concept of smart devices and focuses on the definition and performance assessment of a secure architecture for the Internet of Nano-Things (IoNT). The IoNT refers to the interconnection of Nano-scale devices and objects to enable various applications and functionalities.

In this presented research paper, the power/area efficient VLSI implementation approaches have been presented for achieving power efficient nuclear devices and help to manufacturing small size digital devices for nuclear applications. Different two Nano-size node technologies have been compared using cadence S/W package simulator. The low-power wireless networks have been merged in the various applications such as the nuclear radiation monitoring. Power/area efficient digital and logic circuits implementing will directly improve the performance of low power wireless networks in the nuclear applications.

For providing power/area efficient digital and logic circuits, it is should be choosing the suitable VLSI logic style. The FS-GDI is known a power efficient and lower transistor count approach. On the other hand, the hybridization concept is presented as a method for implementing the efficient circuits, which have the required/determined characteristics. The implementation technique based on the hybridization means utilizing more than on logic styles to implement a digital or logic circuits

for optimizing the performance of the implemented circuits. In our presented paper, the hybrid technique is presented to merge the traditional VLSI logic style with the area efficient GDI approach. The presented research work in our paper aims to study the performance of implemented circuits using the traditional, new and hybrid-based logic styles techniques. Also, the effects of the Nano-size node technology on the performance of the implemented circuits such as consumed power, delay/processed time and transistor count, "The same design has been repeated/implemented using the same logic styles under two various Nano-size node technologies". Hence, the transistor count metric is the same and does not change where the design is not changed. While, the other performance metrics such as the delay time, the consumed power and PDP are changed as cleared in the simulation experiments results.

1.1 Research Motivation

This section presents the motivation of this research work. The main purpose of our research is implementing the power efficient and area FA circuits for enhancing the performance of ALU units and multipliers to be more power efficient, effective area/lower transistor count and high speed. Also, design FA schemes with lower power complexity, it leads directly to decreasing the complexity of the whole digital systems. Optimizing performance of logic and digital circuits can be achieved by choosing the suitable logic style. In our research paper, power and area efficient FS-GDI and hybrid logic styles are utilized for presenting various efficient FA circuits implementing approach. The computer simulation experiments give promising results for extending this FA implementation approach for including the complete ALU circuits and the whole logic circuits and digital circuits of data processing, image processing or security techniques [40]. Also, the time complexity due to the FA process time causes latency increasing, it is problem in real-time applications. The presented approaches decreases the time complexity through decreasing the process time, as cleared in the experimental simulation results. Finally, the size of the node technology is considered also in the presented work.

The performance of the Nano-scale technologies electronic elements is studied with respect to the available 45 nm and 65 nm technologies. There are various digital circuits realizing are utilized for implementing the FA circuits in the different Nano-scale technologies. [3]. the rest of this paper is presented as follows: Section 2 presents the low-power VLSI approaches and their sub-approaches. Section 3 introduced the GDI approach development. Section 4 presents the simulation results. In section 5, the conclusion is introduced.

2. Low Power VLSI Approaches

This section provides an overview of the various styles of VLSI (Very Large Scale Integration). Subsequently, we delve into the various approaches, along with their respective advantages and disadvantages. Figure 1 illustrates the implementation of an AND logic, while Figure 2 shows an XOR logic gate realized through different approaches.

The most widely adopted approach in VLSI design is Complementary Symmetry Metal-Oxide-Semiconductor (CMOS). CMOS offers numerous advantages, including low noise margin, low power consumption, high speed, ease of development, and its prevalence in most chip designs. Nevertheless, CMOS technology encounters several challenges, including high power dissipation, a large transistor density per unit area, long delay times, and high power consumption. An alternative approach commonly employed is Pass Transistor Logic (PTL). PTL is also popular and offers certain advantages such as reduced silicon area, improved speed, and reduced power consumption. However, it should be noted that PTL tends

to be slower at reduced power levels and exhibits notable power dissipation [10].

The Transmission Gate (TG) is considered a third approach where its distinctive feature is the utilization of fewer transistors to implement complex gates. By combining PMOS and NMOS transistors, TG helps mitigate issues related to noise margin, power dissipation, and switching. The Complementary Pass-Transistor Logic (CPL), is the fourth one; specifically the N-MOSFET. CPL (Complementary Pass-Transistor Logic) has several benefits, such as high speed, low input capacitance, and the capability to implement complex logic using NMOS (Networks of Modular Design) networks. However, it also has certain drawbacks, including a decrease in threshold voltage, static power consumption, and increased delay when using longer pass-transistor chains. On the other hand, Double Pass-Transistor Logic (DPL) is a modified version of CPL. DPL offers advantages such as well-balanced input capacitance, no voltage drop, no requirement for buffers, full swing operation, and low power consumption. However, DPL does face challenges such as larger area requirements and the need for inverters [11].

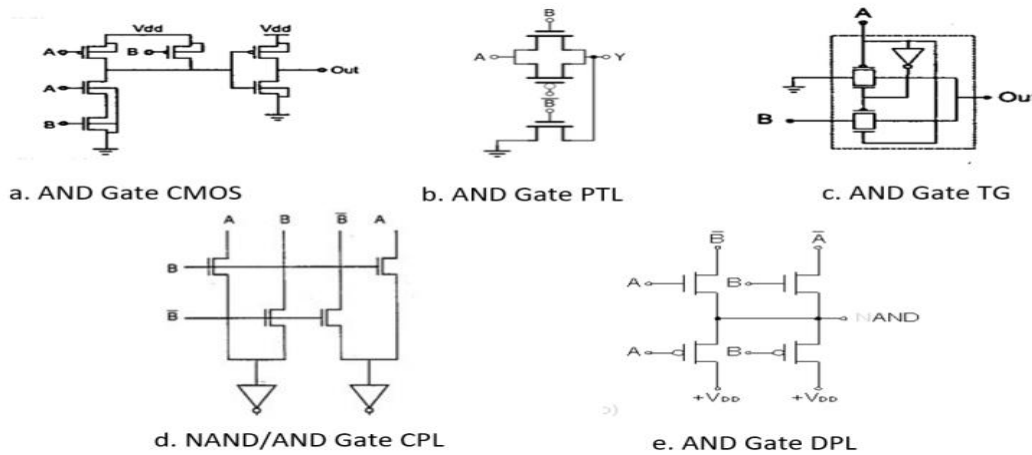


Fig. (1): logic AND gate realization.

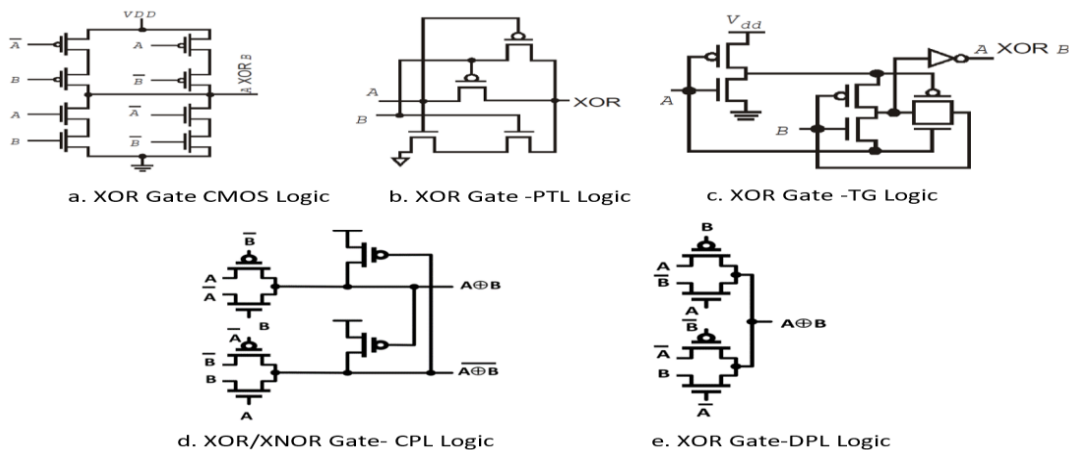


Fig. (2): logic XOR Gate realization

3. GDI approach Development

The GDI (Gate Diffusion Input) approach was introduced by Morgenshtein et al. as a means of implementing low-power VLSI designs. Over a span of fourteen years, Morgenshtein presented various iterations of the GDI technique, including the original GDI cell in 2002, the modified GDI in 2010, and the Full Swing GDI in 2014. The GDI approach offers a compact silicon chip area and aims to improve power consumption, area utilization, and logic gates propagation time when compared to Conventional methods [12-14].

The GDI approach was first invented in 2001, allowing the implementation of complex gates using only two transistors. This technique is particularly well-suited for designing fast and low-power circuits while more efficient in terms of fewer transistor usage than CMOS and PT, as demonstrated in Table 1 [10]. The table shows how to simplify different logic gate hardware by reducing the number of transistors, which improves power efficiency.

Table (1): Transistors count for GDI and CMOS

Realized Function	CMOS	GDI
$F1=\bar{A}B$	6	2
$F2=\bar{A}+B$	6	2

Figure 3 illustrates the GDI approach evolution from 2001: 2014. Figure 3a showcases original GDI cell, while Figure 3b depicts the modified one. The GDI approach final version of is presented in Figure 3c. Using the GDI technique, VLSI digital circuits achieved significant improvements in power consumption, propagation delay, and chip area compared to CMOS and PTL techniques, as shown in Figures 3d and 3e, which depict NOR and XOR gates implemented using the FS-GDI approach.

Both PTL and GDI techniques encountered challenges related to reducing voltage swing at their

outputs due to threshold drops. In 2014, Morgenshtein addressed the issues faced by the original GDI cell by introducing the Full Swing GDI (FS-GDI) approach. This approach incorporates a single-swing Restoration Transistor (SR) as a different solution, ensuring full-swing operation [14].

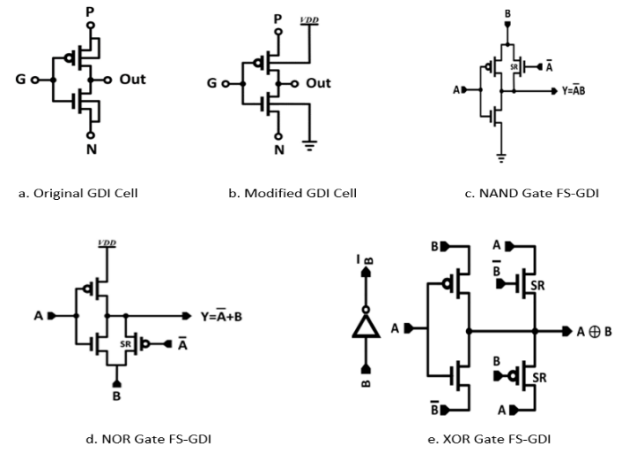


Fig. (3): Cell of GDI approach developing.

4. RESULTS AND DISCUSSION

The numbers, which indicate the smallest feature size of the transistor (PMOS or NMOS), constitute the primary distinction between technologies: 180 nm, 90 nm, etc. The minimal feature size refers to how closely transistors can be arranged on a chip during the fabrication process so that they can be used for a variety of applications. The smaller the chip, the more transistors that can be fabricated on it, producing smaller transistors that are both faster and more power-efficient but the disadvantage in lower technology is high leakage power consumption because of increased sub-threshold leakage. The second drawback is decreasing the noise margin. As shown in Fig. 4, Moore's law is followed by the technology node process.

This study investigated the effects of technology on the power consumption, latency, and PDP of circuits, in order to identify opportunities for improving circuit performance using 65nm and 45nm processes [15].

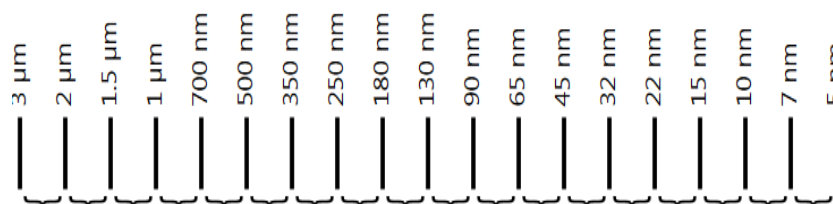


Fig. (4): Technology node CMOS process.

4.1 Parameters: Simulation Setting

In this sub-section, the simulation setting and the various values of the important variables/parameters of the simulation have been discussed. Several computer simulation experiments have been executed to evaluate performance the proposed Hamming encoding circuits. These designs are executed using a TSMC 65nm CMOS technology in Cadence Virtuoso. The simulation setting and various parameters have been given in Table 1.

In the following, the various designs of FA using 45 nm presented and 65 nm technologies have been evaluated by simulator cadence virtuoso software package. Example of the designed circuits using the cadence virtuoso S/W package is given in Figure 5. The presented experiments are limited due to the limitation of the used S/W package of the used simulator, where the available node technology is 65nm and 90 nm node technologies.

Table (1): Parameters of simulation setting

Parameter	Simulation Value
Simulation Package	Cadence Virtuoso Software Package
CMOS Technology Process	65 nm Technology node
Clock Frequency	125 MHz
Supply Voltage (Testing)	0.6 V & 0.9 V & 1.2 V (for normal operating voltage)
PMOS transistor size	Wp/L=240/60,
PMOS transistor size	Wn/L=120/60
Noise Margin (NM _H , NM _L)	0.5 - 0.2 Volts
Metrics	Delay, Power, PDP, No. Ts

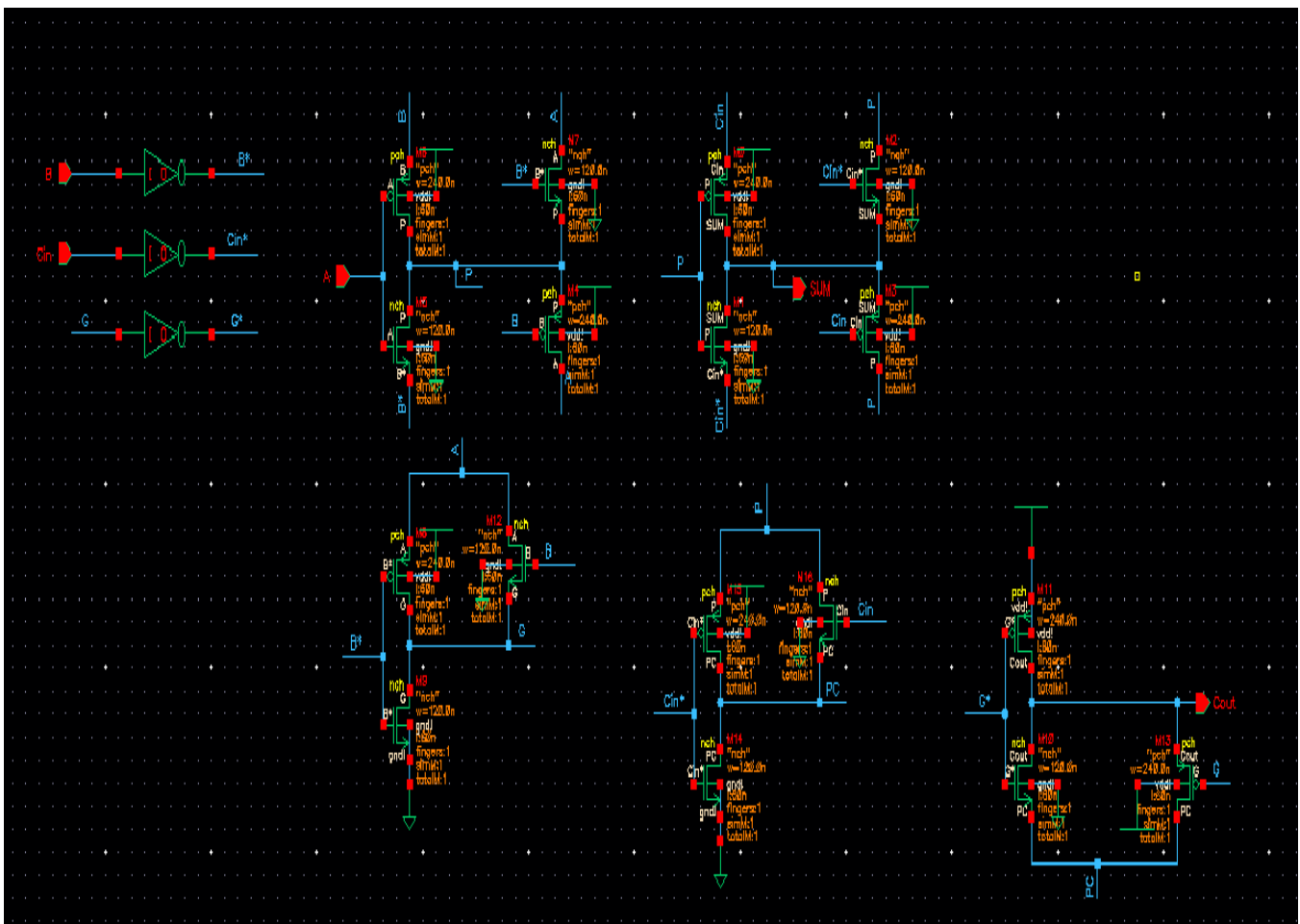


Fig. (5): Design and implementation process of the circuits using the S/W package simulator.

Figure 6 shows the design of a CPL-based FA that was evaluated using a 45 nm CMOS process, it gives results of 2.68 μ W, 38.8 pS, and PDP 103.9 aJ, and 7.5 μ W, 63.8 pS, and 478.5 aJ when tested using a 65 nm process [14].

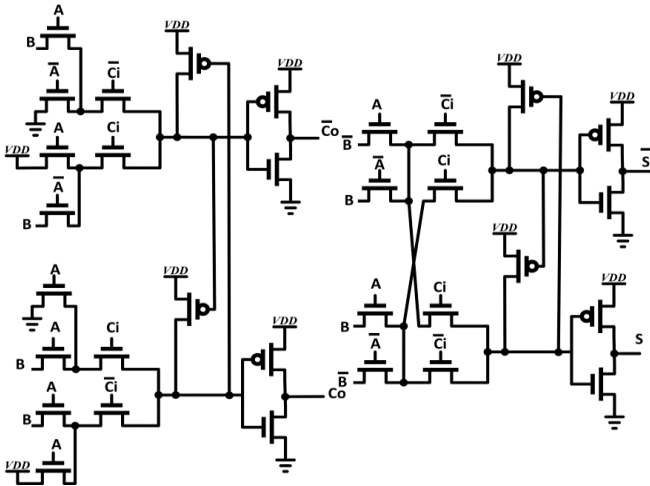


Fig. (6): FA with CPL design

Figure 7 shows the design of a Full Adder (FA) based on C-CMOS, which was evaluated using a 45 nm CMOS process. The testing revealed power consumption of 0.975 μ W, a delay of 46 pS, and a Power-Delay Product (PDP) of 45 aJ. Additionally, when tested with a 65 nm process, the FA consumed 7 μ W of power, exhibited a delay of 65.75 pS, and had a PDP of 460.25 aJ [15].

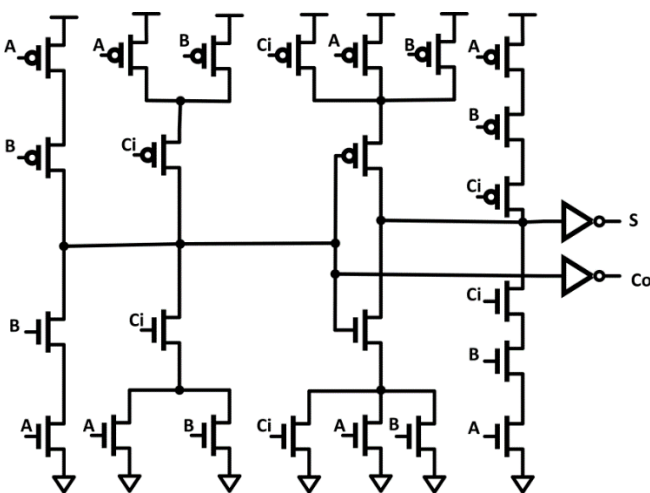


Fig. (7): FA with C-CMOS design

According to [16], Figure 8 displays the design of a hybrid-based Full Adder (FA) that underwent testing using a 45 nm CMOS process. The test results showed a power consumption of 1.613 μ W, a delay of 35.0 pS, and a Power-Delay Product (PDP) of 56.8 aJ. Similarly,

when tested with a 65 nm process, the FA consumed 6.4 μ W of power, exhibited a delay of 43.0 pS, and had a PDP of 275 aJ.

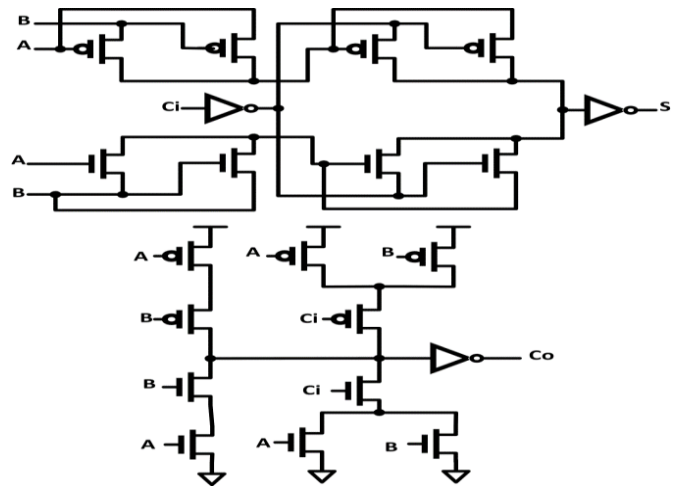


Fig. (8): FA circuit using Hybrid technique

Figure 9 presented FS-GDI design of FA which tested with 45 nm CMOS process, the result gives a 0.97 μ W, 37.8 pS and 35.1 aJ for the consumed power, the delay and PDP, respectively. This FS-GDI based FA has been tested using 65nm node technology. According to the experiments results, its consumed power was 6.3 μ W, 45 pS delay and PDP was 283 aJ. As proved in the results, the lower Nano-size node improves the speed and power consumption but the transistor count still the same.

Table 2 presents the simulation results of various FA circuits with respect to the various techniques used for implementing the circuits and different performance metrics. This table tabulates several design techniques at the 65 nm nanotechnology process compared to 45 nm nanotechnology.

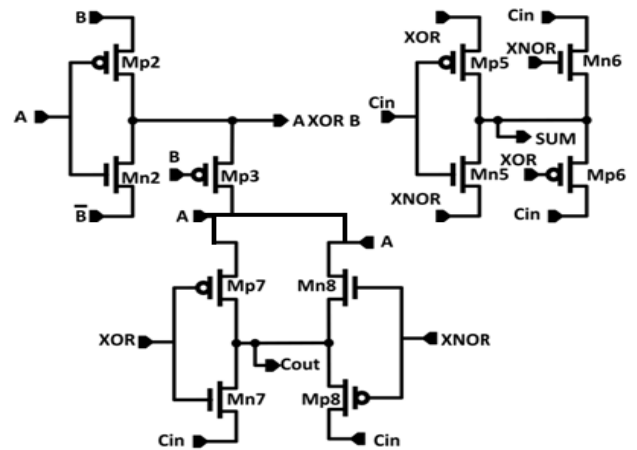


Fig. (9): GDI-Based FA schematic

Table (2): Simulation results of FA circuits with 65 nm and 45 nm CMOS nanotechnology.

Utilized Technique	Various Nano-size node Technologies							
	65nm Node Technology				45nm Node Technology			
	P(uW)	D (pS)	PDP (e-18J)	No. of Ts	P(uW)	D (pS)	PDP (e-18J)	No. of Ts
DPL	7.5	63.8	478.5	38	2.68	38.8	103.9	38
C-CMOS	7	65.75	460.25	28	0.975	46	45	28
FS-GDI	6.3	45	283	18	0.97	37.8	35.1	18
Hybrid	6.1	43	262	18	1.1	35	38.5	18

The different FA circuits have been implemented using the various Nano-scale technology processes, the 65 nm and 45 nm technologies, the results which are tabulated in Table 2. As cleared from these results, the performance metrics values are improved with the lower Nano-scale technology. The C-MOS approach in the 45 nm process presents improvement in the power with respect to the different realizing approaches.

Due to the limitations of the S/W package of the cadence virtuoso simulator, the previous designed circuits using 45nm node are re-implemented and tested using available 65 nm node technology. The power efficient digital and logic circuits can be achieved by choosing the suitable technique. The low power digital circuits is useful for various types of wireless networks such as the Wireless Sensor Networks (WSN) and Wireless Body Area Networks (WBANs), this networks suffer from constraints and limitations of power resources [17-19].

The power efficient circuits will directly improve the power efficiency of the digital processing circuits and encoding circuits. Hence, the life time of WSN nodes will be more long [21]. In [22], the renewable energy techniques are considered for the low-power wireless networks applications. Authors in [22] presented the main research points to enhance the power efficiency of the digital and logic circuits and the low-power wireless networks. The power efficient digital circuits is useful for various nuclear applications due to decreasing the consumed power. Also, the area efficient VLSI approaches can be used to design and implement small size nuclear devices.

Our research work in this paper aims to improve the time and power complexity of full adder circuits through using power efficient logic style techniques such as GDI and the hybrid technique [23]. Improving the time complexity of FA circuits will directly improve the performance of all its applications, such as multipliers

circuits, ALU units, encoding/decoding processes and DSP circuits.

5. CONCLUSIONS

The adoption of Nano-scale technologies in electronic element fabrication offers numerous advantages in the nuclear field. These include superior material properties, radiation resistance, and multifunctionality. By harnessing these advantages, electronic components can be tailored to meet the specific requirements and challenges of nuclear applications, thereby enhancing safety, reliability, and operational effectiveness. This work studies the performance of various FA circuit designs using the different implementing Nano-scale technologies. The same design of FA circuits is realized by the 65 nm technology and 45 nm technology. As shown in the simulation experiments, the lower technology scale performs better than the bigger one. Also, the C-MOS realizing approach presents better performance in the lower Nano-scale technology compared to the other realizing approaches.

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