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Tunnel field effect transistor (TFET): A review

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Abstract

Tunnel field effect transistors (TFETs) offer a solution to the concerns that accompany conventional Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) due to their continuous downscaling. Short channel effects, limitation of minimum (60 mV/decade) subthreshold swing (SS) at room temperature and high OFF current hindered the improvement of the performance of MOSFET devices. TFETs based on band-to-band tunneling (BTBT) mechanism, break the physical limits of 60 mV/dec subthreshold swing and operate with low power consumption. Consequently, TFET with low leakage current, is considered as a great choice for ultra-low power circuits. This review paper provides a general overview of the TFET device demonstrating its physics, working principle, and performance parameters. Additionally, various methodologies of analytical modeling and numerical simulation of TFETs are discussed. Finally, various applications based on TFET and recent possible TFET structures are described.

Keywords: BTBT, MOSFET, TFET, ON Current (I_{ON}), Subthreshold Swing (SS)

1. Introduction

Technological developments in recent decades are based on the miniaturization of MOSFETs. Advances in manufacturing processes, geometries, and the use of different materials improve switching speeds and electronic functionality [1]. However, the shrinking dimensions of MOSFETs have resulted in increasing power consumption [1] and short-channel effects [2]. CMOS technology encounters a physical limitation of thermally injected charge carriers through barriers according to Boltzmann carrier distribution. At room temperature, this results in the limitation of SS to 60 mV/decade as a minimum value [1, 3]. The TFET is an evolution of the "Esaki diode" (also known as the "tunnel diode"), which operates on the quantum tunneling principle and achieves high-speed operation [4]. The operation principle of the TFETs is based on band-to-band tunneling where carriers tunnel from the source side valance band to the channel side conduction band. With TFET, it is possible to achieve low power consumption, SS below 60 mV per decade, low leakage current, high ON- current (I_{ON}) to OFF- current (I_{OFF}) ratio, and considerable immunity against short channel effects [4, 5]. Furthermore, the manufacturing process for TFETs is somewhat similar to that of traditional MOSFETs [7]. Nevertheless, TFETs have limitations such as low I_{ON} and ambipolarity characteristics [8].

The Surface Tunnel Transistor (STT) consists of a p^+-i-n^+ diode structure with an isolated gate over the intrinsic region which controls the tunneling mechanism was introduced by Baba in 1992 [9]. Then, the tunnel FET was developed with a buried oxide thin layer grown on a silicon substrate. Fig. 1 shows the structure of an *n*-channel TFET with the source, the channel, and the drain regions. Subsequently, different TFET structures and material modifications have been proposed to boost I_{ON} current, reduce I_{OF} current, reduce ambipolar behavior, and improve subthreshold swing such as Double gate TFET (DG-TFET) [10], feedback TFET [11], Circular TFET

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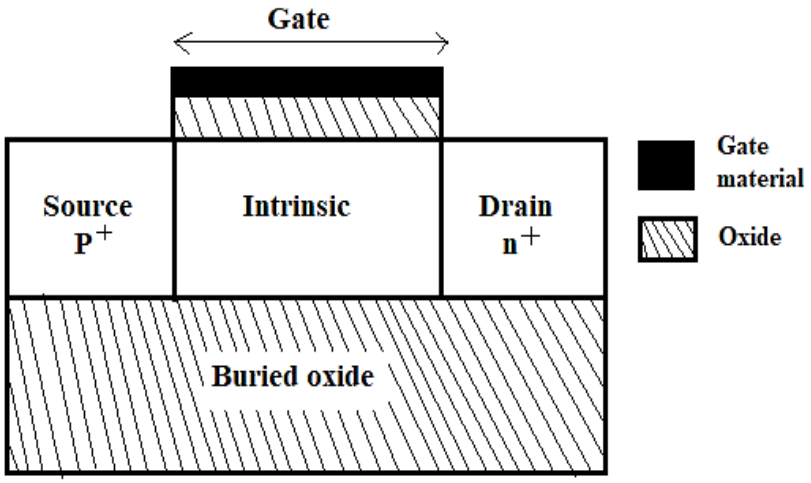

Fig. 1 The structure of P-I-N TFET [6].

[12], Gate-all-around TFET [13], Raised Buried Oxide Tunnel FET [11], Junction less TFET [14], Dual Material Gate TFET [15], Hetero Junction TFET [6, 11, 16], p-n-i-n TFET [17], Hetero dielectric gate TFET [18]. Moreover, different materials with lower bandgap, such as Ge TFET [16, 18], InAs TFET [20], III-V semiconductor material [21], Carbon Nanotubes (CNTs) TFET [21, 22], Graphene Nanoribbon (GNR) Based TFET [24] are also being investigated instead of Si material for better TFET performance.

Analytical modeling of tunnel FET gives an insight into the physics of the device. It is worth mentioning that a proposed analytical model for one TFET design is often not effective for another TFET. Therefore, different TFET architectures can have different models. Modeling the drain current of the TFET primarily involves solving the Poisson equation with appropriate boundary conditions in suitable regions of TFET. Then, the surface potential, the electric field, the tunneling generation rate, and the drain current are derived. The analytical models may neglect the presence of mobile carriers and the depletion regions at the source and the drain or take them into account, depending on the ease or difficulty of the model.

On the other hand, numerical simulations play a significant role in investigating exploratory devices like TFETs. As technology has advanced, tools have become available to design and simulate circuits, and these computer-aided design tools have greatly reduced the cost of preparing circuits. Various TCAD simulators provide BTBT tunnel models in TFET simulation, such as Silvaco, Sentaurs, and Medici. The two techniques of TFET simulation are the semi-classical simulation and the full quantum simulation [25]. In semi-classical simulation, it is performed according to the drift-diffusion theory and includes BTBT as an additional generation/recombination mechanism [25]. The BTBT tunneling mechanism is either a local BTBT model or a non-local BTBT model. For simulations of TFETs, non-local models perform better than local models as they accurately model the physics of the device [3]. For TFETs such as GNR TFETs, CNT TFETs, or thin nanowire TFETs, full quantum simulations become crucial where the quantum confinement effects are necessary to be included to obtain accurate results. The non-equilibrium Green's functions (NEGF) approach is one of the most common methods for performing quantum transport calculations through nano-scale devices.

TFETs with various materials and architectural designs are being investigated in different applications. Logic functions such as OR, NOR, AND, NAND, XOR, and XNOR can be implemented by TFET with different architectures. Furthermore, inverters, multiplexers, memories, amplifiers, and biosensors are designed using TFET.

Development of TFET configurations is required to improve the device performance than the conventional or planner TFET. Various novel TFET structures such as Gate Around TFETs, Fin TFETs, Nano sheet TFETs, L-shaped TFETs, U-shaped TFETs, Dual Source FETs (DS TFETs), and T-shaped TFETs have been proposed.

The present review paper is organized into seven sections. Section 1 includes the introduction. Section 2 describes the physics and working principle of the TFET. Section 3 covers the different analytical models

of various TFET structures. TFET numerical simulations including semi-classical simulation and full quantum simulation are presented in section 4. Section 5 describes the TFET-based applications while recent TFET configurations are presented in section 6. Finally, we conclude in section 7.

2. Physics of TFET

Fig. 2 compares the thermal carrier injection mechanism and the tunneling injection mechanism. In the thermal carrier injection mechanism, only carriers that have energy higher than the barrier height are injected into the channel as in the MOSFET [26].

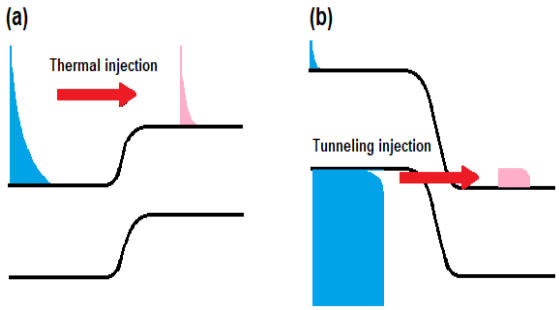

Fig. 2 Comparison between the two carrier injection mechanisms: a) the thermal carrier injection and b) the tunneling carrier injection [26].

However, the operation of the TFET depends on the BTBT mechanism, allowing the carriers to cross the potential barrier without jumping over it. Carriers can tunnel from one side to another side if the barrier is thin enough and there are available empty sites on the opposite side [27]. The bandgap energy of the p+ region excludes most of the femi-Dirac tail distribution of the electrons, and the electrons in the conduction band can be almost ignored. Therefore, only the tunneling of the electrons in the valence band (VB) to the empty sites in the conduction band (CB) leads to the injection of majority carriers into the n^+ region [26].

The energy band diagram of the OFF-state and ON-state of an *n*-type TFET is obtained in Fig. 3. The TFET is considered in the OFF state when the drain voltage $V_{DS} > 0$ and the gate voltage $0 < V_{GS} < V_{OFF}$ where V_{OFF} is the gate voltage value at which the drain current begins to take off. When the CB of the channel region is above the VB of the source region, no tunneling occurs. The negligible OFF-state current exists as a result of the thermionic emission of the carriers across the drain-source barrier and the collection of the minority carriers from the source to the drain [25].

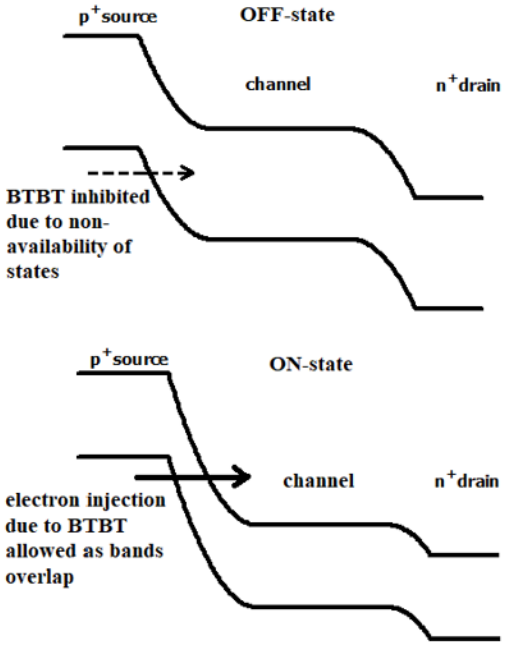

Fig. 3 The energy band diagram of the OFF-state and ON-state of an *n*-type TFET.

TFET is in the subthreshold region when $V_{OFF} < V_{GS}$ < threshold voltage (V_{TH}) of the device. At increasing V_{GS} beyond V_{OFF}, the source and channel bands get aligned results in enabling BTBT of electrons in the source VB to the channel CB and swept to the drain by applying a positive bias to the drain. The subthreshold swing of TFET depends on the gate voltage and it has two types:

1. The point subthreshold swing (SS_{POINT}) [25, 28]

It is defined as the reciprocal of the actual slope of the I-V characteristics at a particular gate voltage (V_{GS}) as obtained in

$$(SS_{POINT})_{V_{GS}} = \left(\frac{dV_{GS}}{dLog\,(I_{DS})}\right)_{V_{GS}} \quad (1)$$

2. The average subthreshold swing (SS_{AVG}) [25, 28]

It is defined as

$$SS_{AVG} = \frac{(V_{TH} - V_{OFF})}{Log(I_{V_{TH}}) - Log(I_{OFF})} \quad (2)$$

As the V_{GS} rises beyond V_{TH}, the drain current continues to increase and the I_{ON} of the TFET is obtained at $V_{GS} = V_{DS} = V_{DD}$. The tunneling probability of the TFET is calculated by the Wentzel–Kramer–Brillouin (WKB) approximation as follows [5, 25] :

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$$T_{BTBT} \approx \exp\left[-\frac{4\sqrt{2m^*}\,E_g^{*\frac{3}{2}}}{3|e|\,\hbar\left(E_g^* + \Delta\Phi\right)}\sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}}t_{ox}t_{Si}}\right] \quad (3)$$

where m^* is the effective carrier mass, E_g^* is effective bandgap, e is the electron charge, ħ is the reduced Planck constant, ϵ_{Si} is the silicon relative permittivity, ϵ_{ox} is the relative permittivity of the gate oxide, t_{ox} is the gate dielectric thickness, t_{Si} is the silicon film thickness and $\Delta\Phi$ is the energy overlap window, $\lambda_{ch} = \sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}}t_{ox}t_{Si}}$ is called the effective screening length in the channel.

The drain current of the TFET is proportional to the T_{BTBT} and the $\Delta\Phi$ as given in Equation 4 [25].

$$I_D \propto \exp\left[-\frac{4\sqrt{2m^*}\,E_g^{*\frac{3}{2}}}{3|e|\,\hbar\left(E_g^* + \Delta\Phi\right)}\sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}}t_{ox}t_{Si}}\right]\Delta\Phi \quad (4)$$

2.1 Effect of device parameters on TFET

We can conclude from equation (4) that the drain current can be boosted by the following procedures [25]:

- Increase the relative permittivity of the gate oxide (ε_{ox}) decrease the thickness of the gate oxide (t_{ox}) or decrease the silicon body thickness (t_{Si}). The effect of these parameters will appear in decreasing the effective screening length in the channel (λ_{ch}) which gives more steepness and increases the I_{ON} of the TFET.
- Using materials with low effective carrier mass (m^*) and a small bandgap (E_g).
- Increasing the source doping results in increasing the bandgap narrowing and decreasing the tunneling distance.

2.2 Ambipolar behavior of TFET

Ambipolarity characteristic of n-TFET refers to the conduction of current at both positive and negative gate voltages [25, 26, 29]. In *n*-type TFET, by applying a negative V_{GS}, the bands under the gate will be pushed up. Hence, the current will flow due to the tunneling of the electrons from the VB of the channel to the CB of the drain as shown in Fig. 4.

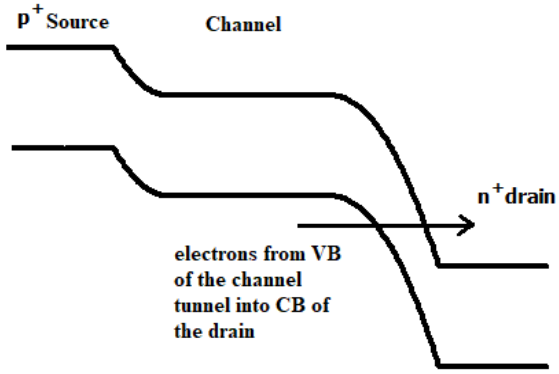

Fig. 4 Energy band diagram of the ambipolar state of an n-type TFET.

There are various techniques for reducing the ambipolar current in TFET including:

- Gate-drain underlap technique [29]30].
- Gate-drain overlap technique [30].
- Using the spacer between the gate and the drain [31].
- Lowering the drain doping [31].
- Use materials with a large bandgap on the drain side [31].

3. Analytical Modeling of TFET

Researchers have developed more analytical models of TFETs based on various architectures and different gate geometries to enhance the device's performance.

Intended for simple derivation, some analytical models assume that the TFET operates in the subthreshold region to ignore the presence of the mobile carriers and it operates without taking into account the depletion regions of the source and the drain. An analytical model is proposed by T.S. A. Samuel et al. [32] for a silicon-on-insulator (SOI) TFET where the two-dimensional (2-D) Poisson equation is solved using the parabolic approximation technique as obtained in Fig. 5. The 2-D Poisson/Laplace equation is given by

$$\frac{\partial^2\phi(x,y)}{\partial x^2} + \frac{\partial^2\phi(x,y)}{\partial y^2} = 0 \quad (5)$$

where $\phi(x,y)$ is the body potential which defined as

$$\phi(x,y) = c_0(x) + c_1(x)\,y + c_2(x)\,y^2 \quad (6)$$

Where the constants $c_0(x)$, $c_1(x)$ and $c_2(x)$ will be calculated by applying the boundary conditions

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obtained in Equations (7-10) to Equation (6). The boundary conditions in the channel region are given

1) The potential value at the source end

$$\phi(0, y) = \phi_{bi} \qquad (7)$$

2) The potential value at the drain end

$$\phi(L_{ch}, y) = \phi_{bi} + V_{DS} \qquad (8)$$

3) The electric flux continuity at the gate-oxide interface

$$\frac{\partial \phi(x,y)}{\partial y}\Big|_{y=0} = \frac{\phi_s(x) - V_{GS} + V_{FB}}{t_{ox}} . \frac{\varepsilon_{ox}}{\varepsilon_{si}} \qquad (9)$$

4) The electric field at $y = t_{si}$

$$\frac{\partial \phi(x,y)}{\partial y}\Big|_{y=t_{si}} = 0 \qquad (10)$$

where ϕ_{bi} is the built-in potential, V_{FB} is the flat band voltage, V_{GS} is the gate-to-source voltage, V_{DS} is the drain-to-source voltage, ε_{ox} is the SiO_2 relative permittivity, ε_{si} is the Si relative permittivity, t_{ox} is the oxide thickness and the surface potential $\phi_s(x) = \phi(x,y)|_{y=0}$.

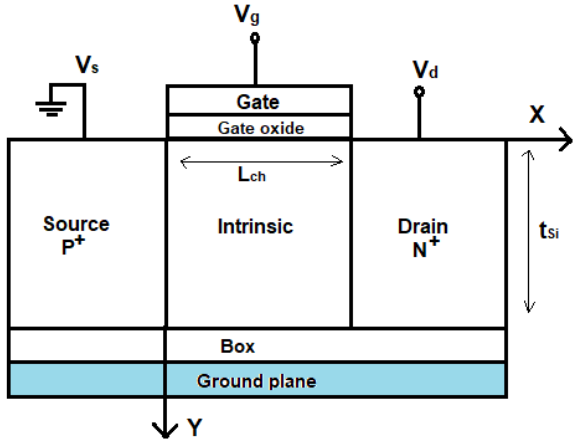

Fig. 5 single-gate SOI TFET structure [32].

The lower side of the buried oxide layer (BOX) is grounded and this layer the thickness is considered to be very thin to neglect the potential over this region. Therefore, the potential at the upper side of the BOX is assumed to be zero. The lateral electric field (E_x) and the vertical electric field (E_y) are calculated by

$$E_x(x,y) = -\frac{\partial \phi(x,y)}{\partial x} \qquad (11)$$

$$E_y(x,y) = -\frac{\partial \phi(x,y)}{\partial y} \qquad (12)$$

The tunneling generation rate (G_{BTBT}) according to Kane's model is given by

$$G_{BTBT} = A \frac{|E|^2}{\sqrt{E_g}} e^{\left[-B \frac{E_g^{3/2}}{|E|}\right]} \qquad (13)$$

where $|E| = \sqrt{E_x^2 + E_y^2}$ is the magnitude of the electric field and E_g is the band gap energy.

Then, the drain current can be calculated by G_{BTBT} integration over the tunneling volume

$$I_{DS} = q \int G_{BTBT}\, dV \qquad (14)$$

Many analytical models were proposed for Double Gate TFET (DGTFET) such as T. Samuel and N. Balamurugan [33]. They solved the 2-D Poisson equation using the parabolic approximation technique with boundary conditions referred to in equations (7,8) and added the electric–flux continuity at the gate's oxide interfaces for the two metal gates. A 2-D analytical surface potential model of heterostructure DG TFET with channel-source junction-pocket is proposed by K. Dharavath and A. Vinod [34]. The Poisson's equation is solved in the two regions of the channel using the boundary conditions referred to in equations (7,8) by adding the surface potential continuity and the electric field continuity at the boundary of two different doping concentration regions. M. Sharma et al. [35] presented an analytical model for dopingless DGTFET with a spacer layer between the source–channel region and a spacer layer between the drain–channel region. They classified the dopingless DGTFET structure into five regions. The potentials in the three regions (under the spacer layer near the source, under the spacer layer near the drain, and at the intrinsic region) are derived by solving the 2-D Poisson equation. Furthermore, the potentials at the source region and the drain region are calculated by electrostatic-based work-function-induced doping. The tunneling Generation rate is calculated using the Kans's model with E_{avg} which is calculated using the minimum tunnel. Moreover, analytical models for Triple Material Gate TFET are presented in C. Usha and P. Vimala [36] and S. Gupta and S. Kumar [37].

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On the other hand, modeling GAA TFET is different from single gate or double gate TFET modeling in that solving Poisson's equation with cylindrical coordinates. N. Balamurugan et al. [38] developed an analytical model of the Dual Material GAA Stack Architecture of TFET (DMGAASA TFET) based on the Poisson equation in cylindrical coordinates as follows:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\,\frac{\partial\phi\,(r,z)}{\phi r}\right)+\frac{\partial^2\phi(r,z)}{\partial^2 z}=\frac{q\,N_A}{\varepsilon_{Si}} \quad (15)$$

where $\phi(r,z)$ is the electrostatic potential in the silicon film, $0 \le z \le$ channel length (L) and $0 \le r \le$ radius of the silicon film (R).

S. Dash, and G. Mishra [39] presented an analytical model for a cylindrical gate TFET (CG-TFET) by solving the 2-D Laplace equation in the cylindrical coordinates. The electric field, the drain current, and the threshold voltage are derived by using the potential at the center of the cylinder. M. Suguna et al. [40] developed an analytical model of triple material surrounding gate junctionless TFET (TMSG JLTFET) with three different individual gates using the finite difference method in solving Poisson's equation. The Subthreshold Swing is calculated as

$$SS=\frac{K_B\,T}{q}\ln 10\left(\frac{\partial\Psi_s}{\partial V_{gs}}\right)^{-1} \quad (16)$$

On the other hand, accurate analytical models included the drain and the source depletion regions to ensure correct boundary conditions. Y.Yahia et al. [41] proposed a pseudo 2-D model for DG-TFET while considering the source and the drain depletion regions as shown in Fig. 6. The drain current can be approximated as

$$I_{BTBT}=q\,t_s\,L_T\,A_k\,E_{av}^2\,exp\left(-\frac{B_K}{E_{av}}\right) \quad (17)$$

where $E_{av}=\frac{E_g}{qL_T}$ is the average electric field in the x-direction and L_T is the shortest tunnel length.

Also, M. Bardon et al. [42], S. Kumar et al. [43], C. Usha and P. Vimala [44], and G. Jain et al. [45] proposed analytical models taking into account the depletion regions of the source and the drain.

Several analytical studies on TFETs considering mobile charge carriers have been carried out to increase the accuracy of models. For high gate voltage, the validity degrades for the models that neglect the influence of the channel mobile carriers on the tunnel FET electrostatics. M. Gholizadeh and S. Hosseini [46] presented an analytical model for DGTFET using a solution of the 2-D Poisson equation considering the influence of the mobile charge carriers.

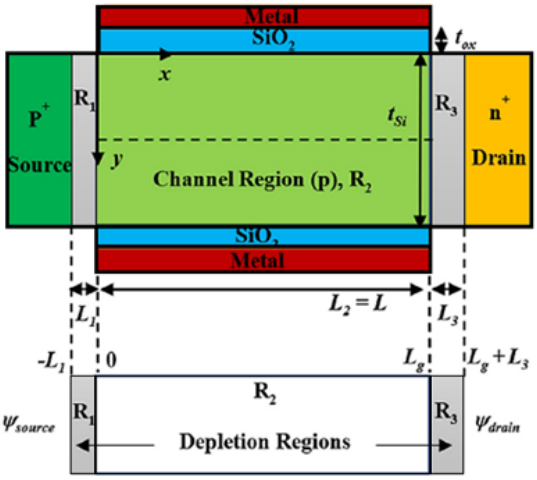

Fig. 6 The structure of DG-TFET with the device regions [41].

The electrostatic potential is developed using the superposition principle as the summation of two terms i.e., the solution of the 1-D Poisson's equation and the solution of the 2-D Laplace equation. Their model well extracted both the subthreshold and super-threshold currents of the device. H. Xu and Y. Dai [47] proposed a more accurate analytical model of DGTFET by considering the effect of mobile charges and the interface-trapped charges.

On the other hand, models [48, 49] predicted the electrostatic potential by considering the effect of mobile charges in the channel taking into account the source and the drain depletion regions.

4. Numerical Simulation

Numerical simulations can be used to quickly and inexpensively investigate different TFET architectures instead of performing experiments. In semi-classical simulators, a mesh or grid is used to specify the structure of the device. A finer mesh is defined in areas where high precision is required and where the potential or carrier concentration changes rapidly [25].

The direct tunneling models are either local tunneling models or nonlocal tunneling models. Local tunneling models can be easily implemented in a simulator, but they cannot accurately capture the BTBT physics as a result of assuming a constant electric field over the tunneling length. Local models are simple and easy to use, making them suitable for the analytical models, but less suitable for accurately simulating TFETs [50]. The

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local tunneling models are Kane's model, Schenk's model, and Hurkx's model [25]. The nonlocal model provides a dynamic tunneling path starting from the VB to the CB or vice versa in the direction of the electric field [51]. Therefore, it is widely used in TFET simulations because it accurately models the physics of the device. Chander et al. [51] analyzed various models such as the Non-Local model, Hurkx model, Schenk model, and Simple model on asymmetric Silicon Germanium-On-Insulator n-channel TFET. The non-local model presented the highest I_{on} to I_{OFF} current ratio and the smallest point subthreshold swing compared to the other models as obtained in Table 1.

Table 1 I_{on} /I_{OFF} ratio and point subthreshold swing of the different models.

Models	Non-Local model	Schenk model	Hurkx model	Simple model
I_{on} /I_{OFF} ratio	3.9×10^9	3.9×10^7	1.8×10^5	4.2×10^7
point subthreshold swing (SS)	37.1	69.2	85.3	102.1

Various models can be defined in TCAD simulators for more realistic results of TFET, i.e. mobility models, recombination models, band gap narrowing, velocity saturation Fermi–Dirac statistics, etc. There are three solution methods in these TCAD simulators, i.e. GUMMEL, NEWTON, and BLOCK [52]. Several simulators are used such as the Silvaco TCAD simulator and Sentaurus that provide efficient BTBT models.

The Silvaco / Atlas TCAD simulator is a physically based 2-D or 3-D device simulator that predicts the electrical performance of a given semiconductor structure [53]. Fig. 7 shows the simulation flow of the Atlas simulator and the order of ATLAS commands is obtained in Table 2.

Basic physics-based semiconductor equations are solved using numerical methods at each mesh point to predict the device operation. The physics-based equations are Poisson's equation, the continuity equations for the electrons and holes, and the current equations of the electrons and holes [54].

D. Madadi and S. Mohammadi [55] proposed a GAA InAs–Si heterojunction vertical TFET with a triple metal gate. The switching characteristics of the proposed TFET are improved as a result of the narrow bandgap source and the enhanced control of the channel. They used a SILVACO TCAD device simulator with suitable models to study the TFET characteristics. The device simulator is calibrated by reproducing the experimental data of a fabricated InAs–Si vertical TFET [56] to validate their simulation results as obtained in Fig. 8. The simulated results and the reported data have a good agreement. H. Xie and H. Liu [57] proposed a dual-material gate heterostructure JLTFET biosensor. Silvaco TCAD simulator is used with appropriate physical models to simulate the proposed device. The simulation models are calibrated by regenerating the reported results in [58] as obtained in Fig. 9.

Furthermore, many studies have been done on TFET with suitable models using Silvaco as obtained in Refs. [7, 13, 34, 35]. Moreover, Sentaurus TCAD software numerically simulates the electrical behavior of the semiconductor devices. Terminal voltages, currents, and charges are calculated based on the physical equations describing the conduction mechanisms and the carrier distribution. It solves each step through an iterative process. The software contained many physical models of the semiconductor process; through these models, the electrical characteristics of the TFET can be simulated. Various TFET simulations using Sentaurus are presented in Refs [14, 16, 38, 40].

Also, the set of non-linear equations derived from the TFET analytical models can be modeled and solved by MATLAB software as in [59, 60].

On the other hand, the full quantum simulation becomes essential as a result of the shrinking of device dimensions. However, full-band quantum transport simulators require much longer running times compared to semi-classical simulators [25]. Non-equilibrium Green's functions (NEGF) method is considered the most applicable quantum transport model for small device dimensions such as CNT TFET [22, 23] and GNR TFET [24, 61].

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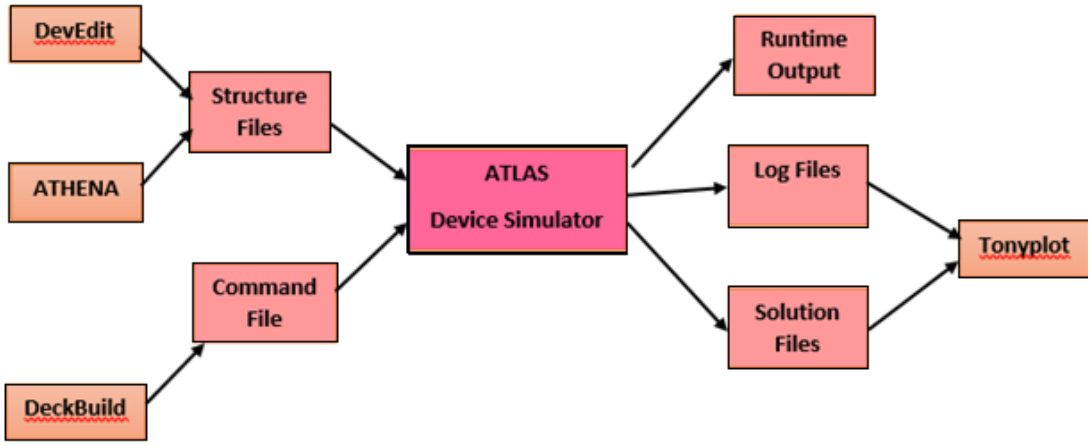

Fig. 7 The simulation flow of Atlas simulator.

Table 2 The order of ATLAS commands

Group		Statements
Structure specification	These statements define the structure of the model.	MESH, REGION, ELECTRODE and DOPING
Models specification of the material	These statements identify the physical models and the material parameters.	MATERIAL, MODELS, CONTACT and INTERFACE
Numerical methods	The used numerical methods in the simulation.	METHOD
Solution specification	These command the simulator to solve for certain bias conditions [54].	LOG SOLVE LOAD SAVE
Results analysis	These statements consist of commands to open and analyze the solution [54].	EXTRACT TONYPLOT

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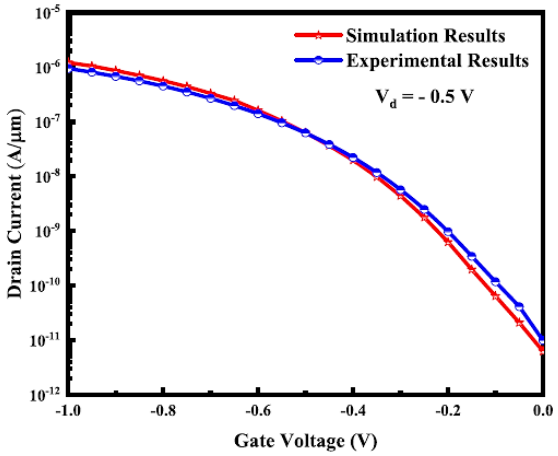

Fig. 8 Calibration of the vertical InAs–Si TFET reported in [56] and the Silvano simulator results [55].

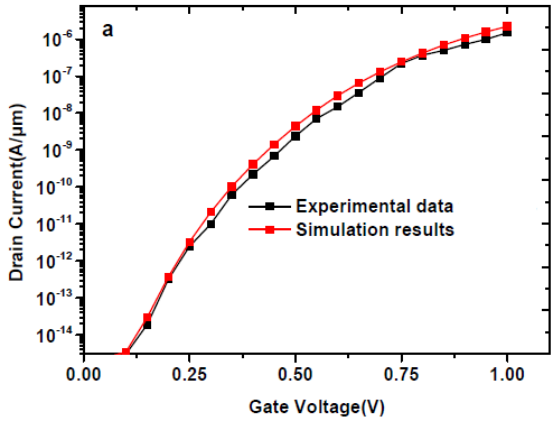

Fig. 9 Simulation models calibrated with experimental data [57].

5. TFET-based Applications

Various types of applications based on TFETs are being studied such as logic functions, inverters, multiplexers, memory cells, amplifiers, and biosensors.

5.1 Logic Gates based on TFET

S. Banerjee et al. [62] presented a realization of different logic functions, for example, OR, NOR, AND, and NAND using DGTFET with independent bias of the two gates. The OR function can be achieved when BTBT occurs at biasing any of the gate terminals by V_{DD} in conventional n-type DGTFET. Similarly, the NAND function is implemented using conventional p-type DGTFET. However, to implement the AND function, the BTBT should occur only at biasing the two gate terminals by V_{DD}. Therefore, they achieved this by using gate-source overlap in n-type DGTFET while choosing a suitable silicon body thickness. Adding source-gate overlap increased the tunnel width and eliminated the surface BTBT, which reduced the current when a single gate terminal was biased to logic "1". Therefore, a small I_{OFF} current is detected when the gate terminals are biased to logic "00", "01", and "10". Tunneling occurred in the TFET body t_{si} due to the mutual action of the top and bottom gates, leading to a high I_{ON} when the gate terminals are biased at logic "11". Similarly, the NOR function is implemented using p-type DGTFET with gate-source overlap to ensure that BTBT occurs only when the two gate terminals are grounded.

S. Garg and S. Saurabh [63] proposed a technique for the implementation of XOR and XNOR logic functions using dual-material DGTFETs exploiting the unique property of ambipolarity of the TFETs. Moreover, V. Ambekar and M. Panchor [64] presented a dual pocket-heterojunction tunnel FET (HTJ-TFET), and M. Rahama and P. Banerji [65] proposed a silicon-based DG vertical TFET to implement different logic functions with improved subthreshold swing and high ON current.

5.2 TFET as a part of digital circuits

TFETs have been considered primarily for digital applications due to their possibility of realizing subthreshold swing below the theoretical limit of 60 mV/dec for MOS devices at room temperature [66] and a high I_{ON}/I_{OFF} ratio [67]. TFETs are used in different digital circuits such as inverters, Memory cells, and Multiplexers [70, 71].

For an inverter based on TFET, when the input moves from low to high and high to low, the inverter shows overshoot and undershoot, respectively. S. Mookerjea et al. [69] compared the transient response of Silicon DGTFET with its MOSFET transistor counterpart. This comparison showed that the silicon TFET inverter has a worse fall time delay than the MOSFET as a result of the low I_{ON} and the high Cgd of the TFET. Hence, they suggested using InAs with low effective mass and low bandgap material to increase the I_{ON} current. Inverter based on InAs TFETs displayed a smaller voltage overshoot/undershoot and improved the fall time delay as a result of decreasing the Miller capacitance and the high I_{ON} compared to Si TFETs. D. Paul and Q. Khosru [68] compared the performance of the inverter based on bilayer Phosphorene DGTFET and dual-material bilayer Phosphorene DGTFET.

On the other hand, Static Random Access Memory (SRAM) cells based on TFETs with different structures and different materials are presented in [8, 72]. The speed and stability of SRAM cells are improved by

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using TFET devices with a high I_{ON}/I_{OFF} ratio, low subthreshold swing, and low leakage current [8].

5.3 TFET as part of Amplifier

U. Dutta et al. [73] compared a GAA Hetero Dielectric Tri Material Gate TFET (HDTMGTFET)-based common source (CS) amplifier and MOSFET-based amplifier in terms of power dissipation and amplification factor. The comparison obtained that the CS Amplifier based on GAA TFET has higher gain and lower leakage power than the MOSFET-based amplifier.

P. Agopian et al. [1] compared the performance of a two-stage operational transconductance amplifier (OTA) circuit design with four TFET structures and MOSFET technology. The comparison shows that TFETs have superiority in low and medium-frequency applications.

5.4 TFET based biosensor

Biosensors are devices that can generate electrical signals from the physicochemical reactions of biomolecules [74]. Targeted biomolecule sensing consists of two steps biomolecule detection and transduction. Several parameters should be considered when designing an accurate biosensor such as sensitivity, response time, and ease of manufacturing.

D. Sarkar and K. Banerjee [75] proposed a Silicon nanowire-based TFET (SiNW TFET) biosensor with an electrolyte gate. To capture the target biomolecules, the intrinsic area is covered with a thin dielectric/oxide region functionalized with specific receptors. The charged captured biomolecules induced a gate effect, which modulates the tunneling barrier between the bands, thus modulating the tunneling current. However, electrolytic gates do not give better channel control due to noise. A. Gao et al. [76] presented a silicon nanowire TFET biosensor with a planner gate for better control of the electrical conduction as shown in Fig. 10.

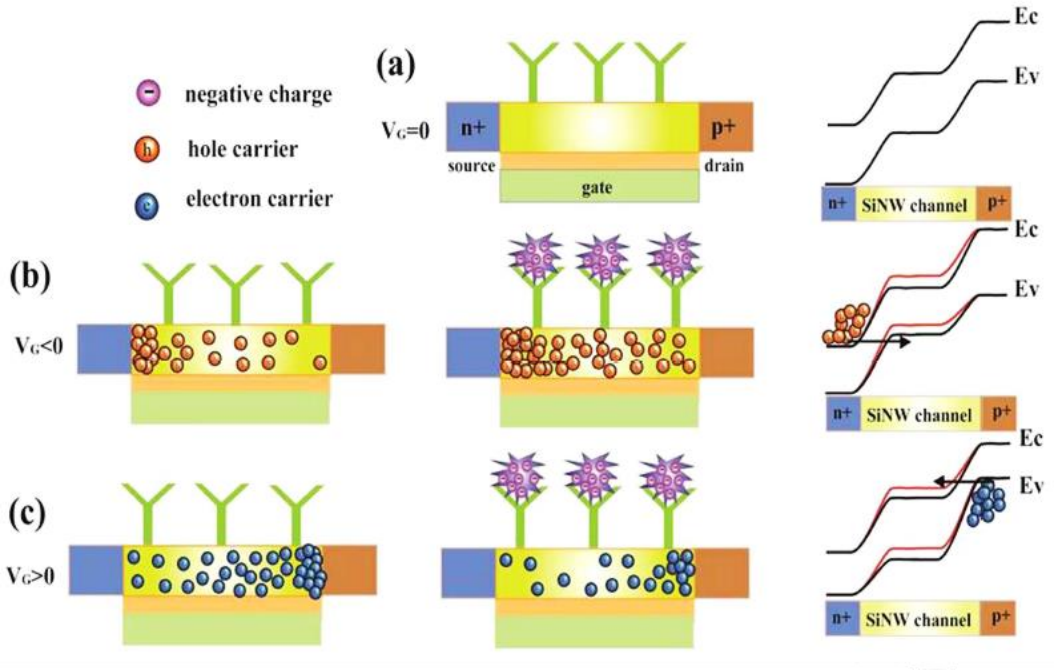

Fig. 10 Operating principle of SiNW TFET for detecting charged biomolecules [76].

On the other hand, the concept of dielectric modulated TFET are promising candidate as a biosensor in a lot of proposed research where a cavity region is created in the oxide layer below the gate electrode. The dielectric constant in the oxide is modulated once the targeted biomolecules are occupied and stabled in the cavity as obtained in Fig. 11. This resulted in changing the effective coupling between the gate and oxide layer which led to changes in current. A Double Gate TFET biosensor based on the dielectric modulated technique is presented by R. Narang et al. [77]. The proposed TFET-based biosensors have steeper *SS*, lower I_{off}, lower static power consumption, and higher sensitivity than conventional MOSFET biosensors.

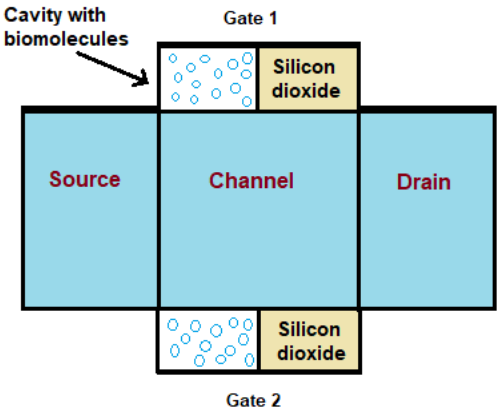

Fig. 11 TFET structure with nanocavity [78].

Furthermore, D. Abdi and M. Kumar [79] presented a TFET-based biosensor with nanogap-embedded overlapping gate-on-drain TFET. The sensing is based on the change of the TFET ambipolar current when the biomolecules with various dielectric constants are immobilized within the cavity. Ajay et al. [80] proposed a biosensor based on dielectric modulated DGTFET. The cavity is created at the source and drain sides to enable using the conduction of n-TFET for sensing the biomolecules by applying positive and negative voltage.

6. Recent TFET structures

6.1 Gate All Around TFET (GAA TFET)

GAA TFET gives better enhancement for channel gate control and reduces short-channel effects [28]. Fig. 12 shows the structure of a GAA nanowire TFET [81]. Surrounding gate structure increases the Si channel width per unit area resulting in increasing the device current per unit area [82].

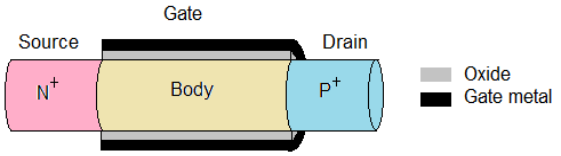

Fig. 12 The structure of GAANW TFET [81].

Various GAA TFET architectures are presented to improve the device performance, for example, dual gate material GAA TFET [60], heterojunction TFET with dual gate material [83], Stacked gate oxide SiO_2/HfO_2 cylindrical GAA TFET with source pocket engineered [83] and InAs-GaAs GAA TFET with hetero dielectric gate oxide [84]. Furthermore, comparisons between several nanowire TFET device architectures are studied in [85].

6.2 Fin TFET

Fin FET is considered a type of Multi-Gate FET (MGFET) which enriches the electrostatic control of the gate on the channel leading to improved device performance. A. Dharmireddy et al. [86] proposed Fin TFET with the double metal gate of separated work functions to enhance I_{ON}, decrease $I_{OFF,}$ and improve the subthreshold swing of the TFET as obtained in Fig. 13.

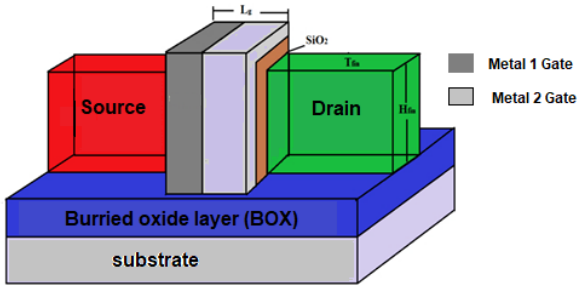

Fig. 13 3D view of Double Metal Fin gate Tunnel FET [87].

Furthermore, double metal Fin TFET with dual hetero gate oxide structure [88] and dopingless SiGe channel fin-shaped TFET [89] are studied to improve Fin TFET performance.

6.3 Nano sheet TFET

Nano-sheet FET is described as a GAA that wraps the channel in four directions to improve the electrostatics and the drive current [90]. The NSFET is also known as Multi Bridge Channel FET (MBCFET) or nano-beam [91]. The channel in the Nano-sheet FET appeared to be a horizontal sheet resulting in an increase in the channel area and increase in current density. S. Anthoniraj et al. [92] proposed a vertically stacked SiGe Nano-sheet TFET to improve the I_{ON} and the subthreshold swing as obtained in Fig. 14.

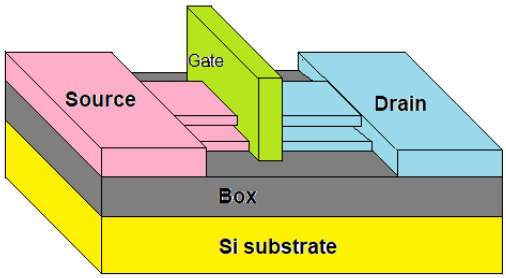

Fig. 14 SiGe nanosheet TFET diagram [92].

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Furthermore, a Hetero Dielectric Nano-sheet TFET with three channels using HfO_2 and SiO_2 dielectrics was created at the extended source-channel and drain-channel interfaces, respectively as presented in [93].

6.4 L-shaped TFET

L-shaped TFET exhibits BTBT perpendicular to the channel direction where the increase in tunneling area is based on the gate-source overlap that leads to an increase in the device current as obtained in Fig. 15. Unlike the planner TFET, the tunneling area is limited by the channel inversion layer thickness [94].

Various techniques are presented to improve the device performance of L-shaped gate or L-shaped channel TFETs as obtained in N. Abraham1 and R. James [95], P. Singh et al [96], and B. Ma et al. [97].

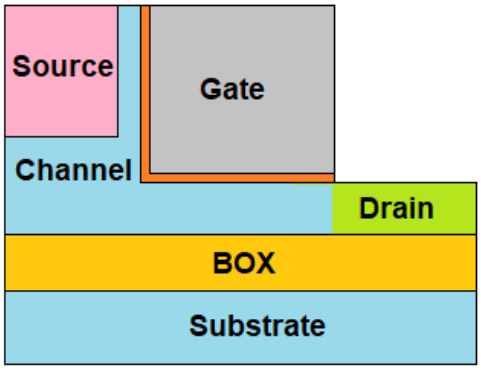

Fig. 15 Schematic of L-shaped TFET [94].

6.5 U-shaped TFET

W. Li et al. [98] studied a hetero-dielectric gate UTFET (HG-UTFET) with an N^+ pocket to ensure occurring strong BTBT in both the parallel and perpendicular directions of the channel as obtained in Fig. 16.

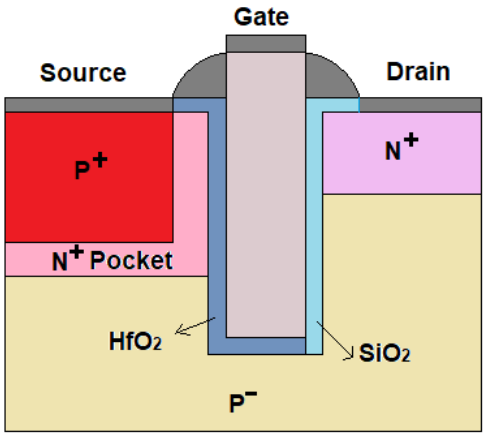

Fig. 16 HG-UTFET structure [98].

W. Wang et al. [144] proposed a U-shaped channel TFET (UTFET) with a SiGe source to increase the tunneling current. Moreover, S. Badgujjar et **a**l. [99] proposed a dual source U-shaped Vertical TFET where the tunneling area is doubled to enhance the ON-current and decrease the subthreshold swing.

6.6 T-shaped TFET

A silicon-based T-shaped gate dual-source TFET in Fig. 17 is presented by S. Chen et al. [100]. The overlap of the T-shaped gate offered a high tunneling junction area by introducing an n^+ pocket to further increase the ON current. P. Dubey and B. Kaushik [101] proposed an III-V heterojunction T-shaped TFET to increase ON current and improve the SS of the device. B. Goswami et al. [102] compared three T-shaped Dual gate TFETs with different materials: Silicon, Gallium Arsenide, and Silicon-Gallium Arsenide.

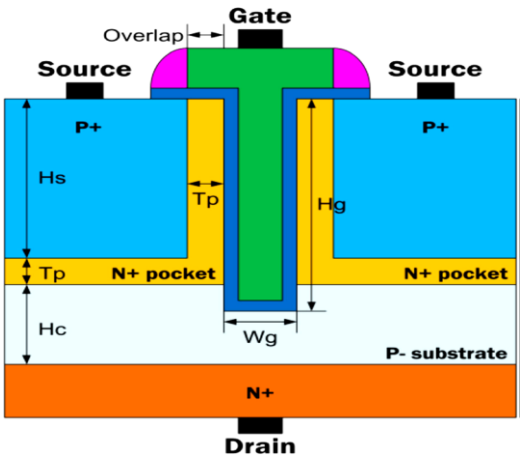

Fig. 17 The structure of T-shape gate dual-source TFET (TGTFET) [100].

7. Conclusions

This paper explains the physics of TFET which depends on the BTBT mechanism that breaks the physical limits of 60 mV/dec subthreshold swing and results in a low OFF current of the device. Due to ambipolar conduction and low ON current of TFET compared to MOSFET, various structures and materials of TFET are investigated to improve the device performance. This paper reviewed different analytical models and numerical simulations of TFET architectures. TFETs are good choices for different applications, such as logic gates, inverters, memory cells, amplifiers, and biosensors with low power consumption.

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